Analysis of PLL Phase Noise Effect for High Data-rate Underwater Communications [†]

Chong Hyun Lee[1*], Jinho Bae [1], Changku Hwang[2], Seung Wook Lee[3] and Jungchae Shin[3]

[1]*Department of Ocean System Engineering, Jeju National University, Jeju 690-756, Korea*

[2]*Hadware Division, Oracle Inc., 4030 George Sellon Cir, Santa Clara, CA, 95054, USA*

[3]*Gumi Plant, Hanwha Corporation., 258 Kongdandong, Gumi, Kungbuk, 730-030, Korea*

Abstract

High data-rate underwater communications is demanded. This demand imposes stringent requirements on underwater communication equipment of phase-locked-loop (PLL). Phase noise in PLL is unwanted and unavoidable. In this paper, we investigate the PLL phase noise effect on high order QAM for underwater communication systems. The phase noise model using power spectral density is adopted for performance evaluation. The phase noise components considered in PLL are reference oscillator, voltage controlled oscillator (VCO), filter and divider. The filters in PLL noise are assumed to be second order active and passive low pass filters. Through simulation, we analyze the phase noise characteristics of the four components and then investigate the performance improvement factor of each component. Consequently, we derive specifications of VCO, phase detector, divider to meet performance requirement of high data-rate communication using QAM under phase noise influence.

Keywords: Underwater Communication; Phase-Locked-Loop (PLL); Voltage Controlled Oscillator (VCO); Quadrature Amplitude Modulation (QAM); Phase noise

1. Introduction

There is a considerable demand of high data rate underwater communications which can transmit one or more bit per second(bps) per Hz of bandwidth for commercial as well as military purpose. To meet this demand, several systems have been devised which achieve data rates of the order of tens of kilobits per second over ranges of a few kilometers. This demand imposes more stringent requirements on underwater communication equipment. A better receiving terminal of underwater communication system can be improved by reducing phase noise in the phase-locked-loop (PLL).

Phase-locked-loop (PLL) is a closed loop control system that uses negative feedback to maintain constant (locked) output frequency and phase to the frequency and phase of input. The main elements of this PLL are voltage control oscillator (VCO), phase detector (PD), loop filter and main divider. The PLL has achieved "lock" when the difference between the output of VCO and the reference signal is zero.

Noise in PLL is classified into two categories, which are amplitude noise and phase noise. Amplitude noise is detected and terminated easily, whereas phase noise is difficult to identify and express in an equation due to unpredictable characteristics of electronic components. Therefore, it is important to study the characteristic of the phase noise because it affects the system performance and the signal to noise ratio (SNR).

In this paper, we assume four noise sources which are originated from reference oscillator, loop filter, voltage-controlled oscillator, and main divider. Then

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*Corresponding author. Tel.: +82 64 754 3481, Fax.: +82 64 751 3480.
E-mail address: chonglee@jejunu.ac.kr.

we investigate individual noise characteristics by analyzing the integrated phase noise power obtained by accumulating each sources. Next, we derive specification of each component for secure communication performance in high order QAM system under phase noise effect. Finally, we present computer simulation results of noise sources effect on high data-rate communications.

2. Phase Noise Model for PLL Synthesizer

In this section, we introduce phase noise model of PLL synthesizer [1]. The components of PLL are shown in the figure 1.
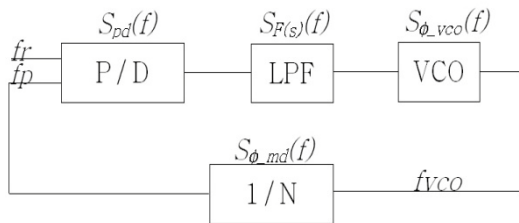

Fig. 1 Components of PLL

$$S_\phi(f) = k_0 + \frac{k_1}{f} + \frac{k_2}{f^2} + \frac{k_3}{f^3} + \frac{k_4}{f^4} \qquad (1)$$

, where the k_O represents thermal noise which acquires 0 dB/dec slope region and k_1/f is flicker noise which represents –10 dB/dec slope region.

Each noise model has different characteristics and different slope in offset frequency region. With this general form of noise model, we use noise model for each components. The phase noise model of VCO can be written as

$$S_{VCO}(f) = k_{0\_VCO} + \frac{k_{1\_VCO}}{f^2} + \frac{k_{2\_VCO}}{f^3} \qquad (2)$$

The phase noise model of divider can be written as

$$S_{\phi\_md}(f) = k_{0\_md} + \frac{k_{1\_md}}{f} \qquad (3)$$

The phase noise model of reference oscillator can be written as

$$S_{\phi\_ref}(f) = k_{0\_ref} + \frac{k_{1\_ref}}{f} + \frac{k_{2\_ref}}{f^2} + \frac{k_{3\_ref}}{f^3} \qquad (4)$$

Then the combined noise model of divider and reference oscillator can be written as

$$S_{mult}(f) = N^2 \left[S_{\phi\_md}(f) + \frac{S_{\phi\_ref}(f)}{R^2} \right] \qquad (5)$$

, where the N represents factor of the divider.

Based on the phase noise model $S_{\_a}(f)$, the 2nd order active filter can be written as follows:

$$S_{\_a}(f) = S_{\_mul\_out}(f) + S_{\_a\_fil}(f) + S_{\_vco\_out}(f) \qquad (6)$$

Similarly, $S_{\_p}(f)$, passive filter PLL phase noise can be written as follows:

$$S_{\_p}(f) = S_{\_mul\_out}(f) + S_{\_p\_fil}(f) + S_{\_vco\_out}(f) \qquad (7)$$

The $S_{\_vco\_out}(f)$ in (6) is the closed loop phase noise model of $S_{VCO}(f)$ in (2) and can be expressed as

$$S_{\_vco\_out}(f) = S_{vco}(f) \cdot \left| \Theta_{CL\_vco}(jf) \right|^2 \qquad (8)$$

, where $\Theta_{CL\_vco}(jf)$ is the transfer function of closed loop.

The $S_{\_mul\_out}(f)$ in (7) is the closed loop phase noise model of $S_{mult}(f)$ in (5) and can be expressed as

$$S_{\_mul\_out}(f) = S_{mult}(f) \cdot \left| \Theta_{CL\_mult}(jf) \right|^2 \qquad (9)$$

, where $\Theta_{CL\_mult}(jf)$ is the transfer function of divider and reference oscillator. The $S_{\_a\_fil}(f)$ and $S_{\_p\_fil}(f)$ in (6) and (7) are noise model of passive and active filter, respectively.

Based on the models described, we derive requirement of phase noise margin of PLL. To begin with, we present bit error rate (BER) of high order QAM communication system. The theoretical bit error rate for a matched Nyquist filter QAM receiver for M = 4, 16, 64, 256 and 1024 assuming equiprobable symbols and no FEC can be written as follows:

$$P(S/N) = \frac{1 - \left[1 - 2(1 - \frac{1}{\sqrt{M}})Q(\sqrt{\frac{3 * S/N}{M - 1}}) \right]^2}{\log_2 M} \qquad (10)$$

where M means M-QAM and S/N represents signal to noise ration in two-sided Niquist bandwidth. Then, the accumulated phase can be found by using the following equation [2]

$$\Delta dB = 10\log(1+10^{\frac{-\Delta N}{10}}) \qquad (11)$$

where N represents the SNR loss due to phase noise, i.e. SNR – phase noise power.

By substituting (11) into (10), we can obtain BER degradation due to phase noise. For example, if accumulated phase noise power equals -57.08dBc, then we can obtain the BER curve vs. SNR, plotted in Figure 2.
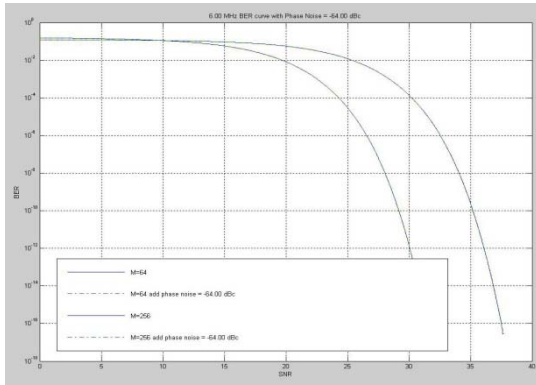
Fig. 2 BER formance of 64 and 256 QAM when integrated phase noise is -57.08 dBc

As shown in figure (2), SNR loss is negligible for both 64 and 256 QAM, when BER equals 10^{-8}. However, if accumulated phase noise power equals -38.12dBc, then we can observe SNR loss of 64 and 256 QAM equals to 0.36 dB and 1.70 dB, respectively. The BER curve vs. SNR, are plotted in figure 3. From the results, we can conclude that if 256 QAM system requires SNR loss of 1.70 dB, then integrated phase noise should be less than -38.12dBc. With this phase noise power, we can find the specification of PLL components to meet the phase noise requirement. This procedure proceeds in the following section.
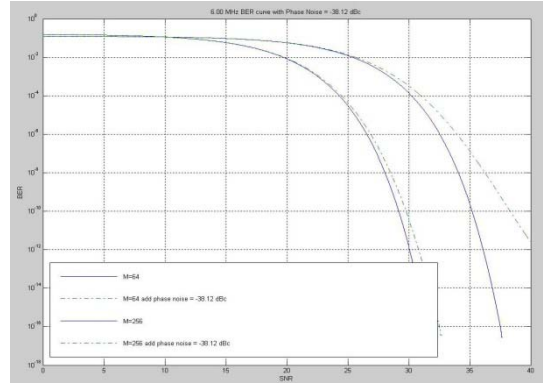
Fig. 3 BER formance of 64 and 256 QAM when integrated phase noise is -38.12 dBc

3. Simulation Results

3.1 Integrated Phase noise

In this section, we present integrated phase noise simulation results based on model described in previous section.

The parameters of PLL components to meet requirement that the SNR loss should be less than 0.36 and 1.70 dB are summarized in the following table 1.

Table 1. Parameters for phase noise less than -38.12 dBc

Parameters	Specification
K_vco	$K0\_vco = 10^{-15.5}$, $K1\_vco = 10^{-3}$, $k2\_vco = 10^{-0.7}$
K_md	$K0\_md = 10^{-15.5}$, $K1\_md = 10^{-12.5}$
K_ref	$K0\_ref = 10^{-15.8}$, $K1\_ref = 10^{-12.7}$, $K2\_ref = 10^{-9.86}$, $K3\_ref = 10^{-7.82}$
K_R	$K0\_R1 = 10^{-12.64}$, $K0\_R2 = 10^{-12.92}$
K_op	$K0\_OP = 10^{-17.045}$, $K1\_OP = 10^{-16.02}$
Kp	$KP = 0.5$
N	$N = 1000$
Kv	$Kv = 10^{7}$

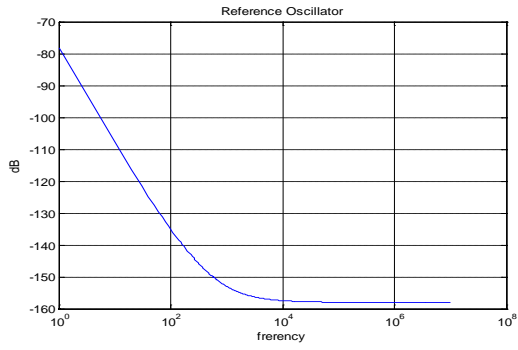The phase noise output of the oscillator model is shown in the Figure 4.

Fig. 4 Noise model of oscillator

The phase result of closed loop active low-pass active filter is shown in the Figure 5.
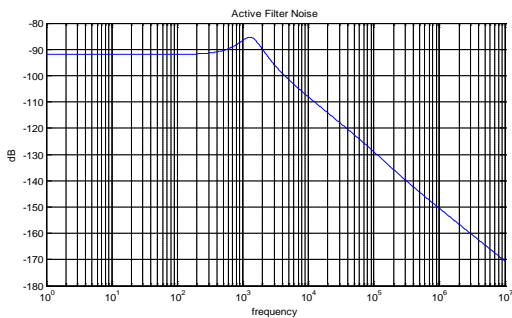

Fig. 5 Noise model of closed loop active low-pass active filter

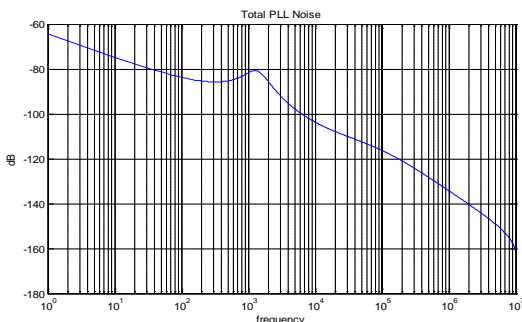The result of the accumulated noise of active lowpass active filter is shown in the Figure 6.

Fig. 6 Total Noise model of active lowpass active filter

Finally, the total integrated PLL noise is shown in the Figure 7.
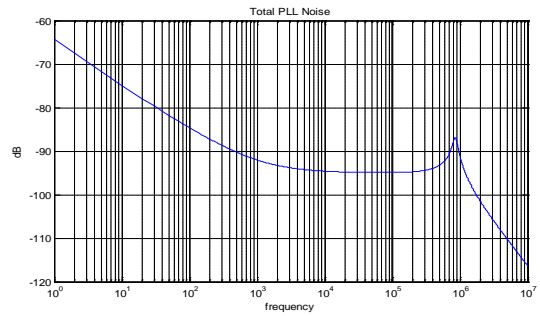

Fig. 7 Total PLL Noise model of active lowpass active filter

As shown in the figures, the presented noise model are well matched to physical noise.

Next, we present the phase noise effect on the constellation of 64 QAM system. The simulation parameters are as follow:

● Number of data: 12,000
● SNR: 20dB
● Phase noise variation: |2| and |20| degree
● Modulation: 64QAM
● Channel: AWGN Channel

The constellation variation at phase noise variation = |2| degree is shown in the Figure 8.
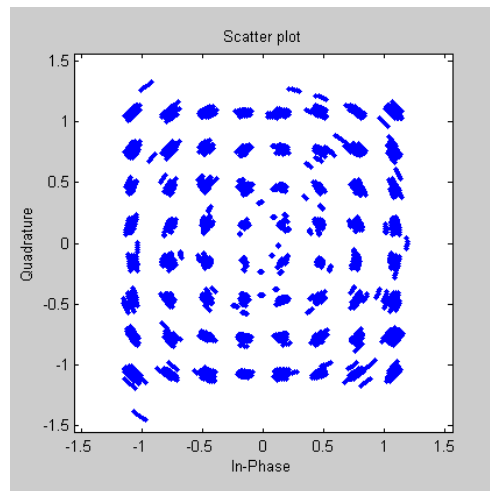

Fig. 8 Constellation of 64 QAM at at phase noise = |2|

The constellation variation at phase noise = |20| degree is shown in the Figure 9.
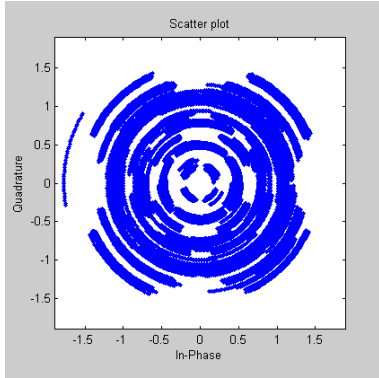
Fig. 9 Constellation of 64 QAM at at phase noise = |20|

As shown in the figures, the phase noise makes large impact on the performance of high data-rate communication.

3.2 Requirement Analysis of PLL Specification

In this section, we present phase noise simulation results based on model described in previous section. The 2nd order active filter is used and signal bandwidth is assumed to be 6MHz. For simulation we only consider divider values while fixing other parameters in Table 1.

For N = 10, total phase noise and integrated noise are shown in the following figure 10. In the figure, we can observe that integrated phase noise is -64dBc. The phase noise of -64dBc gives negligible BER degradation, which can be seen in the figure 11. In the figures, we can observe no loss in SNR when required BER is 10^{-8}.
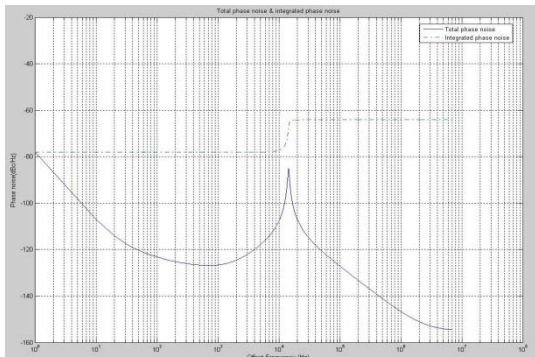

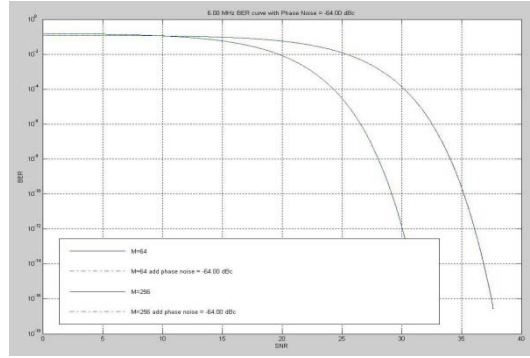Fig. 10 Total and Integrated Phase noise when N =10

Fig. 11 BER performance of 64 ad 256 QAM when integrated phase equals -64 dBc

However, if N becomes 100, we can observe that the accumulated phase noise is -38dBc at 6 MHz bandwidth and the corresponding SNR loss at BER = 10e-8 by investigating the figures 12 and 13. The SNR loss for 64 and 256 QAM system s are 0.36 and 1.70, respectively.
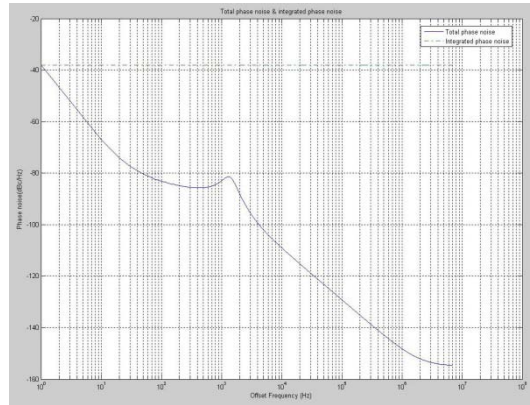

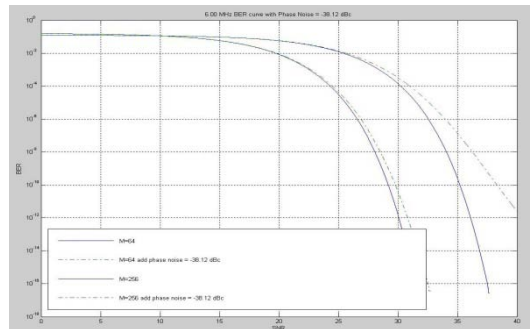Fig. 12 Total and Integrated Phase noise when N = 1000

Fig. 13 BER performance of 64 ad 256 QAM when integrated phase equals -64 dBc

The results of various N are summarized in the following table. As seen in the figures, we can observe that as N decreases, the integrated phase noise becomes smaller. Also, we can obtain the optimum divider value, N, generating the integrated phase noise of -38.12dBc, which causes in turn SNR loss of 0.36 and 1.70 dB for 64 and 256 QAM, respectively.

Though we perform simulation by changing N and fixing the other PLL parameters, the changes of other PLL parameters are possible. The requirement analysis using combination of other parameters to satisfy the given SNR loss can be obtained via changing other parameters.

Table 2. Integrated Phase noise according to N

		Integrated Phase noise
	10	-64.00
N	100	-57.08
	1000	-38.12

4. Conclusions

In paper, we present relationship between QAM communication system performance and integrated phase noise for high data-rate underwater communications. The phase noise models considered in PLL are reference oscillator, voltage controlled oscillator (VCO), active and passive low-pass filter and divider. By considering 64 and 256 QAM modulation and demodulation systems, we verified that if SNR loss due to phase noise is required to be less than 0.36 and 1.70, then integrated phase noise should be less than -38.12 dBc. Also we analyzed the phase noise characteristics of each PLL component to meet the phase noise requirement. The phase noise effect on PLL is also analyzed via computer simulation and then, we present the specification of phase noise requirement of PLL components for maintaining secure high data-rate underwater communication using QAM modulation and demodulation.

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