수직자기기록 채널에서 기록 밀도에 따른 반복복호 기법의 성능

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Performance Of Iterative Decoding Schemes As Various Channel Bit-Densities On The Perpendicular Magnetic Recording Channel

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요 약

본 논문에서는 직렬 연접 길쌈 부호와 LDPC 부호를 이용하여 수직자기기록 채널에서의 성능을 조사하였다. 실험과정에서 기록 밀도는 1.7, 2.0, 2.4, 2.8 일 때를 각각 실험하였다. 직렬 연접 길쌈 부호는 LDPC 부호보다 복호기의 구현 복잡도가 더 낮다. 직렬 연접 부호는 순환 구조적 길쌈 부호의 부호기와 복호기, 그리고 프리코더와 인터리버로 이루어져 있다. 본 실험에서 직렬 연접 길쌈 부호의 복호 알고리즘은 메시지 전달 알고리즘을 이용하였으며, LDPC 부호의 복호 알고리즘은 Sum Product 알고리즘을 이용하였다. 신호 검출기와 오류정정부호 사이에 반복 복호 기법을 적용한 터보등화기 기법을 적용하였고, 기록 밀도가 높아짐에 따라 직렬 연접 길쌈 부호가 LDPC 부호 보다 더 효율 적인 것을 보였다.

Key Words : Serial Concatenated Convolutional Codes(SCCC), Low-Density Parity-Check(LDPC) Codes, Perpendicular Magnetic Recording(PMR) Channel, Channel Iteration, Iterative Decoding.

ABSTRACT

In this paper, we investigate the performances of the serial concatenated convolutional codes (SCCC) and low-density parity-check (LDPC) codes on perpendicular magnetic recording (PMR) channels. We discuss the performance of two systems when user bit-densities are 1.7, 2.0, 2.4 and 2.8, respectively. The SCCC system is less complex than LDPC system. The SCCC system consists of recursive systematic convolutional (RSC) codes encoder/decoder, precoder and random interleaver. The decoding algorithm of the SCCC system is the soft message-passing algorithm and the decoding algorithm of the LDPC system is the log domain sum-product algorithm (SPA). When we apply the iterative decoding between channel detector and the error control codes (ECC) decoder, the SCCC system is compatible with the LDPC system even at the high user bit density.

Ⅰ. Introduction

To increase the storage capacity of hard disk drives (HDDs), magnetic recording systems require higher bit density. However, higher bit density systems are limited by inter-symbol interference (ISI) and thus have poor read performance. Storage systems require a detection algorithm that has a good bit-error rate (BER) performance. Noise predictive maximum likelihood (NPML) detection

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has been used for magnetic recording channels[1,2]. A better decoding scheme than NPML is required for good BER performance as the user bit density (UBD) required is getting higher. Thus, many researchers have emphasized iterative decoding.

Serial concatenated convolutional codes (SCCC) with channel iterative decoding have been shown to result in performance gains[3]. Iterative decoding codes have been investigated in high density magnetic recording channels to improve the low signal-to-noise ratio (SNR)[4,5]. The low-density parity-check (LDPC) codes or turbo iterative decoding schemes perform better than NPML on the PMR channel model. The Turbo codes, which is a parallel concatenated convolutional codes, is very complex to implement. SCCC using recursive systematic convolutional (RSC) codes are simpler than other iterative decoding, such as LDPC or Turbo codes. SCCCs perform better than NPML alone[6,7].

PMR channels have non-linear noise known as jitter[8]. Therefore, we simulate two systems with 80% jitter noise and 20% additive white Gaussian noise (AWGN). The main goal of the paper is to discover a less complex solution than LDPC codes. Therefore, we use RSC codes and additive decoding method, in particular the turbo-equalization. Turbo-equalization is the iterative decoding between the channel detector and the RSC decoder. Here, turbo-equalization is used in an SCCC system for improved performance. LDPC systems also use turbo-equalization between the channel detector and the LDPC decoder. Although the Viterbi algorithm is a simple decoding algorithm, it is not used here because it is not a soft-input soft-output (SISO) algorithm. Also, it is not the best one to use on the partial-response (PR) channel. Hence, the soft message-passing (MP) algorithm channel detector is used instead.

The soft message-passing algorithm channel detector is a forward-backward algorithm similar to the maximum aposteriori (MAP) algorithm. The SCCC system consists of a max-log MP algorithm channel detector and a max-log MP algorithm RSC decoder ,and the LDPC system consists of an max-log MP algorithm channel detector and a log-domain sum-product algorithm (SPA) LDPC decoder[7,9].

Ⅱ. PMR Channel Model

In a PMR channel, a signal transition step response can be modeled as follows[8].

$$g(t)=A\times\tanh\left(\frac{2t}{0.597\pi\times T_{50}}\right) \tag{1}$$

where A is the peak amplitude of this signal and T_{50} is the measured half of the unipolar pulse amplitude. $K=T_{50}/T_b$ is the normalized recording density and channel bit interval is T_b. The data sequence a_k (i.e., $a_k=-1$ or 1) is non return to zero (NRZ) binary data, and the superposition of the transition responses is the readback signal. The readback signal function is given below.

$$r(t)=\sum_{k=-\infty}^{\infty}a_k[g(t-kT)-g(t-(k+1)T)]+n_w(t)+n_j(t) \tag{2}$$

where $n_w(t)$ is the AWGN and $n_j(t)$ is the jitter noise. The channel SNR is defined as follows.

$$SNR=10\log_{10}\left(\frac{A^2}{\sigma_w^2+\sigma_j^2|g'(t)|^2}\right) \tag{3}$$

where σ_w^2 is the power of AWGN and $\sigma_j^2|g'(t)|^2$ is the power of the jitter. The value of the parameter A is 0.5.

Ⅲ. Review of Coding Methods

The main goal of this paper is to discover a less complex solution than LDPC codes. Thus, the RSC encoder/decoder is used here for simplicity. The turbo-equalization scheme called channel iteration is used to improve the performance using only the RSC codes.

3.1 SCCC with PR Equalized Recording Channel

The main core of the SCCC system is the

iteration between the channel detector and the RSC decoder. Fig. 1 illustrates the SCCC system with a PR equalized recording channel. The RSC codes uses the generator polynomial of $(31,23)_8$. This RSC codes encoder is illustrated in Fig. 2. The randdom interleaver is used, and precoder is $1/(1\oplus D^2\oplus D^3\oplus D^4\oplus D^5)$.

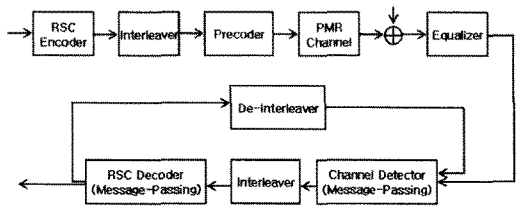

Fig. 1. SCCC system with PR equalized recording channel

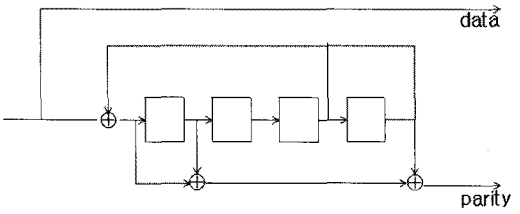

Fig. 2. RSC codes employed use the code polynomial $(31,23)_8$. It has four memories and four XOR operators

3.2 LDPC Codes with PR Equalized Recording Channel

The parity-check matrix of the LDPC codes used is 240 by 4336. The sizes of parity and original data are 240 and 4096 bits, respectively. The column weight of the LDPC is three, and the irregular LDPC is used. Also, for simple encoding, the structure of the parity-check matrix corresponds to the Richardson-Urbanke encoding technique. Fig. 3 shows the LDPC system with the message-passing channel detector.

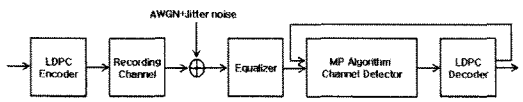

Fig. 3. LDPC system with PR equalized recording channel

3.3 The Number of Operators by using SCCC and LDPC

RSC encoder has four memories and four XOR operators. RSC decoder needs 65,536 memories (16 states by 4,096 ,trellis) and 32 adders (each node has two path, and sixteen states, sum of branch metric and path metric) and 16 comparators (sixteen states, compare of two path metric value, one path is decided by comparison). LDPC encoder has 1,040,640 memories (sub-matrix A,B,C,E,T, Φ) and seven multipliers and two XOR operations and two inverse matrix operations (T^{-1}, Φ^{-1}). LDPC encoding process is illustrated in Fig.4. LDPC decoding algorithm is follows:

step1: Update $L(r_{ji})$.
Step2: update $L(q_{ji})$.
Step3: update $L(Q_i)$.
Step4: Check syndrome.

Size of a parity check matrix is 240 by 4336. Therefore it needs 1,040,640 memories. The matrix was made by us, it has 12,792 number of one's and it is very sparse. Step 1 needs 1,040,640 memories ($L(r_{ji})$) and 12,792 comparators (each one's node needs one comparator, sign comparator) and 12,792 adders (each one's node needs one adder) and hyperbolic tangent function (HTF) and log function. Step 2 needs 1,040,640 memories ($L(q_{ji})$) and

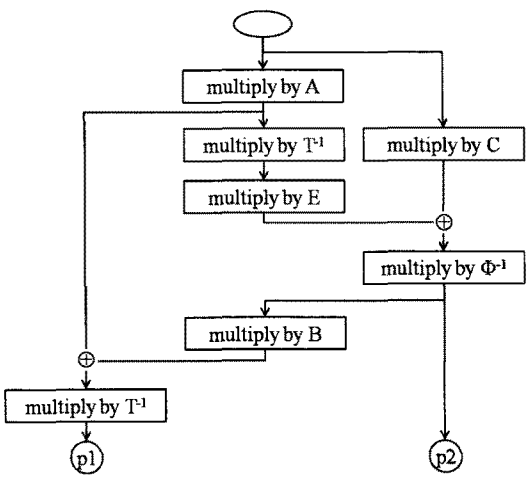

Fig. 4. Block diagram of LDPC encoding process.

12,792 adders (each one's node needs one adder). Step 3 needs 4,336 memories ($L(Q_i)$) and 4,336 adders (each LLR update). Step 4 needs one multiplier and one comparator. The LDPC system needs 3,126,256 memories and 29,920 adders and 12,793 comparators and one multiplier and HTF and log function, totally. This compared operators shown Table I. Log domain Sum-product algorithm is follows[14]:

Step 1:

$$L(r_{ji}) = \Big(\prod_{i' \in V_j \setminus i} \alpha_{i'j}\Big)\phi\Big(\sum_{i' \in V_j \setminus i} \phi(\beta_{i'j})\Big)$$

Step 2:

$$L(q_{ji}) = L(c_i) + \sum_{j' \in c_i \setminus j} L(r_{j'i})$$

Step 3:

$$L(Q_i) = L(c_i) + \sum_{j \in c_i} L(r_{ji})$$

Step 4:

$$\hat{c}H^T = 0$$

$$\hat{c} = \begin{cases} 1 & \text{if } L(Q_i) < 0 \\ 0 & else \end{cases}$$

Table I. Operations Coompared to SCCC system and LDPC System

	SCCC		LDPC	
	encoder	decoder	encoder	decodoer
Memories	4	65,563	1,040,640	3,126,256
Adders	4	32	2	29,920
Comparators	-	16	-	12,793
Multipliers	-	-	7	1
Functions	-	-	2 inverse matrix	HTF, log

Ⅳ. Simulation Results

Performances of the SCCC and LDPC systems are investigated when the user bit densities (UBD) are 1.7, 2.0, 2.4 and 2.8, respectively. The code rate is 0.944(4096/4336). The PR target used is PR(12321). That's because the PR(12321) is the ideal target model in the PMR channel Model. The noise is consisted of 80% jitter and 20% AWGN. The channel bit density is UBD/R, thus, the channel bit densities investigated are 1.799, 2.117, 2.540 and 2.964, respectively. Also, we simulate the NPML system, which has four noise-filter (NP) taps, for comparison the performance of two systems.

First, the BER performances are examined when the UBD is 1.7. Fig. 5 illustrates the BER performance of the LDPC system on PMR in accordance with the number of channel iterations. It shows that if the number of channel iterations increases, then BER performance improves. At 10^{-6} BER, after four channel iterations, it performs 3.5dB better than the NPML. If the LDPC system has no channel iterations, it performs 2.5dB better than the NPML.

Fig. 6 shows the performance of the SCCC system. It performs 2dB and 4dB better than the NPML after one and nine channel iterations, respectively. Fig. 7 compares the BER performance of the LDPC and SCCC systems in accordance with the number of channel iterations applied. It shows that the LDPC system obviously performs better than the SCCC system when there is no channel iteration. When there are four channel iterations, the two systems perform 3.5dB better than the NPML at 10^{-6} BER. Also, the SCCC system with four channel iterations performs better than the LDPC system with no channel iterations.

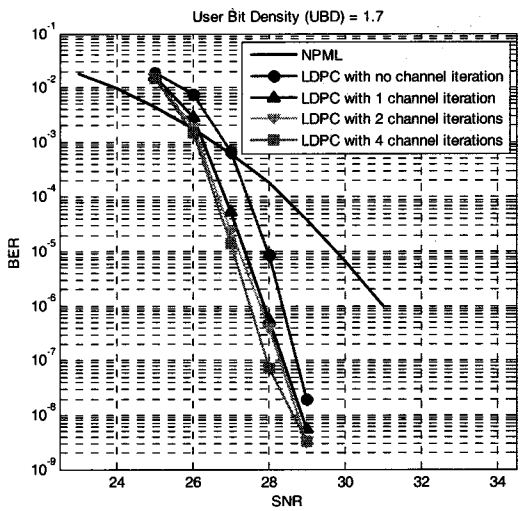

Fig. 5. Simulation results for the LDPC system on PMR in accordance with the number of channel iterations. (UBD=1.7)

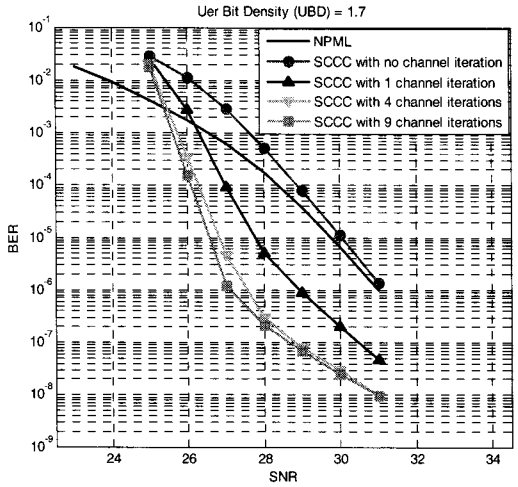

Fig. 6. Simulation results for the SCCC system on PMR in accordance with the number of channel iterations. (UBD=1.7)

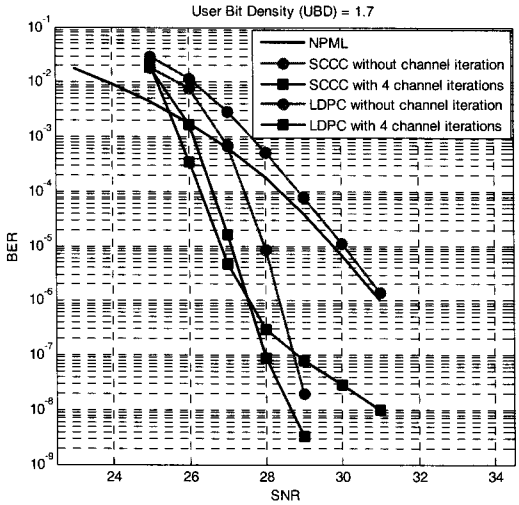

Fig. 7. Simulation results for the LDPC system and the SCCC system on PMR in accordance with the number of channel iterations. (UBD=1.7)

At the low SNR region ($10^{-2} \sim 10^{-6}$ BER), the SCCC system performs 0.3dB~0.5dB better than the LDPC system. The merit of the SCCC system is that it is less complex than the LDPC system, and the drawback is the response delay caused by the number of the channel iterations.

Second, BER performances are examined when the UBD is 2.0. Fig. 8 shows the performance of the LDPC and SCCC systems when the UBD is 2.0. The LDPC system performs 3dB better than the

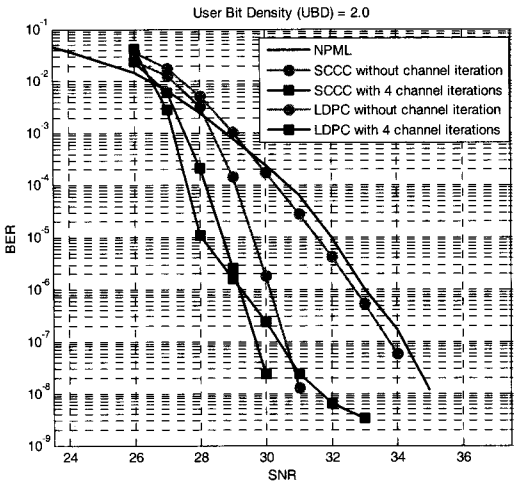

Fig. 8. Simulation results for the LDPC system and SCCC system on PMR in accordance with the number of channel iterations. (UBD=2.0)

SCCC system when there is no channel iteration. But, when there are four channel iterations, the SCCC system performs better than the LDPC system until it reached the SNR of 29dB. Also, the SCCC system with four channel iterations performs better than the LDPC system without channel iteration until 31dB SNR. The SCCC system without channel iteration performs 0.2dB better than the NPML.

Third, Fig. 9 shows the performance of the LDPC

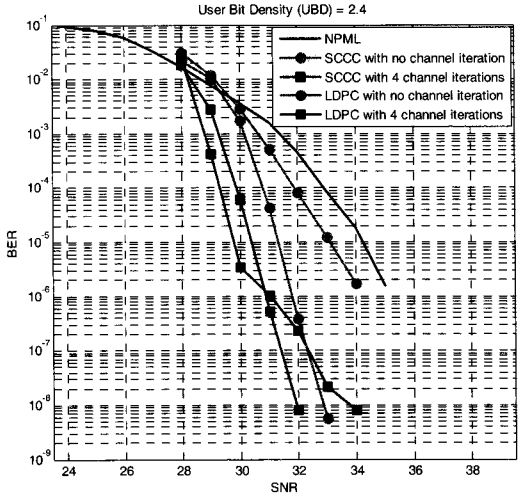

Fig. 9. Simulation results for the LDPC system and SCCC system on PMR in accordance with the number of channel iterations. (UBD=2.4)

and SCCC systems when the UBD is 2.4. The LDPC system performs 2.7dB better than the SCCC system when there is no channel iteration. After four channel iterations, the SCCC system performs better than the LDPC system until 31dB SNR. The two iterative decoding systems, SCCC and LDPC, perform 4dB better than the NPML. The SCCC system without channel iteration performs 0.5dB better than the NPML.

Fourth, BER performances are examined when the UBD is 2.8. Fig. 10 shows the performance of the two systems in accordance with the number of channel iterations applied. Without channel iterations, the LDPC system performs 1.9dB better than the SCCC system. However, after four channel iterations, with a low SNR, the SCCC system performs better than the LDPC system. On the contrary, with a high SNR, the LDPC system performs better than the SCCC system. After four channel iterations, the two iterative decoding systems perform 5dB better than the NPML at 33dB. The SCCC system without channel iteration performs 1.3dB better than the NPML. With a low bit density such as 1.7, the NPML performs better than the SCCC system without channel iterations. However, the SCCC system performs better than the NPML system as the bit density is increased.

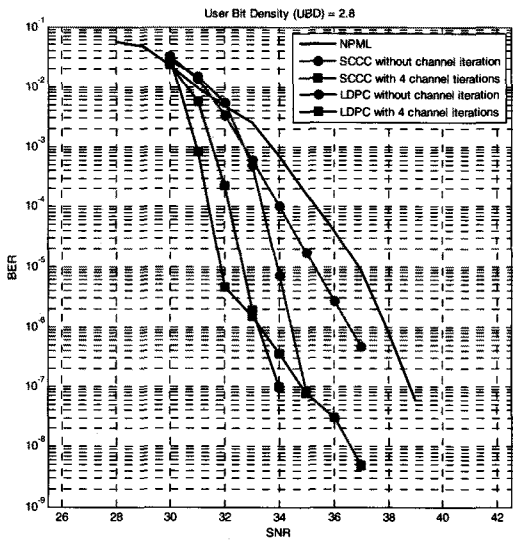

Fig. 10. Simulation results for the LDPC system and SCCC system on PMR in accordance with the number of channel iterations. (UBD=2.8)

V. Conclusion

We have investigated the performances of the SCCC and LDPC systems with different UBDs as the number of channel iterations on the PMR channels. The SCCC system without channel iterations performs better than the NPML when the bit density is increased. When there is no channel iteration, the LDPC system performs better than the SCCC system. However, when there are four channel iterations, the SCCC system performs better than LDPC system until 10^{-6} BER (low SNR region). Therefore, in practice, we can conclude that the SCCC system is a better decoding scheme than the LDPC system because the encoder/decoder for RSC codes is much simpler than the encoder/decoder for LDPC codes. The encoder/decoder for RSC codes consists of some memories and some operators, while the encoder/decoder for LDPC codes consists of many memories, operators and inverse matrix operations, functions. Also the error floor may not cause any problem since the system has to use the outer code (in general, RS codes is used for the outer code in practice) for error free systems.

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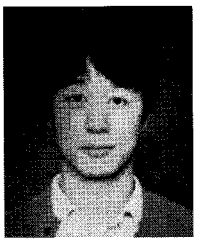

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