DVB-RCS +M 표준기반의 대역확산기술 부호동기기법

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Code synchronization technique for spread spectrum transmission based on DVB-RCS +M standard

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요 약

본 논문은 DVB-RCS +M 표준에서 제안된 직접수열기반의 대역확산기술 중 코드 동기 기술에 관한 것이다. 직접수열기반의 대역확산기술은 다중반송파기반의 대역확산기술에 비해 비선형증폭기의 영향을 덜 받으나 수신단에서 코드 동기 시간 측면에서 불리하다. 이러한 어려움을 개선해보고자 초기 코드 포착을 위한 강인한 상관기 구조가 제안되고 코드 추적을 위한 비동기 DLL(Delay Lock Loop)이 제안된다. 본 기법을 바탕으로 평균 포착 시간 등의 결과를 제시하고 샘플 클럭 타이밍 오차에 영향을 받지 않는 2 오버샘플기반의 코드 추적 회로의 구조와 결과도 제시한다.

키워드 : 유럽형 디지털 비디오 방송 규격- 역방향 위성링크 시스템, 코드 동기, 대역확산, 간섭완화

ABSTRACT

This paper proposes the specific code synchronization technique for DS-SS(Direct Sequence-Spread Spectrum transmission in the DVB-RCS +M standard. DS-SS is better than multi-carrier transmission method under nonlinear channel but imposes a long acquisition time. To improve the synchronization aspect, the robust correlation structure is introduced for acquisition and the nonlinear delay lock loop is done for tracking. MAT(Mean Acquisition Time) performances is shown to validate its superiority. In addition, code tracking and jitter performances are done when code tracking algorithm based on 2 oversamples which is not influenced by sampling clock timing offset and carrier freq. offset is used.

Key Words : DVB-RCS(Digital Video Broadcasting - Return Channel via Satellite), Code synchronization, spread spectrum, Interference Mitigation

Ⅰ. Introduction

The DVB(Digital Video Broadcasting) steering board approved the new study mission to evolve the TM(Technical Module)-RCS(Return Channel via Satellite) standard providing the challenging mobile broadband service in 2006. There is currently an emerging market for provision of broadband services of the nature handled by DVB-RCS to mobile terminals. With demand for mobile broadband interactive service based on DVB-S2/RCS, successful trials and implementation have already been realized using mobile terminals mounted in trains, ship, and aircraft. This is paralleled by the addition of challenging mobility support feature to DVB-RCS.[1][2] DVB-RCS+M is designed for operation in Ku (11-14 GHz) and Ka-band (20-30 GHz). This design choice allows to reuse the existing DVB-RCS and DVB-S2 technologies and to use small antennas,

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thus reducing the deployment and operational costs. However, the critical issue is that specific interference countermeasures are required. The solution devised by the DVB-RCS+M group for interference mitigation is the use of an optional direct sequence spread spectrum (DS-SS) mode for the DVB-S2waveform, with spreading factors up to 16 for the return link single channel per carrier option.

The use of DS-SS in the DVB-S2 waveform means the introduction of a code synchronization subsystem at the receiver side. In this paper, we report the original results of the design and performance assessment of the code synchronization subsystem that have been carried out. It's accomplished jointly with frame acquisition in order to limit the impact on the receiver architecture. As in common practice, the code/frame epoch domain is discretized into a number of cells or hypotheses per chip, and acquisition is achieved through the detection of the spread DVB-S2 Start of Frame (SOF) [2] within the transmission flow. The novelty of the paper lies in robust acquisition subsystem and tracking subsystem. The conventional study has been mainly done in the code acquisition aspect, but in this paper code synchronization has been expanded with code tracking subsystem.

2. System model

Synchronization is the first operation to be performed by a DVB-RCS receiver, and it is achieved by finding the spread Start of Frame (SoF) of the received signal. Thus, despreading and frame synchronization are performed as a whole, taking into account the resulting SoF, which can have different lengths depending on the spreading sequence used. This is accomplished by generating a local replica of the spread SoF code in the receiver and then synchronizing it with the one in the incoming signal. Moreover, since in DVB-RCS communications packet size is of variable length, synchronization has to be achieved at each frame in order to be able to extract the transmission parameters. The knowledge of the transmitted signal timing information is fundamental to receive correctly the signal especially in a Direct Sequence Spread Spectrum (DS-SS) system. In fact, since the spread spectrum sequences used are designed to have small out of phase autocorrelation amplitude, they are very sensitive to erroneous timing estimation. Estimation errors can cause the inability to despread and to demodulate the received signal. Thus code synchronization is essential at the receiver. Synchronization is carried out in two consecutive steps:

- *Acquisition*, which is responsible for an initial coarse timing estimation and synchronizes transmitter and receiver within an uncertainty of half chip ([-0.25, 0.25] T_c) if oversampling equals to two;
- *Tracking*, that performs and maintains fine alignment between transmitter and receiver; obviously the pull-in range must correspond at least to the output uncertainty of the acquisition stage.

Performance of acquisition block has been analyzed in [1], while in the next section tracking strategies are described and performance is assessed. As introduced before, the purpose of tracking is to perform, maintain and improve the synchronization between transmitted and received signal. Given the initial acquisition, the tracking loops keep operating during the whole communication period. If the channel changes abruptly the tracking loops can lose track of the correct timing and re-acquisition is required. Tracking deals with smaller uncertainties than acquisition but it is crucial to reduce timing errors and accomplish correct reception. Tracking devices can be categorized as:

- Open loop (feed-forward loop)
  - Finite observation time;
  - Limited system dynamics can be dealt with during observation time (being based on a open loop estimation, tracking of fast changing parameters is not possible).

- Closed loop (feed-back loop)
  - Infinite observation time;
  - Significant system dynamics can be dealt with during observation time.

- Hybrid systems, that attempt to combine desirable attributes of both open and closed loop estimators.

Since timing parameters change dynamically in time, only closed-loop architectures are considered in this paper.

A generic code synchronization loop is shown below:

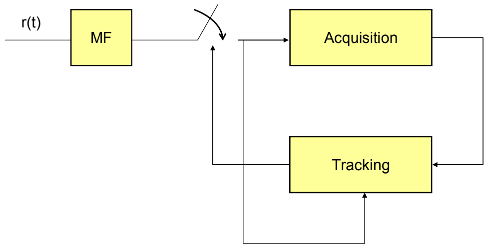


Figure 1. Code Synchronization Loop

In particular the synchronization loop can be expanded into the following scheme described in Figure 2:

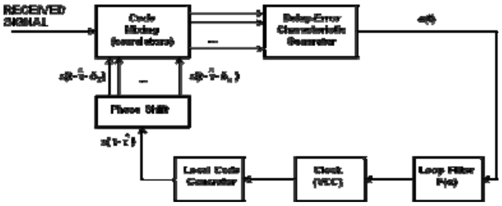


Figure 2. Generic Tracking scheme

The principle of operation of the code tracking loop is that of a standard feedback control system : the incoming waveform, affected by noise is mixed with the locally generated code to produce the waveform e(t). This error signal is used to steer the loop and correct the estimation. The aim of the tracking circuit is to correct the local replica, so that it represents the received signal accurately, and the error signal is null. The code delay error ε(t), given by the difference between the real propagation delay and the local code estimated delay, and the error signal e(t) are linked together by a function called S-curve. The capacity of any code tracking loop to stay in lock, that is to track successfully, is related to the maximum error it can sustain before it loses lock and it is linked to the interval in which the S-curve is non-zero. In this region, in fact, an error in the code phase estimation ε(t) generates a non-zero feedback e(t) which will drive the error towards zero.

It is possible to define two different synchronization strategies based on the inputs of the tracking block. In the first low complexity configuration, the detector designed for the acquisition is used also to perform code tracking, usually with sub optimal performance. The second approach is to design two different detectors, one optimized for acquisition, one for tracking, in order to achieve better performance. In fact, this latter configuration allows usually higher precision since parameters estimation can be achieved after the acquisition block, and the tracking parameters can be optimized accordingly. Note that this solution results in higher complexity since two different correlations have to be performed.

3. Algorithm design

3.1 rationale

DVB-RCS signals are designed with a short spreading sequence (maximum spreading factor 8) and a long scrambling sequence (defined over the entire frame length). The first part of the frame, composed of 26 symbols spread with Spreading Factor SF, is the transmitted preamble, which is identified as SoF. A first tracking estimate can be performed just on the SoF through a data aided strategy exploiting the knowledge of the entire SoF sequence. In the following phase, this estimate is refined through a non data aided algorithm, which can account for the scrambling sequence but not for the data, which are unknown. Note that, since two hypotheses per chip have been considered for the acquisition, synchronous cells can be found also within fractional timing offsets of ±0.5 Tc. This corresponds to a situation in which three H1 cells (synchronous cells) can be found, one with 0 Tc, and two with ±0.5 Tc. Even in the case in which only one of the latter two hypotheses overcomes the threshold, tracking should be able to refine the estimation moving towards the perfect synchronism. Accordingly to the acquisition phase in the following sections the pull-in range of the tracking loop will be designed as [-0.5; +0.5] Tc. In the following some generic tracking schemes are described.

3.2 DLL tracking loop

In literature, over the years, the predominant tracking configuration proposed and analyzed is the Delay Lock Loop (DLL). This tracking circuit can either be operated in coherent or non-coherent mode depending on the system application. Non coherent tracking loops are used in Spread Spectrum communication receivers where code acquisition and tracking are performed prior to carrier synchronization. In DVB-RCS this scheme is used to refine tracking in the presence of unknown data. In this case the acquisition output gives an estimate of the synchronization which can be used to align the spreading and scrambling sequences. For this reason a coherent accumulation over spreading and scrambling can be adopted, while a non coherent DLL is used to avoid the phase uncertainty due to the unknown data. Similarly to the coherent case, an Early-Late scheme approximates the non coherent DLL loop. The simplified non coherent Early-Late circuit, for the case of a real received signal, is shown in the figure below:

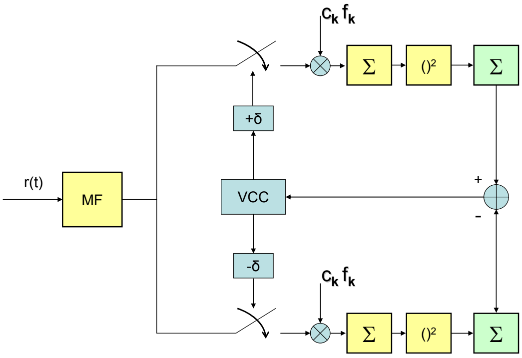


Figure 3. Non Coherent Early-Late Circuit

3.3 Analysis of the Non-Coherent Early Late scheme

Assuming for the sake of simplicity to have a rectangular waveform and consequently a triangular correlation function Rc, an analytical S-curve S(ε,δ) can be generated using the Early-Late scheme as in Figure 3 where is the delay in the received sequence, $\hat{\tau}$ is the delay of the locally generated sequences and δ the normalized Early-Late shift, which is a project parameter and corresponds to a fractional part of T_c. ε represents the code delay error ($\varepsilon = (\tau - \hat{\tau}) / T_c$,T_c=1) . The goal of the tracking mode is to maintain ε at low values.

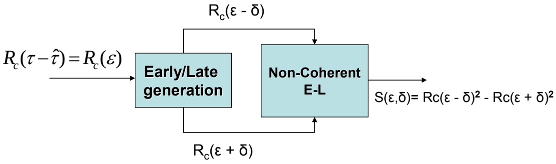


Figure 4. Early -Late S -curve generation

Figure 5 shows three non-linear S-Curve corresponding to three different choices of δ, as δ decreases the slope at the origin increases and provides a stronger feedback for small timing errors.

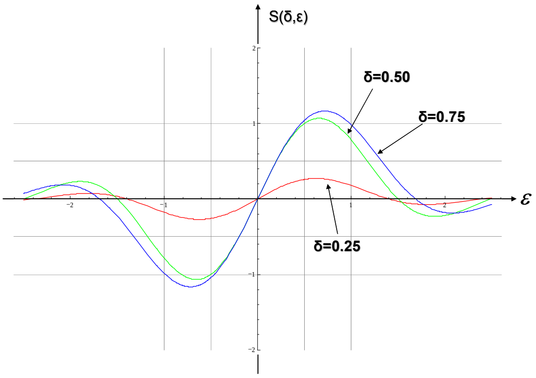


Figure 5. S-curves for different choices of Early-Late shift δ filtered pulses

3.4 Analysis of the Non-Coherent Dot Product

Unlike the classic Non-Coherent Early-Late scheme, the Dot-Product discriminator is not based on the difference of the squared signals but on the multiplication of the Early/Late difference by the prompt signal. Thus all three code replicas of the signal are used. The scheme is shown in Figure 6.

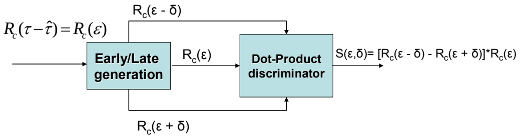


Figure 6. Dot-Product scheme

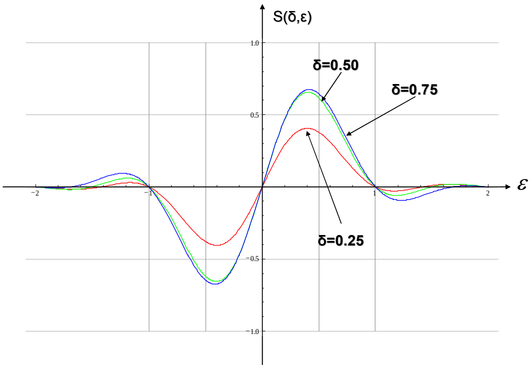
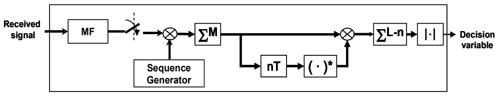


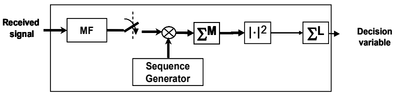
Figure 7. S-curves for different choices of Early-Late shift δ filtered pulses

3.5 Advanced Tracking Techniques

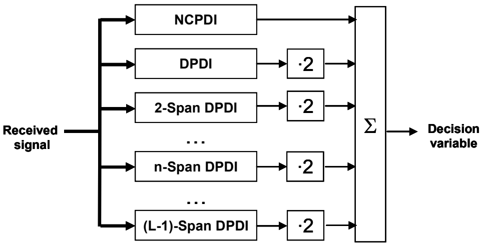
The tracking blocks have to be evaluated taking into account different correlation blocks for acquisition and tracking. Different acquisition strategies have been analyzed in [3][4], with different performance, in different scenarios. Note that the same blocks can be used in the tracking loops instead of the coherent correlation. In the second phase of the project an extension to Post Detection Integration (PDI) discriminators for code tracking will be evaluated. The block diagrams of these schemes have been reported below.



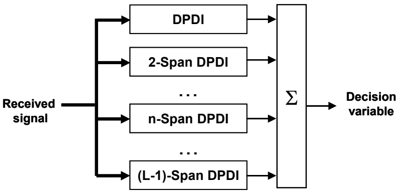
DPDI (n=1)
n-Span DPDI (n>1)



NCPDI



GPDI



D-GPDI

Figure 8. Post Detection Integration detectors block diagrams

4. Performance Evaluation

The following table shows all the parameters that have to be optimized.

Loop Filter Order	1^{st}, 2^{nd}
Loop Filter Gain	γ, β
Integration Type	Non Coherent, Differential, GPDI
Coherent Integration Length	M
Discriminator type	Early Late, Dot Prod
Early Late Spacing	Δ

Table 1. Parameter optimization

The first order loop is fit to track a timing offset, while the second order loop is able to track also a timing drift. The first parameter that has to be optimized is the Loop Filter Gain γ (or γ and β if a second order loop is considered). If a low γ is used (γ = 0.00001) the tracking loop needs too many symbols to obtain a fine timing estimation, while if a high γ is used (γ = 0.0005) the fluctuations around the timing estimate are stronger. A correct compromise is γ = 0.00005, and in the figure 9, this value has been used. The picture 9 shows the tracking loop behavior with different Loop Filter Gain values.

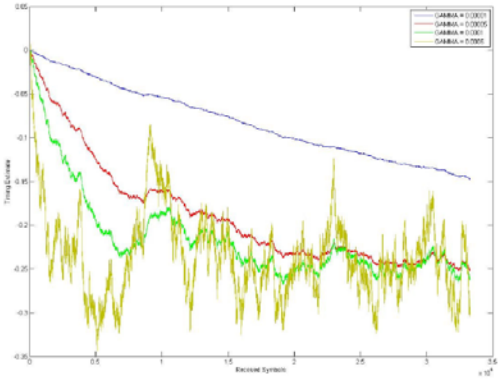


Figure 9. Tracking performance with different loop filter gains

In the following the use of a first order loop and of a second order loop is described. As expected, only the second order loop is able to track a timing drift (in this case of 10 ppm).

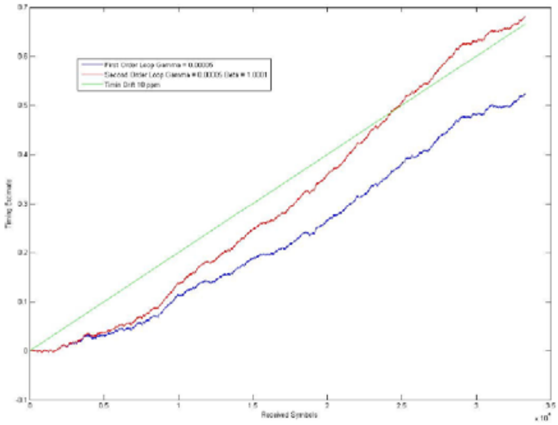


Figure 10. First and Second order tracking loop performance

Figure 11 illustrates the tracking loop performance with different acquisition schemes. Note that the classical Non Coherent scheme (NCPDI) and the differential (DPDI) represent very good trade-offs between complexity and performance.

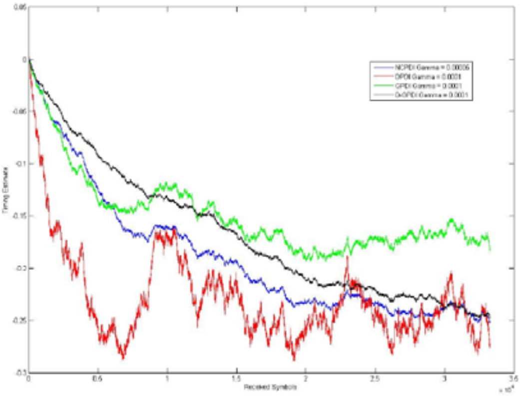


Figure 11. Timing estimate with different acquisition schemes

For DVB-RCS Forward Link, a Non Coherent Tracking Block with coherent correlation length equal to 2 chips, or a Differential block (DPDI with PDI length equal to 2) should be considered to perform the Early Late processing. The presence of the SoF, which is known to the receiver, can not be exploited because of the large frequency error. A Second Order Loop (SOL) should be adopted to track the possible presence of timing drifts.

5. Conclusions

This paper illustrates robust acquisition subsystem and tracking subsystem based on DS-SS system for DVB-RCS +M standard. The conventional study has been mainly done in the code acquisition aspect, but in this paper code synchronization has been expanded with code tracking subsystem. The combination of robust correlator and tracker in the acquisition and tracking mode shows satisfactory performance, respectively. However, note the acquisition time and jitter performances are highly dependent of receiver complexity.

Acknowledgement

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