Analysis of Transport Characteristics for FinFET Using Three Dimension Poisson's Equation

Hak-Kee Jung, Ji-Hyeong Han, *Member, KIMICS*

Abstract — This paper has been presented the transport characteristics of FinFET using the analytical potential model based on the Poisson's equation in subthreshold and threshold region. The threshold voltage is the most important factor of device design since threshold voltage decides ON/OFF of transistor. We have investigated the variations of threshold voltage and drain induced barrier lowing according to the variation of geometry such as the length, width and thickness of channel. The analytical potential model derived from the three dimensional Poisson's equation has been used since the channel electrostatics under threshold and subthreshold region is governed by the Poisson's equation. The appropriate boundary conditions for source/drain and gates has been also used to solve analytically the three dimensional Poisson's equation. Since the model is validated by comparing with the three dimensional numerical simulation, the subthreshold current is derived from this potential model. The threshold voltage is obtained from calculating the front gate bias when the drain current is $10^{-6}A$.

Index Terms— FinFET, Three Dimension Poisson's Equation, Threshold Voltage, DIBL, Doping.

I. INTRODUCTION

THE FinFET structure is one of the MOSFET having the highest potential for the down sizing dimension below 45nm according to the Silicon Roadmap[1]. The scaled-down devices improves the current level in IC, and makes fabrication cost go down. If the channel is scaled down, the performance of MOSFET may be limited and two-dimensional electrostatic effects become important due to short channel effects(SCE). The FinFET has the same limitation as the channel is scaled down. The electrostatic controllability by gate bias has gotton lower due to the increasing charge sharing from source/darin when the channel shrinks down[2]. The SCE such as the threshold voltage roll-off, drain induced barrier lowering(DIBL) and the degradation of the subthreshold swing(SS) and so forth occurs in the scaled down devices. As the results of SCEs, the subthreshold current increases and device performance is degraded.

The compact and accurate models of the carrier transport are needed to increase and make good for use of FinFET in IC. An analytical model for the threshold voltage of mesa-isolated fully depleted ultrathin SOI MOSFET has been reported[3]. This model solves 2D(two dimensional) Poisson's equation analytically using quasi-2D method. It is not adequate to analyze and consider SCEs even if this model considers the narrow width effects. Jeppson's charge sharing model[4] for the analytical threshold voltage model does not include the solution of 3D Poisson's equation even if extending Yau's charge sharing model[5]. The 3D analytical threshold voltage that takes into account the narrow width effect along with SCEs for only bulk MOSFET has been presented[6]. Katti et al. have reported the 3D analytical model for SOI MOSFET to involve the short channel and narrow width effects[7]. The 3D Poisson's equation to obtain analytical potential model for FinFET has been used. Using this analytical potential model, we calculate the transfer relationship of gate voltage and drain current, and obtain the threshold voltage for different values of channel lengths, thickness and width. The FinFET has two bias contact such as front and back bias. The threshold voltage is defined as the front gate bias when drain current is $10^{-6}A$ as the onset of the turn-on condition even though many definitions for the threshold voltage have been reported in the literature[8].

The analytical potential model is explained from analytical 3D Poisson's equation in Sec. II. Since this potential model has been verified comparing with 3D numerical results, the threshold voltage is calculated

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using this potential model for different values of channel lengths, thickness and width in Section III. Concluding remarks are provided in Section IV.

II. ANALYTICAL POTENTIAL MODEL AND TRANSPORT MODEL

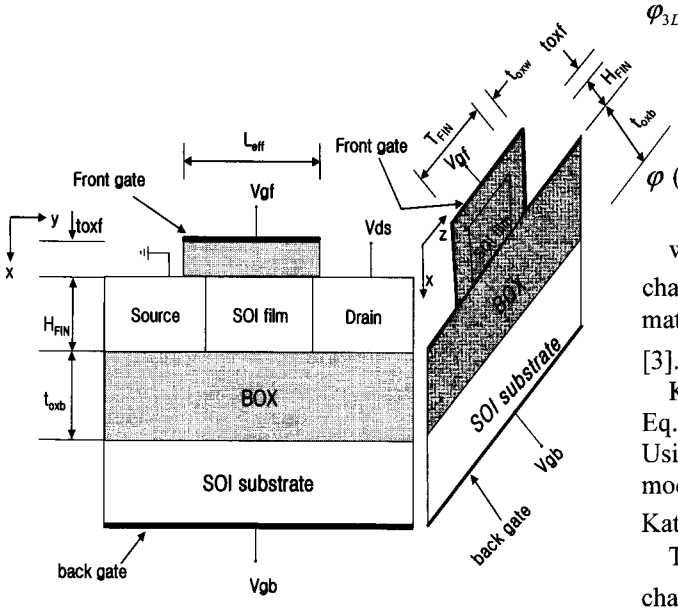

Fig. 1 Cross-sectional view of FinFET along the channel length and along the channel width.

The overview of FinFET is shown in Fig 1 with the coordinate system. To analyze 3D Poisson's equation, Fig.1 shows the cross-sectional view along the channel and width with each notation. The front view is cross section along the channel length of FinFET. The L_{eff} is effective gate length and V_{ds} is source-drain voltage. The T_{fin} is width and H_{fin} is thickness of channel, and t_{oxw} and t_{oxb} are oxide thickness of side and back gate respectively. The V_{gf} and V_{gb} are front and back gate bias. The side view is cross section along the channel width of FinFET. The FinFETs have three gates of front, side and back direction and we can know the potential of side direction is symmetrical.

The complete solution of Poisson's equation is the summation of 1D solution , φ_{1D}, 2D solution, φ_{2D} and 3D solution, φ_{3D}. The channel electrostatics under threshold and subthreshold region is governed by the Poisson's equation with only inversion charge term as follows[3].

$$\varphi_{1D} = \varphi_{sb} + E_{sb}(H_{fin} - x) + \frac{q}{2\varepsilon_{Si}} N_A (H_{fin} - x)^2$$

$$\varphi_{2D} = \sum_{r=1}^{\infty} \frac{1}{\sinh(\gamma_r L_{eff})} [V'_r \sinh(\gamma_r y) + V_r \sinh(\gamma_r (L_{eff} - y))]$$

$$\times [\sin(\gamma_r x) + \frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{oxf} \gamma_r \cos(\gamma_r x)]$$

$$\varphi_{3D} = \sum_{s=1}^{\infty} \sum_{r=1}^{\infty} P_{sr} [\sinh\{\chi_{sr}(T_{fin} - z)\} + \sinh(\chi_{sr} z)]$$

$$\times \frac{\sin(\alpha_s (y - L_{eff}))}{\cos(\alpha_s L_{eff})} [\sin(\beta_r x) + \frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{oxf} \beta_r \cos(\beta_r x)]$$

$$\varphi(x, y, z) = \varphi_{1D} + \varphi_{2D} + \varphi_{3D} \quad (1)$$

where N_A is the doping concentration in the channel and the varibles related with dimension and material such as $\varphi_{sb}, E_{sb}, \gamma_r, P_{sr}, \chi_{sr}, \alpha_s, \beta_r$ refer to [3].

Katti et al. have reported the procedure to solve Eq.(1) with boundary conditions of reference [3]. Using the same procedure, the analytical potential model in the channel $\varphi(x, y, z)$ has been expressed in Katti's model[3].

To calculate the subthreshold current I_{ds}, the channel is now divided into two parts, i.e. front gate region of $0 \le x \le x_{\min}$ and back gate region $x_{\min} \le x \le H_{fin}$, where the potential is the minimum at $x_{\min}$. Thus, the subthreshold current is consisted of front current $I_{ds}^{\ f}$ and back current $I_{ds}^{\ b}$ as following ;

$$I_{ds} = I_{ds}^{\ f} + I_{ds}^{\ b} \quad (2)$$

The potential variation is small along the channel height because of lesser control of the front gate and in the width direction because of the proximity of the two side gates that are at the same potential. The analytical model of I_{ds}^{f} and I_{ds}^{b} is explained in Katti's model[3]. This model is verified as calculating the potential distributions, and the threshold voltage and drain induced barrier lowing to be the representative short channel effects are calculated using our potential model and current analytical model for different values of channel length, width and height in Section III. The threshold voltage is calculated as the front gate bias when drain current is $10^{-6} A$.

III. VERIFICATION OF POTENTIAL MODEL AND GEOMETRY DEPENDENT THRESHOLD VOLTAGE

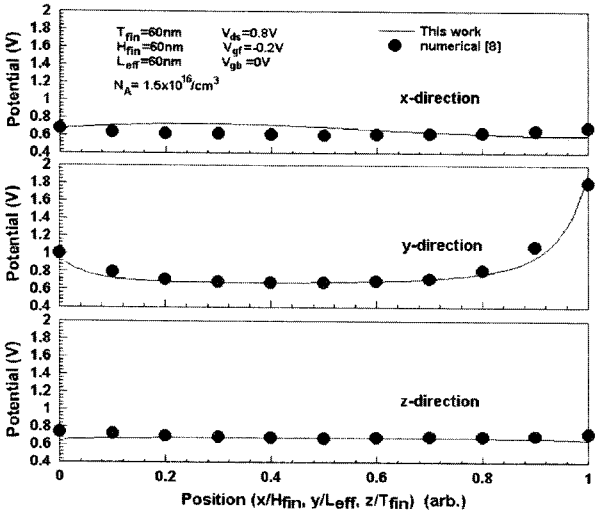

Fig. 2. Potential distribution in the channel for FinFET with doped channel fins

Fig. 2 shows the potential distributions obtained from this model for doped channel FinFET along the channel length for top surface, along the channel width for top surface and the channel height for the center of the top gate. The results of this model have been compared with those of 3D device simulator[8] and we know this model agree with 3D numerical results. The potential along z-direction is symmetrical about $z = T_{fin} / 2$.

Fig. 3 shows the variations of potential along the channel length at $z = T_{fin} / 2$. As shown in Fig.3, the variations of potential in the drain contact is larger than those in source contact. The variation of potential in front gate contact, i.e. in top surface, is varied abruptly, and the bottom of channel is varied slowly. However, the variations of potential in center of channel is nearly constant. We know the influence of front gate bias is more than one of back gate bias. Therefore, the front gate bias is more influenced on current transport phenomena, but the back gate bias has little influence on carrier transport.

As mentioned above, the threshold voltage is defined as the front gate bias when drain current is $10^{-6} A$ as the onset of the turn-on condition. The diffusion component is only included in this model since carrier concentration is low and the drift component of current is trivial in the region of operation. To investigate geometry dependent threshold voltage, we calculate subthreshold current

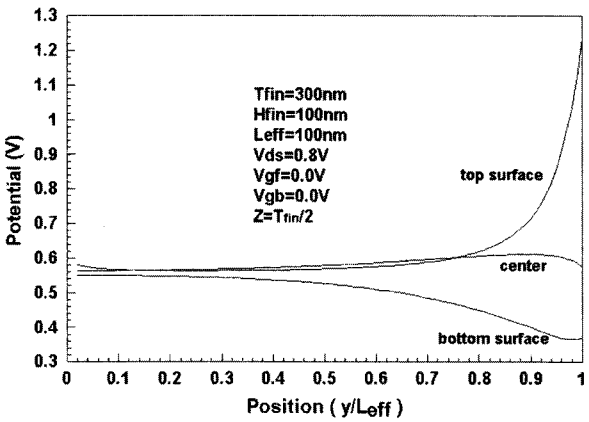

Fig. 3. Potential distribution along the channel length for FinFET to investigate the influence of the top and bottom gate.

using Eq.(2) based on the variation of potential obtained from Eq.(1).

Fig. 4 shows the threshold voltage according to the variation of the channel length, height and width for FinFET. The threshold voltage increases with the increase of channel height since the subthreshold current increases with the decrease of channel height. The threshold voltage decreases with an decrease in H_{fin} due to SCE in lower fins. Fig. 4(b) shows the threshold voltage according to the variation of the channel width for FinFET. The threshold voltage decreases with the increase of channel width since the subthreshold current decreases with the decrease of channel height. The threshold voltage decreases with an increase in T_{fin} due to SCE in thicker fins. Since a decrease in T_{fin} reduces the distance between the two side gates, the control ability of gates over the channel is increased and SCE is decreased. To suppress the SCE, the fin width T_{fin} has to be much smaller than the channel length[9]. In Fig. 4(c), the variation of the threshold voltage with the change in channel length L_{eff} as obtained from this model is plotted. Fig 4(c) shows that the threshold voltage reduces with the reduction in the channel length due to SCE. The subthreshold swing is nearly constant as shown in inlets of Fig. 4(c)

Fig. 5 shows the variations of threshold voltage with channel doping concentration in FinFETs form this model. We know the threshold voltage shifts for doping concentration, and shifts in threshold voltage is larger for high doping of fin. From the undoped case to about $10^{15} / cm^3$, the threshold voltage is nearly constant, but the threshold voltage is abruptly increasing above $10^{15} / cm^3$. If doping concentration

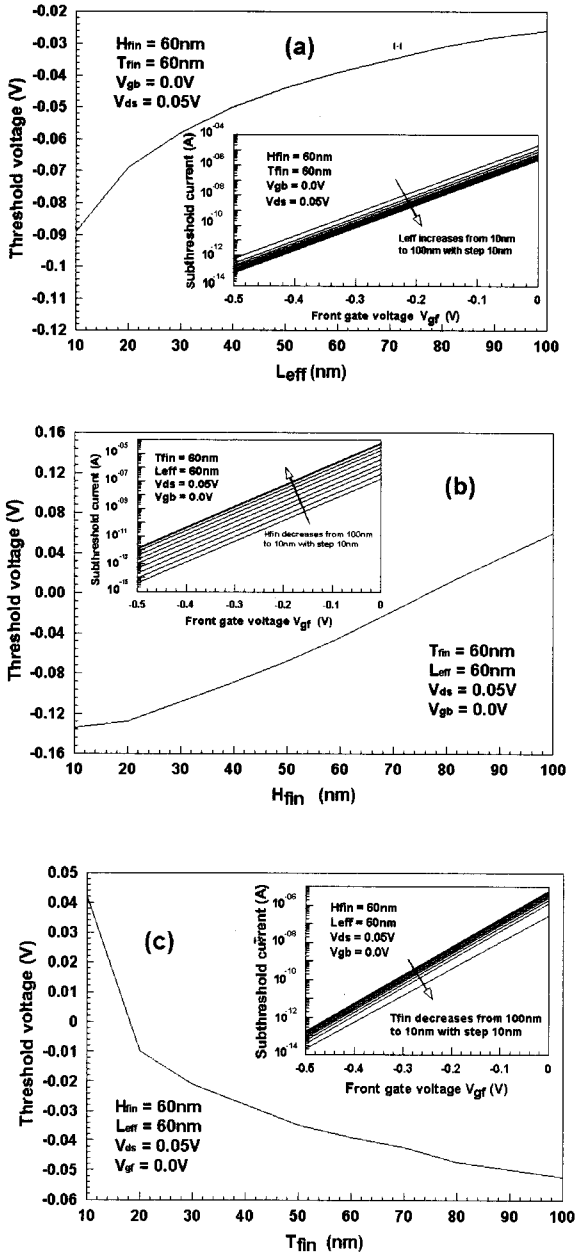

Fig. 4. Threshold voltage according to the variation of the channel length(a), height(b) and width(c) for FinFET with undoped channel fins.

is increased to reduce the short channel effects, the increase in the threshold voltage has been occurred. Therefore optimum doping concentration has to be used to facilitate the performance of FinFET with reduction of short channel effects, specially in the range of high doping concentration.

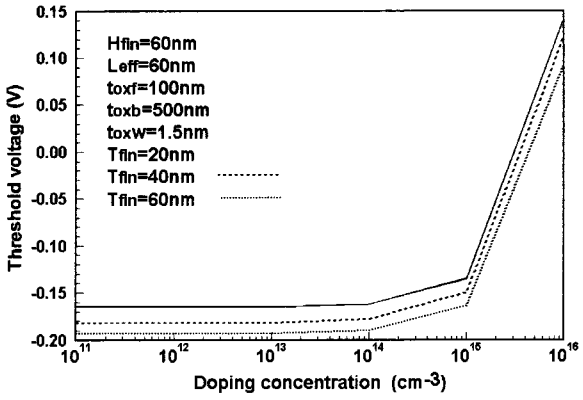

Fig. 5. Threshold voltage according to the variation of doping concentration.

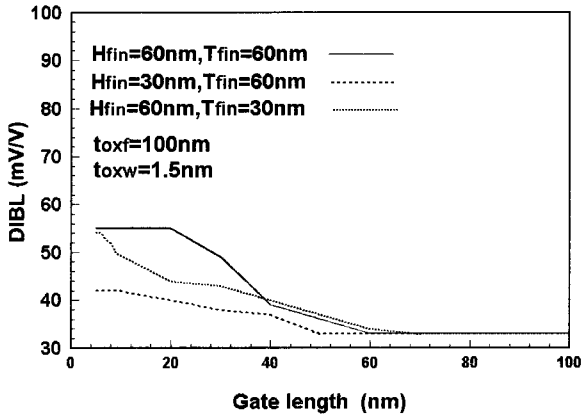

Fig. 6. DIBL according to the variation of the gate length with parameters such as channel height and width.

Fig. 6 shows the drain induced barrier lowing(DIBL) for the variations of gate length with parameter such as channel height and width. The threshold voltage depends on drain bias. This dependence can be express with DIBL to be important for digital application. The threshold voltage becomes a function of the operation voltage due to DIBL. Since the electric field by drain voltage can cause a barrier lowing, the threshold voltage is reduced by the drain voltage. As known in Fig. 6, the DIBL effects is decreased with the increase in gate length, but the DIBL is nearly constant above gate length of 60nm. Below gate length of 60nm, the decreasing degree has been changed with channel height and width. The decreasing rate is reduced with the decrease of channel height and width, and the variation of channel height is more sensitive than one of channel width in DIBL.

IV. CONCLUSIONS

In this paper the threshold voltage of FinFET has has been presented using the analytical potential model based on 3D Poisson's equation. Since the threshold voltage is the most important factor of device design, we have to analyze preciously threshold voltage. To investigate the geometry dependent threshold voltage we obtained the analytical potential model and current model in subthreshold region. The model is validated by comparing with the three dimensional numerical simulation. The subthreshold current is derived from this potential model. Using the model, we have investigated the variations of threshold voltage according to the variation of geometry such as the length, width and thickness of channel. The threshold voltage is obtained from obtaining the front gate bias when the drain current is $10^{-6}A$. We know the threshold voltage increases with the increase of channel height and the threshold voltage decreases with the increase of channel width. Also the threshold voltage reduces with the reduction in the channel length due to SCE. The optimum doping concentration for fin has to be used to facilitate the performance of FinFET. We know the DIBL effects is decreased with the increase in gate length. This model will therefore be available for the analysis of FinFETs and for the circuit design of FinFET.

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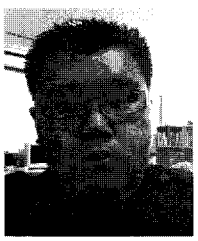

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