Design of a New Harmonic Noise Frequency Filtering Down-Converter in InGaP/GaAs HBT Process

Cong Wang[1] · Jae-Ho Yoon[2] · Nam-Young Kim[1]

Abstract

An InGaP/GaAs MMIC LC VCO designed with Harmonic Noise Frequency Filtering(HNFF) technique is presented. In this VCO, internal inductance is found to lower the phase noise, based on an analytic understanding of phase noise. This VCO directly drives the on-chip double balanced mixer to convert RF carrier to IF frequency through local oscillator. Furthermore, final power performance is improved by output amplifier. This paper presents the design for a 1.721 GHz enhanced LC VCO, high power double balance mixer, and output amplifier that have been designed to optimize low phase noise and high output power. The presented asymmetric inductance tank(AIT) VCO exhibited a phase noise of -133.96 dBc/Hz at 1 MHz offset and a tuning range from 1.46 GHz to 1.721 GHz. In measurement, on-chip down-converter shows a third-order input intercept point(IIP3) of 12.55 dBm, a third-order output intercept point(OIP3) of 21.45 dBm, an RF return loss of −31 dB, and an IF return loss of −26 dB. The RF-IF isolation is −57 dB. Also, a conversion gain is 8.9 dB through output amplifier. The total on-chip down-converter is implanted in 2.56×1.07 mm^2 of chip area.

Key words : Asymmetric Inductance Tank Structure, Double Balanced Mixer, Phase Noise, Voltage Controlled Oscillator.

Ⅰ. Introduction

Through the tremendous growth of wireless handheld devices, high performanceis a major consideration in monolithic microwave integrated circuit(MMIC) designs. This paper explores high performance on-chip down-converter MMIC design for HBT voltage controlled oscillator(VCO) and mixer co-design through their applications in an RF front-end transceiver.

Integrated VCOs are important blocks in communication systems. They are used in virtually all types of up-conversion, down-conversion, frequency modulation, and high frequency generation systems. While most VCOs are designed to generate a sinusoidal voltage waveform, their use and required performance vary widely[1]. An integrated circuit reduces the size of the devices such as on-chip inductors and capacitors; thereby it can improve the spectral purity of VCO. Also, the varactor diode whichis used for frequency tuning of VCO can also be realized on the same chip. A further advantage is that $1/f$ noise is reduced by using ledge function of HBT process[2]. Many VCOs constructed with InGaP/GaAs HBT technology have been developed to achieve the characteristics of low power consumption, low phase noise, and high operation frequency[3]~[5].

In this paper, the uses of AIT structure, high quality tank, and HNFF technique are described and aided design of the proposed VCO. To improve the phase noise performance of integrated LC VCO, the core structure of the VCO is based on a cross-coupled differential configuration. This topology has been widely adapted in low gigahertz regimes due to its simplicity and differential operation. One advantage of this architecture is its high loop gain, which makes it a popular solution for differential VCO designs in RFIC/MMIC.

The frequency conversion process is necessary for the quality of the signal, as well as the wider communication area using a small antenna. Therefore, the mixer is a critical block for this process to perform the frequency translation. The most important elements to consider in the mixer design are high gain, low noise, and low power consumption.

The main topology of the proposed mixer is double balanced Gilbert cell topology. This topology is a fundamental building block, which is used in a wide array of IC applications, including modulators, de-modulators, and RF mixers. This RF mixer can produce positive conversion gain and multi-decade bandwidthoperation. It requires low local oscillator(LO) power and is compact in size. Furthermore, its base-band and multi-decade bandwidth performance make it attractive for the wideband instrumentation and RF communications[6]. Recently, active Gilbert cell mixers with high conversion gain have been reported[7],[8].

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In section II, the down-converter including proposed asymmetrical inductance tank structure VCO, high power double-balanced mixer, and output amplifier are presented. Section III describes measurement results of the down-converter from the fabricated device. Finally, section Ⅳ draws conclusions from these results.

Ⅱ. Enhanced LC VCO and Mixer Co-Design

2-1 Asymmetrical Inductance Tank(AIT) Structure with High Quality Factor

The presented VCO consists of an LC tank, a pair of emitter follower buffers, and a negative resistance block. A cross-coupled differential structure with capacitive coupling feedback is used to reduce the $1/f$ noise. To realize a high quality factor, the core of the VCO with AIT and symmetrical(SIT) structure will be concerned which is shown in Fig. 1(a) and (b), respectively.

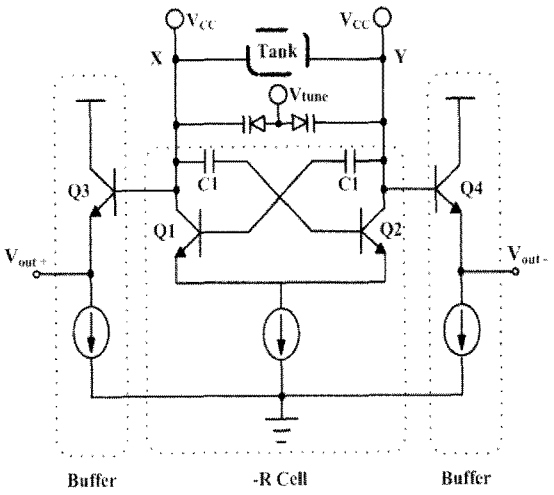
To obtain low phase noise performance, the high Q resonator is optimized; this is one of the most important aspects of oscillator design[9]. As we know, the quality factor can be expressed as the phase of the open-loop transfer function $\Phi(\omega)$ at the resonance of the LC tank in an oscillator

$$Q = \frac{\omega_0}{2}\left|\frac{d\phi}{d\omega}\right|_{\omega=\omega_0} = \frac{R_{\tan k}}{\omega_0 L} \tag{1}$$

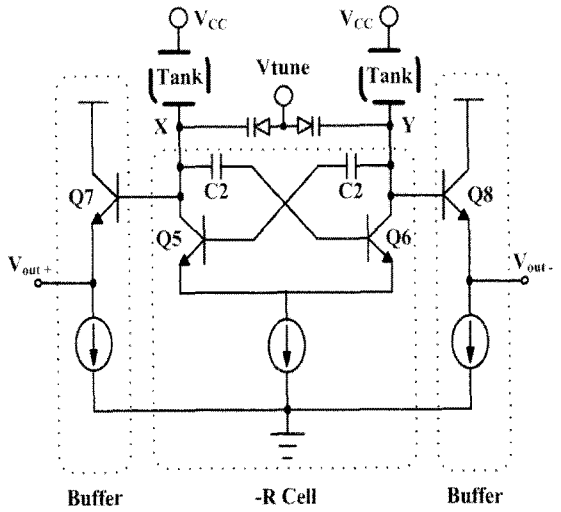
where R_{tank} is the LC tank resistance at the resonant frequency(ω_o), and L is the inductance of the tank. In InGaP/GaAs technology, the resistance of R_{tank} is inversely proportional to the area of inductor.

If the asymmetrical inductor is used in tank, the R_{tank} will be two times better than the symmetrical tank. L depends on the center carrier frequency; therefore it will be almost the same in both the AIT and the SIT. To acquire a high Q value, inductors with low parasitic series resistance are chosen because these inductors have high Q values and provide low phase noise in the oscillator. To this end, the Q-factor of the AIT is definitely superior to the Q-factor of the SIT(shown in Fig. 2), due to a reduction in parasitic resistance. Fig. 3 shows a comparison of the phase noise simulation performance as a function of offset frequency between the AIT and the SIT. The most important point to note here is that the phase noise of the AIT-VCO is greater than 3.4 dB at 1 MHz offset than SIT-VCO. As a result, the AIT structure can be optimized with high R_{tank}, voltage swing, and Q factor when compared with the SIT.

Using the AIT, the wave shape of the core stage has a little distortion in the headroom, which came from the



(a) Asymmetrical inductance tank structure(AIT)



(b) Symmetrical inductance tank structure(SIT)

Fig. 1. Brief circuits of the LC VCOs.

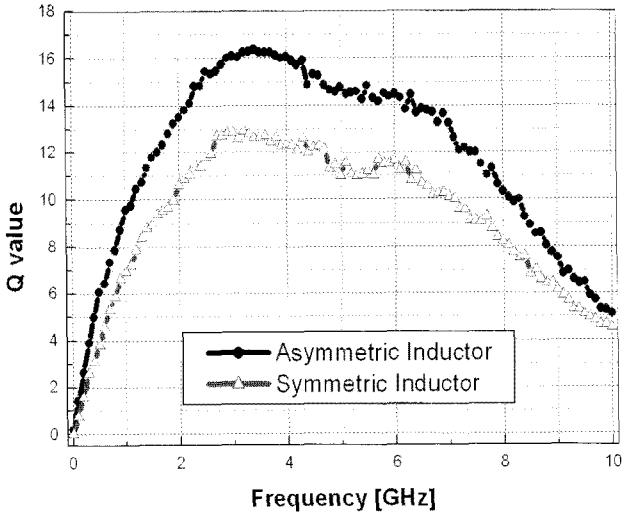


Fig. 2. Q value of the asymmetrical and symmetrical inductors.

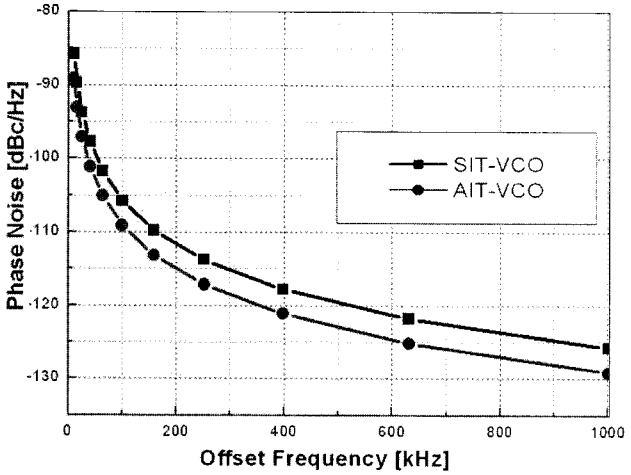


Fig. 3. Phase noise simulation result of the AIT-VCO and SIT-VCO.

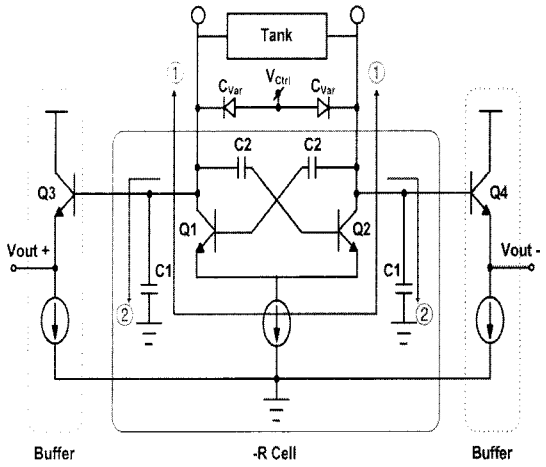


Fig. 4. Schematic circuit of the differential LC VCO using HNFF technique.

asymmetric capacitor in the resonator part. It can be eliminated with symmetric capacitance in the AIT. Generally, the Q value of the tank should be maximized, and the noise generated by the transistor should be as small as possible. In addition, the tank energy should be maximized, leading to a minimization of the tank inductance. All these criteria are taken into account when designing the VCO.

2-2 Harmonic Noise Frequency Filtering(HNFF) Technique

The VCO includes a feedback oscillation signal path and a frequency control path. The phase noise of the oscillator is primarily generated by these two paths, into which the noise is injected. This paper treats the phase noise reduction in these paths using the proposed HNFF technique.

Fig. 4 shows the proposed HNFF structure with cross-coupled negative resistance cell and a buffer. In many integrated transceiver designs, the buffer drives an internal capacitive load(C_L). When C_1 is added, the total capacitance of the load is decreased; superior low phase noise performance is obtained because the harmonic noise is filtered. From Leeson's equation(2), we have

$$\left|\frac{Y}{X}(j\omega)\right|^2 = \frac{1}{4Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{2}$$

where X, Y stands for the input and output function of the feedback circuit, ω_0 is the carrier frequency, Q is the quality factor of the tank, and $\Delta\omega$ is the offset frequency relative to the carrier. This expression reveals the dependence of the output noise upon the Q factor of the tank, the center frequency, and the offset frequency.

As the Q factor of the tank increases, the performance improves in three ways: (a) the noise shaping function, equation (2), becomes sharper; (b) the power dissipation decreases; and (c) the noise injected by active devices decreases.

This improves the phase noise performance, reducing the noise factor of the circuit. In Fig. 4, arrow (1) shows the flow of the odd harmonics in the loop. Before the odd harmonics flow out of the output buffer, the noise frequencies of the odd harmonics short to ground through arrow (2). Fig. 5 shows the phase noise variation as a function of control voltage with and without HNFF technique. Therefore HNFF technique can be adapted to reduce phase noise as shown in Fig. 5.

The capacitor C_1 is chosen to lower the noise fre-

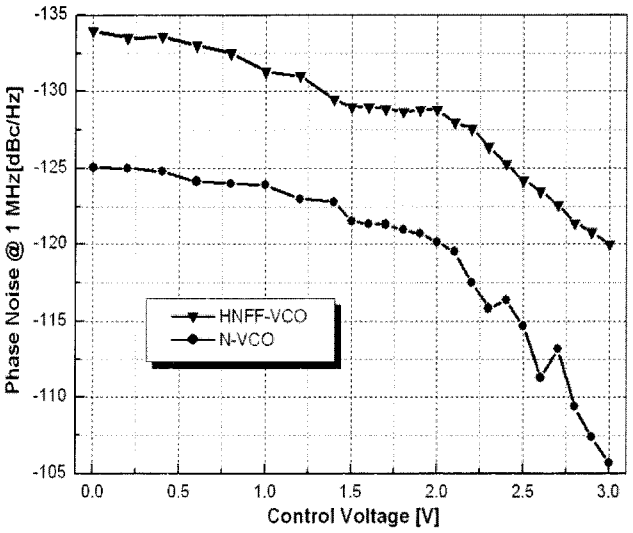


Fig. 5. Phase noise reduction with increasing VCO control voltage.

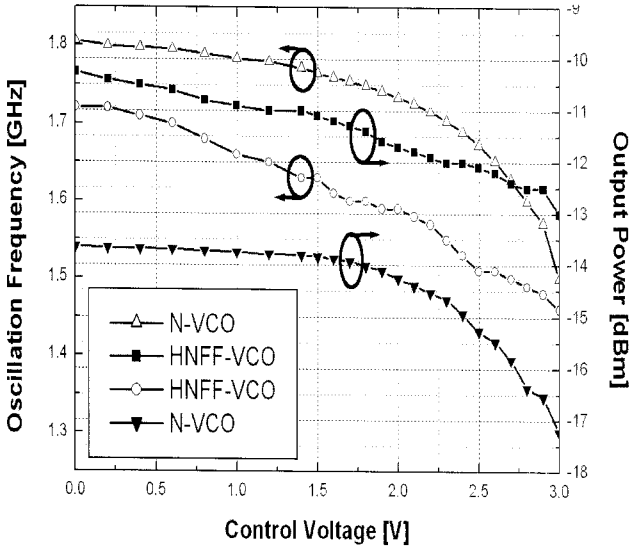


Fig. 6. Variation of oscillation frequency and output power as a function of tuning voltage.

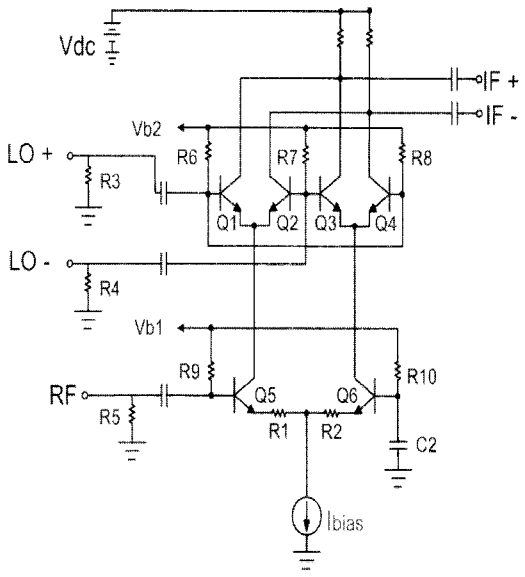


Fig. 7. Schematic of the DBM core.

quency in parallel with whatever capacitance is present at the feedback source of the differential pair as shown in Fig. 4. To acquire a high Q tank, the capacitance of the resonator must be higher than the inductance. Therefore, an inductor with a low parasitic series resistance is chosen because the Q factor of the LC tank circuit is dominated by phase noise. But the total capacitance of the load is decreased with adding capacitor C_1, hence the frequency tuning range is made narrower[10]. Fig. 6 shows the oscillation frequency and output power variation as a function of tuning voltage with and without C_1. A wide tuning range is often important because it can accommodate more process and temperature variations. In order to extend the tuning range, two pairs of base-collector(BC) diode would be used in the case of tank structure.

2-3 Design of High Power Double Balance Mixer

The double-balanced mixer(DBM) utilizes a Gilbert cell core in this paper because of its low DC power consumption, high linearity, and good spurious output rejection. Also, it can provide a high gain and very low noise figure. Strict symmetry is maintained for the balanced structure to minimize the amplitude and phase errors. Fig. 7 shows the schematic of the designed high power double balanced mixer.

The circuit is designed in such a way that the transistor in the LO input part acts as a switch(Q_1, Q_2, Q_3, and Q_4) and can be operated in the cutoff area by applying minimum bias. The bias points of Q_5 and Q_6 are in the saturation region and those of Q_1-Q_4 are within a linear region. Besides, C_2 is signal path for the balanced input signal. By itself, the RF input differential pair is not linear enough for useful applications, so it must be linearized. A common technique to achieve this is known as resistive degeneration using resistors R_1 and R_2[11],[12]. Furthermore, linearity is improved by inserting a broadband resistor(R_5) at the RF port, but it increases the noise figure. Both the LO differential input ports have on-chip broadband 50 ohm resistive terminations (R_3 and R_4), resulting in excellent broadband return losses and superior inter-modulation performance.

2-4 Co-design of the VCO and Mixer

Fig. 8 shows a complete schematic of the integrated VCO and mixer co-design consisting of the VCO, mixer, and output buffer. The output buffer is a cascode differential pair with inductive emitter degeneration represented by L_1 and L_2. This configuration is chosen to reduce the Miller capacitance and increase the power gain. Off-chip pull-up inductors(L_3 and L_4) enable a high output voltage swing. AC coupling capacitors(C_1) help to improve the power matching to 50 Ohm. L_1 and C_2 are IF matching part.

Ⅲ. Measurement Results

A microphotograph of the fabricated VCO and mixer co-design with a die size of 2.56×1.07 mm^2 is depicted in Fig. 9. They are fabricated using a commercial InGaP/GaAs HBT process in which the HBT devices have a cutoff frequency(f_T) of 48 GHz and a maximum oscillation frequency(f_{MAX}) of 80 GHz.

From Fig. 10, phase noise of the measured enhanced

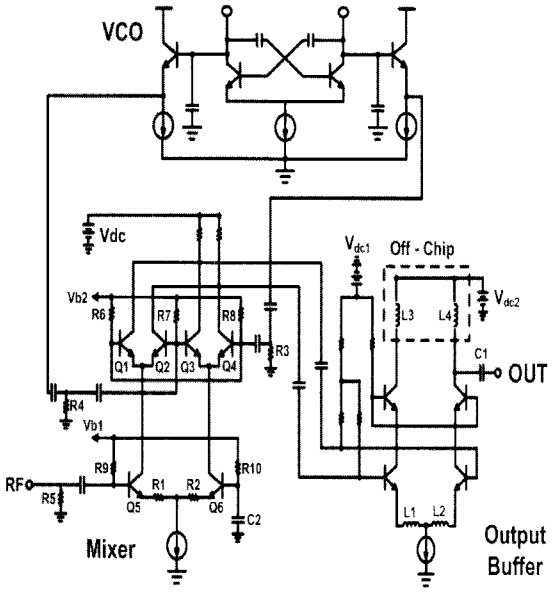


Fig. 8. Schematic of the VCO and mixer co-design.

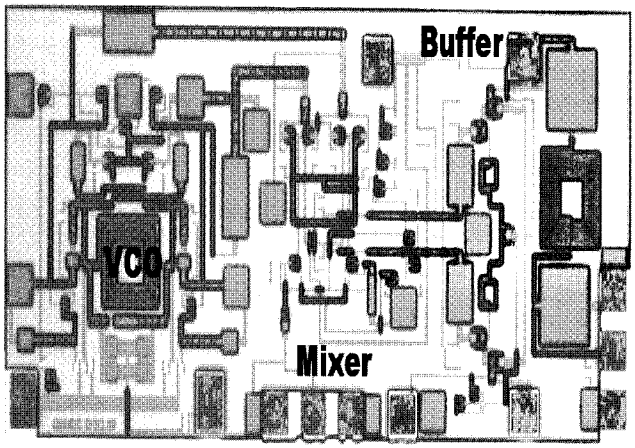


Fig. 9. Microphotograph of the enhanced LC VCO and high power double balanced mixer co-design.

LC VCO is −133.96 dBc/Hz at an offset frequency of 1 MHz. Using the HNFF capacitors produces low phase noise performance since the noise in both the feedback oscillation signal path and the frequency control path is reduced. This is also due to an increase in the parasitic capacitance and the Q factor of the tank. Therefore, the HNFF structure shows low phase noise performance.

A widely used figure-of-merit(FOM) is defined[13] as

$$FOM = L(\Delta f_m) - 20\log\left(\frac{f_0}{f_m}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right) \quad (3)$$

In this work, we achieve FOMs of −181.3 dBc/Hz. It shows an excellent performance compared to the other VCOs in different frequencies and power dissipations.

Fig. 11 shows that the return loss of the RF port is

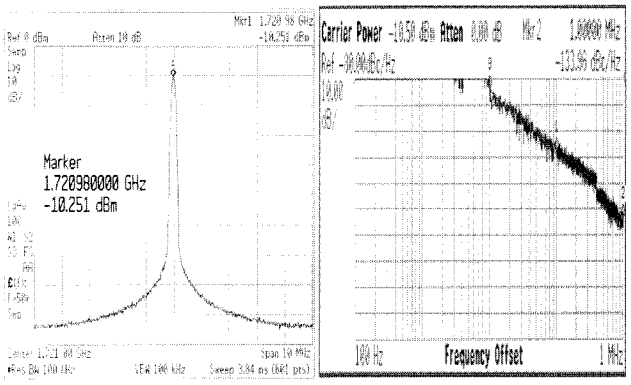


Fig. 10. Phase noise and output spectrum of the VCO measured at the lowest tuning voltage.

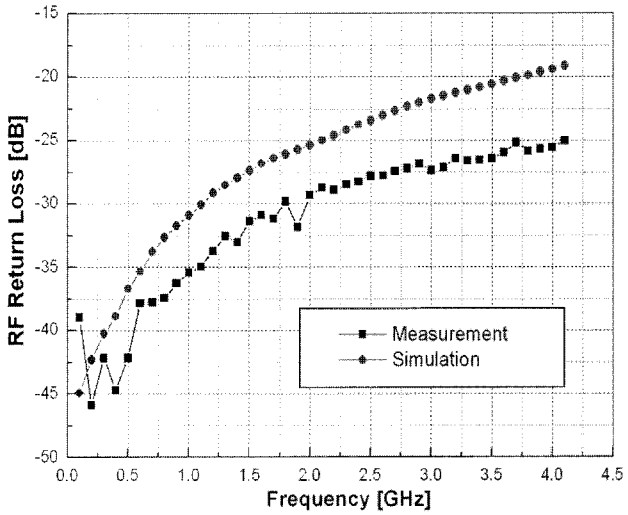


Fig. 11. Simulation and measurement results of RF return loss.

under −20 dB in the frequency range of 400 MHz to 3.5 GHz and −31 dB at the center frequency. Return loss of IF port is about −26 dB. Simulation and measurement results of IF return loss are shown in Fig. 12. Also, the leakage of the RF-to-IF ports measured at −30 dBm(RF power) is −57 dB. To measure the inter-modulation effect, the third order inter-modulation, two signals with a 1 MHz offset are applied to the input port of the mixer. Fig. 13 shows that when the applied input power is −10 dBm, then the IMD3 is 45.071 dBc. The measurement results of the one tone test are shown in Fig. 14. The conversion gain is about +8.9 dB to compensate cable loss at an RF power level of −30 dBm and a LO power level of −10 dBm. The input- referred third order intercept point(IIP3) and the output- referred third order intercept point(OIP3) are calculated by using these results. So, IIP3 is found to be +12.55 dBm and OIP3 is +21.45 dBm. Fig. 15 shows an IIP3 and OIP3 point.

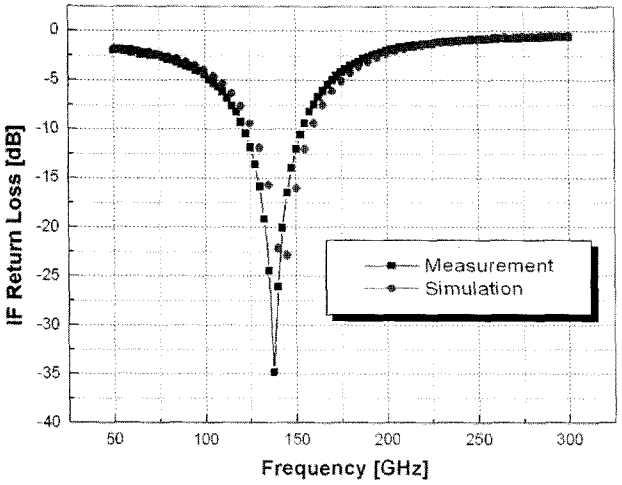


Fig. 12. Simulation and measurement results of IF return loss.

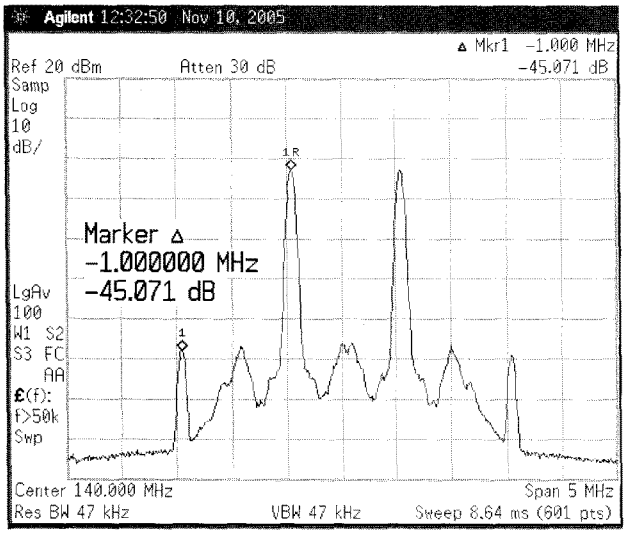


Fig. 13. The characteristics of measured IMD3(RF power: −10 dBm, LO power: −10 dBm).

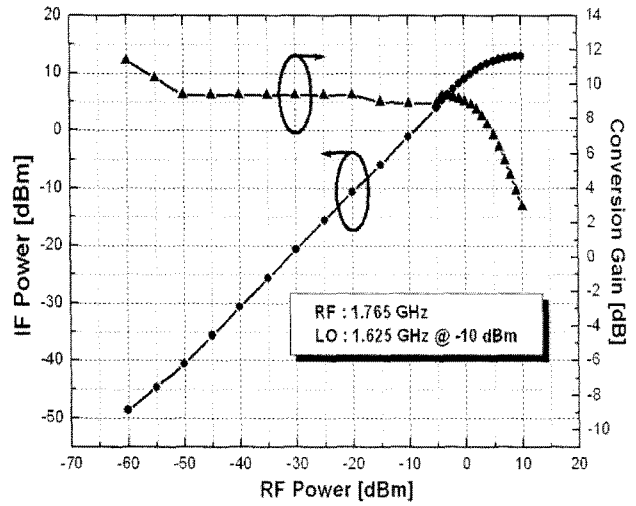


Fig. 14. Measured P1dB compression point.

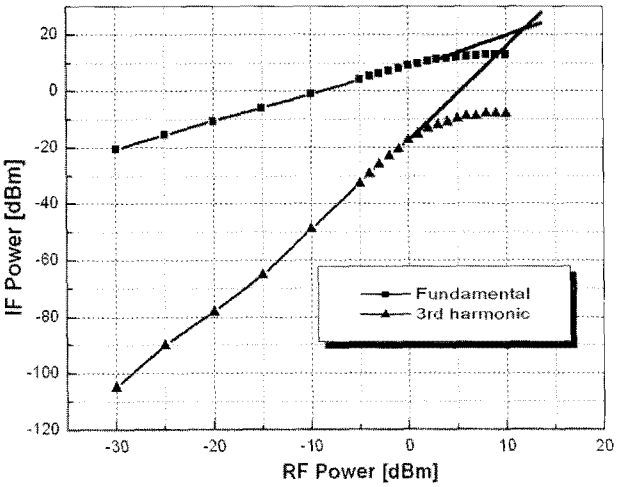


Fig. 15. Fundamental and 3rd harmonic power versus RF power of two tone test.

Ⅳ. Conclusion

LC tuned VCO and down-conversion mixer are two major building blocks of a high frequency radio front-end receiver. In this paper, both circuits have been examined and designed to combine each module for down-converter SoC applications.

The VCO has superior phase noise performance due to the HNFF technique and AIT structure. Also the designed mixer has an output buffer with cascode configuration using pull-up inductors. In conclusion, the successfully superior operation of the co-designed enhanced LC VCO and mixer shows the appropriateness of the proposed design technique.

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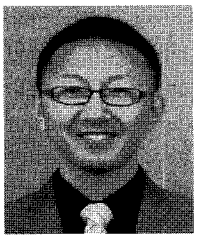

He was born in Qingdao, China in 1982. He received the B.S. degree in Automation Engineering from Qingdao Technological University in 2005, and the M.S. degree in Electronic Engineering from Kwangwoon University in 2008. He is currently studying for a Ph.D. in the same university. His current research mainly focuses on RFIC/MMIC active and passive circuit design and semiconductor manufacturing process optimization.

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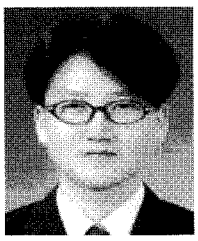

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