Effects of Drain Bias on Memory-Compensated Analog Predistortion Power Amplifier for WCDMA Repeater Applications

Yong-Sub Lee[1] · Mun-Woo Lee[1] · Sang-Ho Kam[1] · Yoon-Ha Jeong[1,2]

Abstract

This paper represents the effects of drain bias on the linearity and efficiency of an analog pre-distortion power amplifier(PA) for wideband code division multiple access(WCDMA) repeater applications. For verification, an analog predistorter(APD) with three-branch nonlinear paths for memory-effect compensation is implemented and a class-AB PA is fabricated using a 30-W Si LDMOS. From the measured results, at an average output power of 33 dBm(10-dB back-off power), the PA with APD shows the adjacent channel leakage ratio(ACLR, ±5 MHz offset) of below −45.1 dBc, with a drain efficiency of 24 % at the drain bias voltage(V_{DD}) of 18 V. This compared an ACLR of −36.7 dBc and drain efficiency of 14.1 % at the V_{DD} of 28 V for a PA without APD.

Key words : Analog Predistorter(APD), Bias, Efficiency, Memory Effect, Power Amplifier(PA).

Ⅰ. Introduction

Power amplifiers(PAs) should operate at a large back-off power(BOP) in order to produce the proper linearity, because modulated signals in modern communication systems have high peak-to-average power ratios(PAPRs). Therefore, efficiency is degraded, primarily due to thermal problems. To improve the efficiency at a large BOP, a number of techniques have now been developed. These can be classified into three types, as follow:

Ⅰ. Switching-mode power amplifiers such as class-E, -F, -F^{-1}, etc[1]~[3].

Ⅱ. Load modulation, such as Doherty amplifiers, etc[4]~[6].

Ⅲ. Bias modulation, such as envelope tracking(ET), envelope elimination and restoration(EER), etc[7],[8].

The first type results in an extremely poor linearity, in spite of its moderate efficiency enhancement. The second method can theoretically provide peak efficiency at a large BOP by constructing two or more devices in parallel and delivers acceptable linearity using G_{m3} cancellation. The last type improves the efficiency by reducing the power consumption with the control of bias voltages, according to the envelope of the instantaneous signal. However, the linearity degradation resulting from bias modulation also should be considered. Therefore, powerful linearization techniques, such as analog(APD) or digital predistorters(DPD), should be carefully employed to these three efficiency-boosting types for linearity improvement, while preserving the enhanced efficiency at a large BOP[9]~[12].

In this paper, we investigate the effects of drain bias on the linearity and efficiency of the analog predistortion PA for wideband code division multiple access (WCDMA) repeater applications. For experimental validations, an APD with three-branch nonlinear paths for the memory-effect compensation is implemented and the class-AB PA is fabricated with a 30-W Si LDMOSFET. The measured results prove that the analog predistortion PA with drain bias modulation can improve the linearity and efficiency over that seen with the PA without APD.

Ⅱ. Drain Bias Effects on Memory-Compensated Analog Predistortion Power Amplifier

2-1 Limited Performance of CAPD

For the conventional APD, it is very difficult to achieve a significant cancellation of the distortion components of the PA, since the PA shows asymmetry between the lower and upper bands, due to memory effects for wideband signals. Fig. 1(a) shows the block diagram of the conventional APD(CAPD). Fig. 1(b) shows the limited performance of the CAPD in linearizing the PA with memory effects for a wideband modulated signal. In the nonlinear path of the CAPD, a diode-based error generator produces a symmetrical distortion signal. The amplitudes and phases in the lower and upper bands are concomitantly controlled by the vector modulator. However, since the PA shows asymmetry between the lower and upper bands, due to memory effects for wideband signals, it is very difficult for the CAPD to significantly cancel the distortion components of the PA in the symme-

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trical states. Therefore, the CAPD with memory-effect compensation should be applied to the PA with memory effects.

2-2 Memory-Compensated MBAPD

To compensate for memory effects of the PA by adding additional nonlinear paths to the conventional APD, we have developed a multi-branch APD(MBAPD) with various delay differences($\Delta\tau$), which further improves the linearity. Fig. 2 shows the simple block diagram of the MBAPD, which consists of a linear path and a multi-branch nonlinear path. The linear path is comprised of the main delay line(τ_L). The multi-branch nonlinear path has a nonlinear function of $E_N(\cdot)$ and various delay lines with different $\Delta\tau$ connected in parallel, which constitutes the memory-compensating part. The τ_L is delay-matched with the main delay in the nonlinear path(τ_N).

The $E_N(\cdot)$ transforms the wideband input signal of $V_I(t)$ into a memoryless nonlinear signal of $E_N[V_I(t)]$, which passes through nonlinear paths with various delays. The total predistorted signal of $V_P(t)$ contains the instantaneous, high-order, and past input signals. Finally, the $V_P(t)$ are used to compensate for memory effects of the PA. The total output signals of the MBAPD of $V_T(t)$ can be expressed as

$$\begin{aligned} V_T(t) &= V_L(t)+V_P(t) \\ &= V_I(t-\tau_L)+\sum_{m=-n}^{n} V_{N(m)}(t) \\ &= V_I(t-\tau_L)+\sum_{m=-n}^{n} E_N[V_I(t-\tau_N-m\cdot\Delta\tau)] \end{aligned} \quad (1)$$

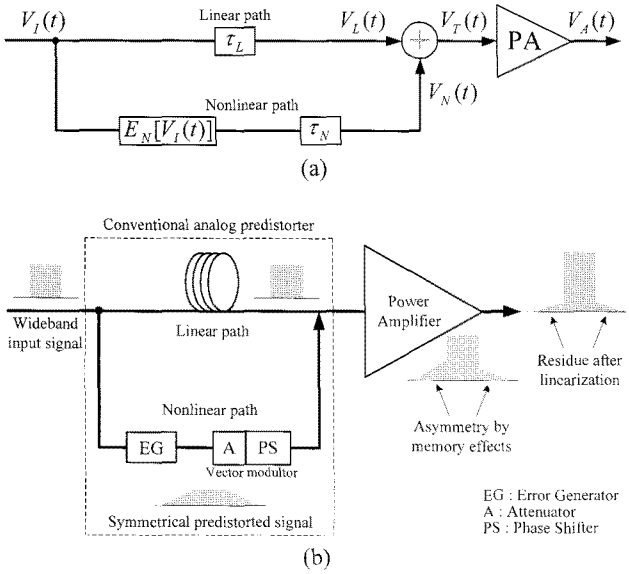


Fig. 1. (a) Block diagram and (b) limitation of the linearity improvement of the CAPD.

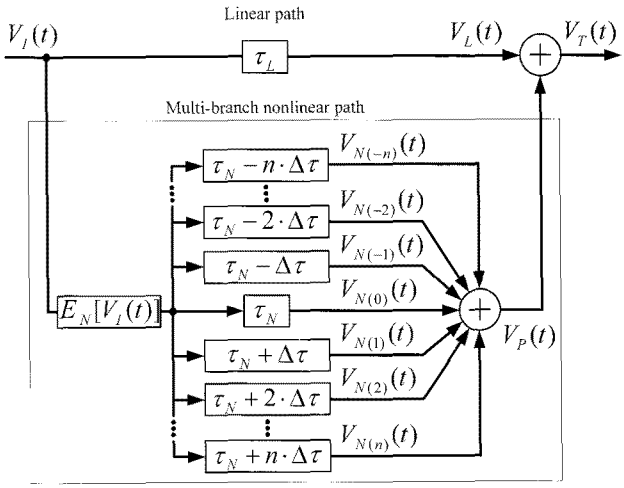


Fig. 2. Block diagrams of the MBAPD.

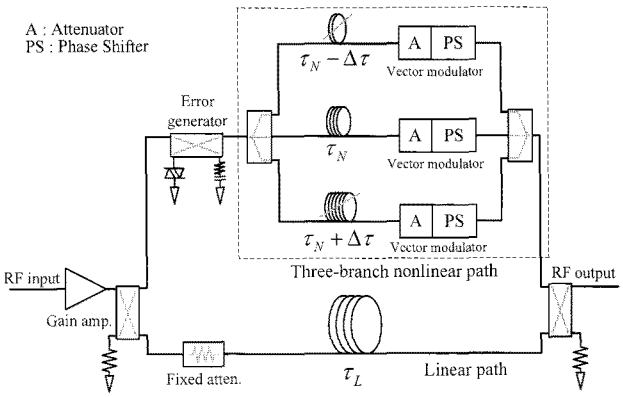


Fig. 3. Schematic of the proposed MBAPD with a three-branch nonlinear path.

where $V_L(t)$ and $V_N(t)$ are the modulated signal after the linear path and each predistorted signal after different delay lines in the nonlinear path, respectively. Although the $E_N(\cdot)$ in the nonlinear path produces the memoryless signal of $E_N[V_I(t)]$, the MBAPD with various $\Delta\tau$ compensates for memory effects as well as for memoryless nonlinearity of the PA since the $E_N[V_I(t)]$ is transformed by various $\Delta\tau$ and summed into the $V_P(t)$ with memory characteristics. Therefore, the linearity can be improved by controlling $\Delta\tau$ and a number of additional nonlinear paths of n, according to the signal bandwidth of modulated signal and the memory-effect quantity of the PA[13].

2-3 Drain Bias Effects on an Analog Predistortion Power Amplifier

Fig. 4 shows the block diagram of the PA with MBAPD. The PA has a different output power, gain, and effi-

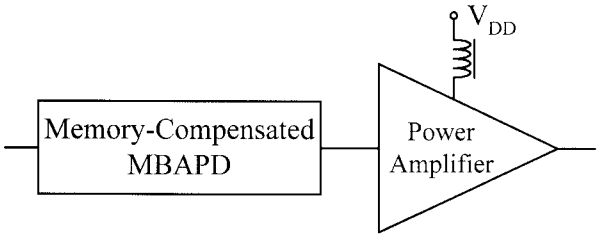


Fig. 4. Block diagram of the PA with MBAPD.

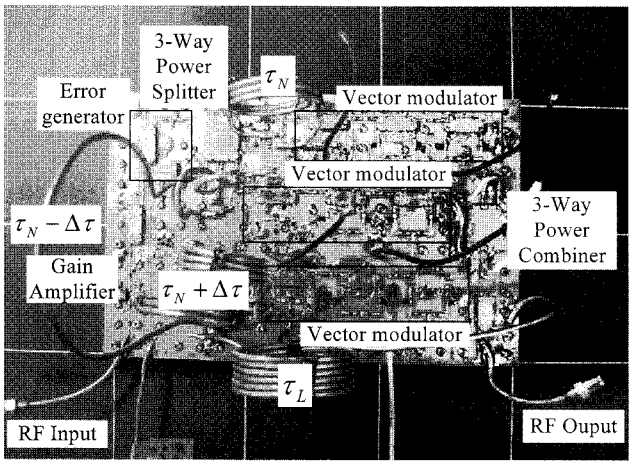


Fig. 5. Photograph of the fabricated MBAPD with three-branch nonlinear path.

ciency when the drain bias voltage changes. Additionally, the nonlinear characteristics of the PA are varied according to drain bias. Therefore, the MBAPD should be optimized at each drain bias. However, it is clear that the linearity improvement of the MBAPD decreases but the efficiency increases because the saturation power is decreased by the reduced drain bias voltage.

Ⅲ. Implementation and Experimental Results

The MBAPD with a three-branch nonlinear path was designed as shown in Fig. 3. The two additional nonlinear paths are shorter and longer in delay than the τ_N and are used to compensate for the memory effects of the PA. A gain amplifier(11-dB gain) and a π-type fixed attenuator in the linear path(3-dB attenuation) make the input and output power levels of the proposed MBAPD identical. In this experiment, the τ_N and τ_L are 1.8 ns and 5.4 ns, respectively. The optimum $\Delta\tau$ is 0.7 ns, which is experimentally determined based on [13]. The vector modulator provides an attenuation over 40 dB and a phase shift over 280° using a variable attenuator and two variable phase shifters, which are fabricated with a 3-dB hybrid coupler, PIN diodes, and varactor diodes. The 3-dB hybrid couplers(Anaren JX 503) and three-way in-phase power splitters(Anaren 4J3305) are used at the input and output of the three-branch nonlinear path in the MBAPD. Fig. 5 depicts a photograph of the fabricated MBAPD.

The class-AB PA has been fabricated using Freescale MRF21030 LDMOSFET with a 30-W PEP at a drain bias voltage(V_{DD}) of 28 V and a V_{GS} of 3.604 V(I_{DQ} = 150 mA) at 2.14 GHz. To reduce memory effects, the drain bias circuit incorporates a $\lambda/4$ bias line with a 3-mm line width and several decoupling capacitors.

3-1 Memory-Compensated MBAPD

To investigate the memory-effect compensation of the MBAPD for a one-carrier WCDMA signal, with a PAPR of approximately 10 dB, we have explored at an average output power(P_{out}) of 33 dBm, which is a 10.2-dB BOP from the P_{1dB} of 43.2 dBm. Fig. 6 shows the measured predistorted signals for the CAPD and MBAPD when the P_{out} of the PA is 33 dBm. Compared to the CAPD with symmetrical signals, the MBAPD shows higher spurious emission in the lower band than in the upper band, which is similar to the asymmetry of the PA with memory effects, as shown in Fig. 7. From

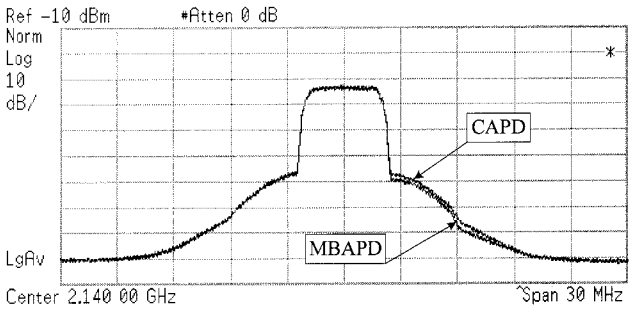


Fig. 6. Measured predistorted signals for the CAPD and MBAPD at a P_{out} of 33 dBm for a one-carrier WCDMA signal.

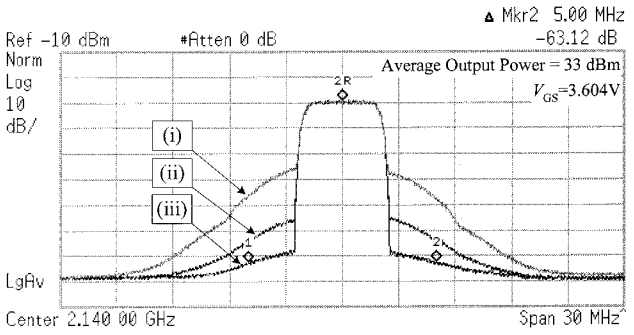


Fig. 7. Measured PSDs of the PA at a P_{out} of 33 dBm for a one-carrier WCDMA signal. (i) Without APD, (ii) With CAPD, and (iii) With MBAPD.

Table 1. Summary of measured result at 33 dBm for a one-carrier WCDMA signal.

Contents		Without APD	With CAPD	With MBAPD
ACLR [dBc]	−5 MHz	−36.7	−54.2	−63.1
	+5 MHz	−39	−54.4	−63.1

the measured power spectral densities(PSDs) in Fig. 7, the MBAPD compensates for memory effects of the PA by fine adjustment of the three vector modulators and then significantly improves an adjacent channel leakage ratio(ACLR). Table 1 shows a summary of the measured results. The ACLRs are measured at the offset of ±5 MHz from 2.14 GHz.

3-2 Effects of Drain Bias

Fig. 8 shows the measured gain and drain efficiency of the PA at various V_{DD} according to P_{out} for a continuous wave(CW). Also shown is the probability density function(PDF) of a one-carrier WCDMA signal. From this figure, the PA with V_{DD} modulation can be observed to deliver high efficiency when the PDF is heavily gathered for a one-carrier WCDMA signal. Fig. 9 shows the measured ACLR and drain efficiency of the PA without APD at various V_{DD} as a function of P_{out}. The ACLRs are measured at −5-MHz offset. From the measured results, the linearity of the PA is degraded as the V_{DD} decreases, in spite of the efficiency enhancement. For this reason, we have employed the previous MBAPD to improve the linearity.

Fig. 10 shows the measured ACLR and drain efficiency of the PA with MBAPD. At each P_{out}, the vector modulators in the APD are optimized to maximize the

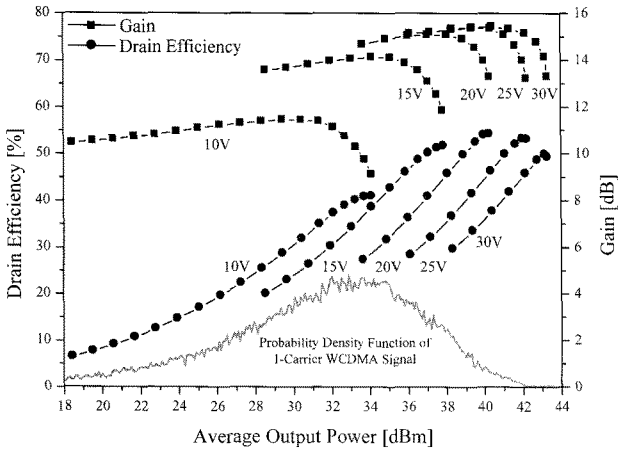


Fig. 8. Measured gain and drain efficiency of the PA at various V_{DD} according to P_{out} for a CW and the PDF of a one-carrier WCDMA signal.

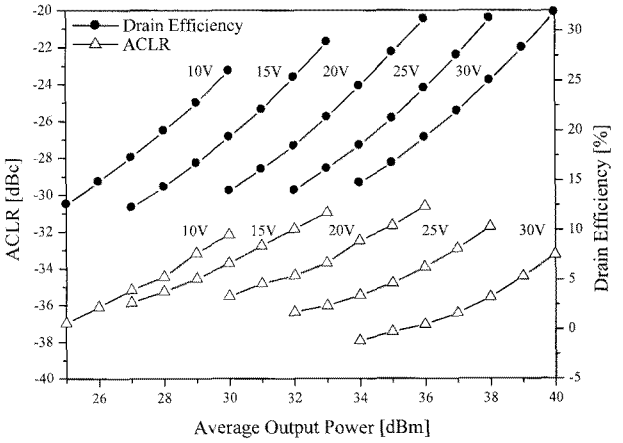


Fig. 9. Measured ACLR and drain efficiency of the PA without APD at various V_{DD} as a function of P_{out} for a one-carrier WCDMA signal.

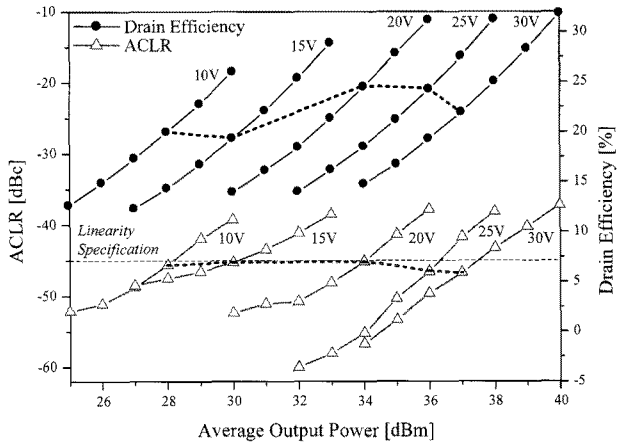


Fig. 10. Measured ACLR and drain efficiency of the PA with MBAPD at various V_{DD} according to P_{out} for a one-carrier WCDMA signal.

ACLR. The dotted lines illustrate the minimum V_{DD} at each P_{out} and the corresponding drain efficiency when the ACLR linearity specification of −45 dBc at ±5-MHz offset is satisfied. The measured results prove that the linearity of the PA with MBAPD can be improved while increasing the efficiency with the V_{DD} modulation.

Fig. 11 depicts the measured ACLR and drain efficiency of the PA with MBAPD according to V_{DD} at a P_{out} of 33 dBm for a one-carrier WCDMA signal. When the PA with MBAPD satisfies the linearity specification of −45 dBc with the maximum drain efficiency, the optimum VDD is 18 V.

Fig. 12(a) shows the Measured ACLRs of the PA without APD at a V_{DD} of 28 V and the PA with MBAPD and V_{DD} modulation according to P_{out} for a

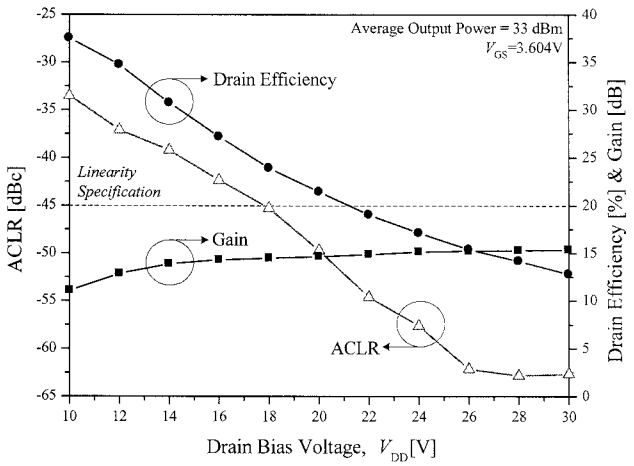
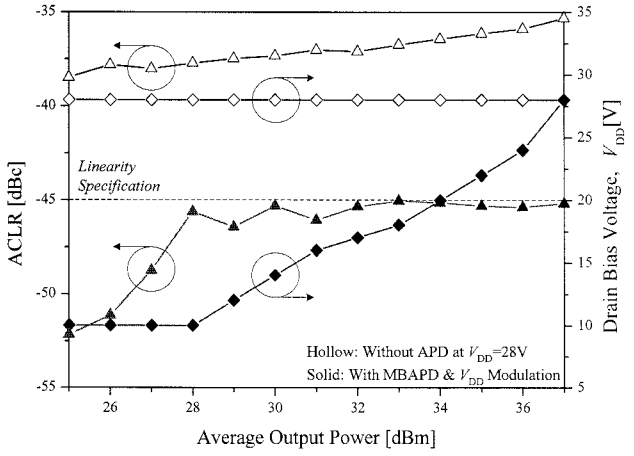
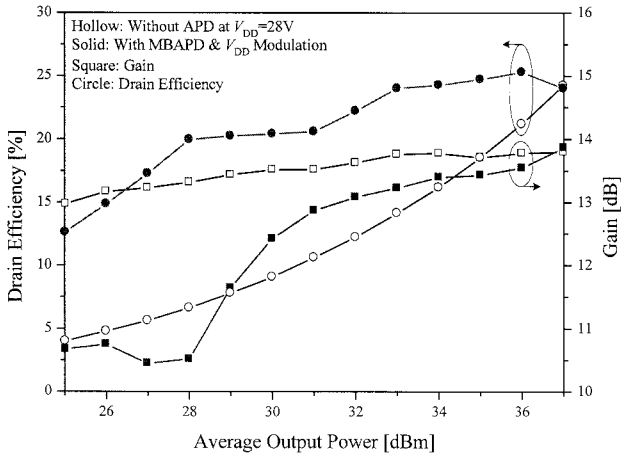


Fig. 11. Measured ACLR, gain, and drain efficiency of the PA with MBAPD according to V_{DD} at a P_{out} of 33 dBm for a one-carrier WCDMA signal.



(a) ACLR



(b) Drain efficiency and gain

Fig. 12. Measured performance of the PA without APD at a V_{DD} of 28 V and the PA with MBAPD and V_{DD} modulation according to P_{out} for a one-carrier WCDMA signal.

Table 2. Summary of measured results at 33 dBm for a one-carrier WCDMA signal.

Contents	V_{DD} [V]	Gain [dB]	Drain efficiency [%]	ACLR [dBc]
Without APD	18	13.1	24.2	−30.5
Without APD	28	15.3	14.1	−36.7
With MBAPD	18	13.2	24.0	−45.1
With MBAPD	28	15.3	14.1	−63.1

one-carrier WCDMA signal. For the PA with MBAPD and V_{DD} modulation, the ACLR is improved by optimally adjusting the MBAPD although the V_{DD} decreases, as compared to the PA without APD at V_{DD} of 28 V. Fig. 12(b) shows the measured drain efficiency and gain for two conditions. For the PA with MBAPD and V_{DD} modulation, the efficiency is improved with lower V_{DD} while reducing the ACLR below −45 dBc. Table 2 shows a summary of the measured results, for various conditions.

Ⅳ. Conclusion

We have investigated the effects of drain bias on the linearity and efficiency of analog predistortion PA for WCDMA repeater applications. For experimental validations, an MBAPD with three-branch nonlinear paths for memory-effect compensation was implemented and the class-AB PA was fabricated with a 30-W Si LDMOSFET. From the measured results at a P_{out} of 33 dBm (10-dB back-off power), the PA with MBAPD showed an ACLR(±5 MHz offset) of below −45.1 dBc with a drain efficiency of 24 % at the V_{DD} of 18V, compared to the PA without APD with an ACLR of −36.7 dBc and drain efficiency of 14.1 % at the V_{DD} of 28 V. From the measured results, it is evident that the PA with MBAPD can be a highly efficient and linear solution for WCDMA repeater applications when the ET or other high-efficiency bias modulation techniques are successfully applied.

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References

[1] Y. S. Lee, Y. H. Jeong, "A high-efficiency class-E

GaN HEMT power amplifier for WCDMA applications", *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 8, pp. 622-624, Aug. 2007.

[2] Y. S. Lee, M. W. Lee, and Y. H. Jeong, "High-efficiency class-F GaN HEMT amplifier with simple parasitic-compensation circuit", *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 1, pp. 55-57, Jan. 2008.

[3] Y. Y. Woo, Y. Yang, and B. Kim, "Analysis and experiments for high-efficiency class-F and inverse class-F power amplifiers", *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 5, pp. 1969-1974, May 2006.

[4] Y. S. Lee, M. W. Lee, and Y. H. Jeong, "Unequal-cells-based GaN HEMT Doherty amplifier with an extended efficiency range", *IEEE Microw. Wireless Compo. Lett.*, vol. 18, no. 8, pp. 536-538, Aug. 2008.

[5] Y. S. Lee, M. W. Lee, and Y. H. Jeong, "Highly efficient Doherty amplifier based on class-E topology for WCDMA applications", *IEEE Microw. Wireless Compo. Lett.*, vol. 18, no. 9, pp. 608-610, Sep. 2008.

[6] Y. S. Lee, M. W. Lee, and Y. H Jeong, "Highly efficient class-F GaN HEMT Doherty amplifier for WCDMA applications", *Microw. Opt. Tech. Lett.*, vol. 50, no. 9, pp. 2328-2331, Sep. 2008.

[7] D. F. Kimball, J. Jeong, C. Hsia, P. Draxler, S. Lanfranco, W. Nagy, K. Linthicum, L. E. Larson, and P. M. Asbeck, "High-efficiency envelope-tracking W-CDMA base-station amplifier using GaN HFETs", *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 11, pp. 3848-3856, Nov. 2006.

[8] F. Wang, D. F. Kimball, J. D. Popp, A. H. Yang, D. Y. Lie, P. M. Asbeck, and L. E. Larson, "An improved power-added efficiency 19-dBm hybrid envelope elimination and restoration power amplifier for 802.11g WLAN applications", *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4086-4099, Dec. 2006.

[9] F. H. Raab, P. Asbeck, S. C. Cripps, P. B. Kenington, Z. B. Popović, V. Pothecary, J. F. Sevic, and N. O. Sokal, "Power amplifiers and transmitters for RF and microwave", *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 3, pp. 814-826, Mar. 2002.

[10] Y. S. Lee, S. Y. Lee, K. I. Jeon, and Y. H. Jeong, "Highly linear predistortion power amplifiers with phase-controlled error generator", *IEEE Microw. Wireless Compo. Lett.*, vol. 16, no. 12, pp. 690-692, 2006.

[11] Y. S. Lee, M. W. Lee, G. B. Choi, and Y. H Jeong, "New analog predistorter using mixing operation for independent control of IM3 components", *Microw. Opt. Tech. Lett.*, vol. 49, no. 10, pp. 2552-2555, Oct. 2007.

[12] J. Kim, Y. Y. Woo, J. Moon, and B. Kim, "A new wideband adaptive digital predistortion technique employing feedback linearization", *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 2, pp. 385-392, Feb. 2008.

[13] J. Carvers, T. Johnson, "Wideband linearization: Feedforward plus DSP", in *Proc. MTT-S 2004 Workshop*, 2004.

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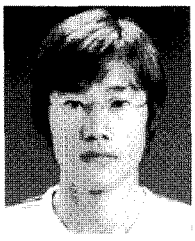

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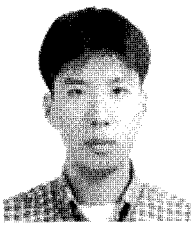

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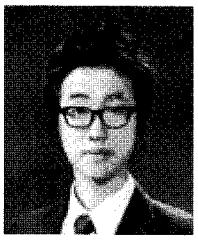

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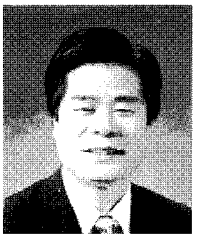

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