Class-E CMOS PAs for GSM Applications

Hongtak Lee · Yumi Lee[1] · Changkun Park[2] · Songcheol Hong[1]

Abstract

Various Class-E CMOS power amplifiers for GSM applications are presented. A stage-convertible transformer for a dual mode power amplifier is proposed to increase efficiency in the low-output power region. An integrated passive device(IPD) process is used to reduce combiner losses. A split secondary 1:2 transformer with IPD process is designed to obtain efficient and symmetric power combining. A quasi-four-pair structure of CMOS PA is also proposed to overcome the complexities of power combining.

Key words : Class E, CMOS, Power Amplifier, Power Combiner, Global System for Mobile Communication(GSM), Polar Transmitter, Transformer, Variable Load, Integrated Passive Device(IPD).

Ⅰ. Introduction

A polar transmitter is very attractive architecture because of its many advantages over conventional transmitters, especially in GSM and EDGE systems. Accordingly, switch-mode power amplifiers for its application are being intensively studied. Recently, with the development of a CMOS process, the potential of a CMOS power amplifier(PA) was successfully demonstrated[1]~[3]. A CMOS PA offers the advantage of a higher level of integration with various digital control circuits in mobile transmitters and low cost over a GaAs-based PA. In this paper, several Class-E CMOS power amplifiers are designed.

A dual-mode power amplifier with a stage-convertible structure is designed. In general, a power amplifier only achieves its peak efficiency at a maximum output power, and the efficiency seriously degrades as the output power reduces. The transmitted power in a wireless system is far below its maximum most of the time[4]. It is, therefore, essential to improve low power efficiency in order to enhance the average power efficiency[4]~[7]. Thus we designed stage-convertible power amplifiers with dual-primary transformers.

Although the distributed active transformer is considered to have the potential to improve the performance of a CMOS power amplifier, the fact that CMOS power amplifiers have lower efficiency levels to GaAs HBT power amplifiers is problematic[8]. To overcome the lossy characteristics of a silicon substrate-the main reason for the degradation of efficiency in power amplifiers-a transformer to combine output power is implemented with an integrated passive device(IPD) process for efficient power amplification. We also designed a split secondary 1:2 transformer for the symmetric impedance level in differential power amplifiers.

Finally, a quasi-four-pair structure with an IPD transformer is designed. The configuration of power transistors is also important for obtaining high performance because the configuration determines the matching condition at the output network of a PA and the complexity of the input feeding lines. A high power capability and simple implementation can be obtained with the quasi-four-pair structure.

Ⅱ. Dual Mode Power Amplifier with Stage-Convertible Structure

2-1 Stage-Convertible Structure

A power combiner is a very important part of power amplifier[9]. A transformer is widely used as an impedance converter from 50 ohm to lower impedance of PAs, as well as a power combiner[1]~[3]. The output power, P_{OUT}, and the drain efficiency(DE) in a switching power amplifier are determined by the load impedance, R_{LOAD}, supply voltage, V_{DD}, and on-resistance of the power transistors, R_{ON}. It can be expressed as,

$$P_{OUT}(W) \propto \frac{V_{DD}^{2}}{R_{LOAD}} \tag{1}$$

$$DE \propto \frac{R_{LOAD}}{R_{ON} + R_{LOAD}} \tag{2}$$

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Although the low load impedance is required to obtain high maximum output power, the load impedance must be increased as the V_{DD} is decreased in order to increase efficiency. Thus, the transformer should achieve a high impedance transformation ratio to obtain power at the high V_{DD} and a low impedance transformation ratio for high efficiency at the low V_{DD}.

Fig. 1 shows the architecture of dual mode power amplifiers with stage-convertible structures. In the high power mode, a driver stage functions as a driver amplifier of a power stage. The power generated in the power stage is much higher than that generated in the driver stage, thus almost power is generated in the power stage in the high power mode. In the low power mode, the driver stage functions as the power stage because the power stage is turned off and the output power of the driver stage is transmitted to a power combiner. The efficiency could be increased because DC power loss at a power stage is removed during the low power mode.

A simplified structure of a dual-primary transformer is shown in Fig. 2[10]. Note, ports of the inner primary part are connected to a power stage for the high power mode, and ports of the outer primary part are connected to a driver stage for the low power mode. In the high power mode, if the current, I, flows from P11 to P12, the current flowing through the secondary part is 0.5I

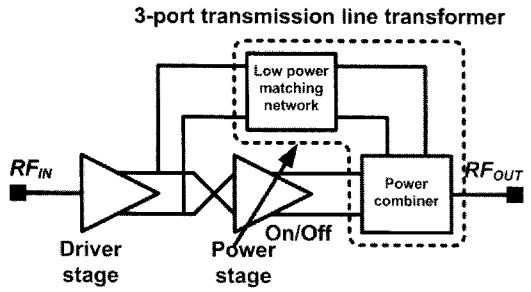


Fig. 1. Stage-convertible structure.

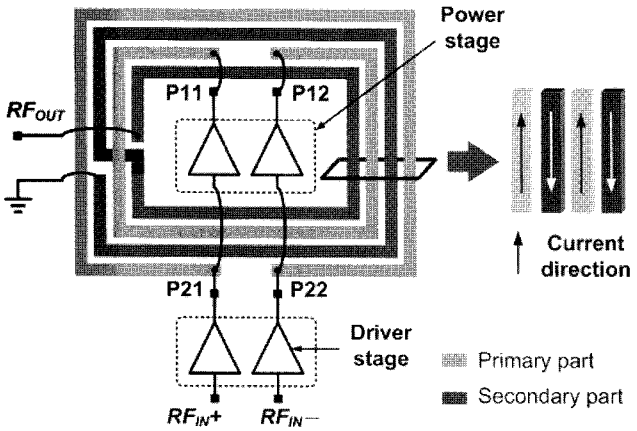


Fig. 2. A dual-primary transformer.

because it surrounds the primary part connected with the power stage. If the output voltage of each power amplifier is +V and −V, the voltage drop between RF_{OUT} and ground is 4 V. Thus, the impedance transform ratio is 8, because RF_{OUT} is connected to the 50 Ω terminal; the equivalent resistance connected with the power amplifier can be calculated as 6.25 Ω. In the low power mode, the secondary part can be considered as two parts. One of the secondary parts adjoins the outer primary part and the other secondary part is located away from the outer primary part. The magnetic coupling between the primary part and the secondary part(which is located away from the outer primary part) is expected to be very weak. If the current, I, flows from P21 to P22, then the current flowing through the secondary part is almost the same as I, the voltage drop of RF_{OUT} can be 2 V. The equivalent resistance connected with the power amplifier can be calculated as 25 Ω. Thus, the levels of output impedance are different between the low and high power modes. Therefore, the dual-primary transformer can be used to increase efficiency in the low-power region of a power amplifier. Additionally, the power stage is programmed to automatically turn on or off according to the variable supply voltage. The contribution of the power stage to the output power is decreased and the contribution of the driver stage to the output power is increased as the V_{DD} is decreased. Thus, the high power mode becomes dominant at the high V_{DD} region and the low power mode becomes dominant at the low V_{DD} region.

2-2 Implementation and Measured Results

Fig. 3 shows the implemented power amplifiers using a 0.18 μm RF CMOS technology and measurement

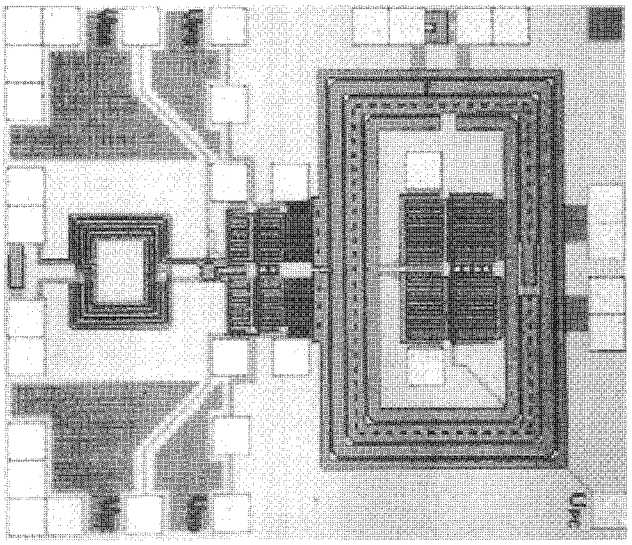


Fig. 3. Chip photograph.

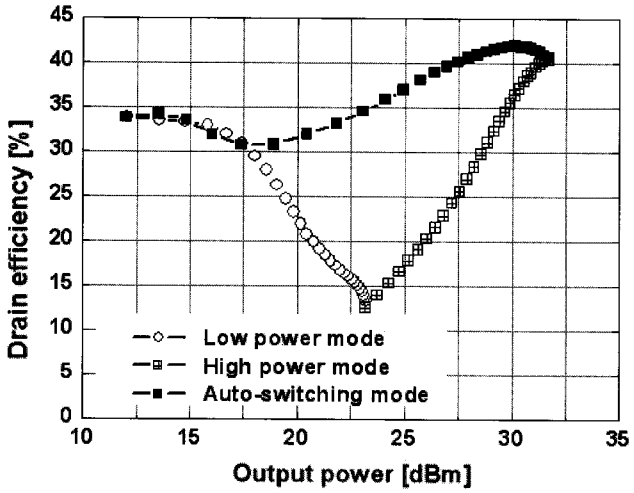


Fig. 4. Measurement results.

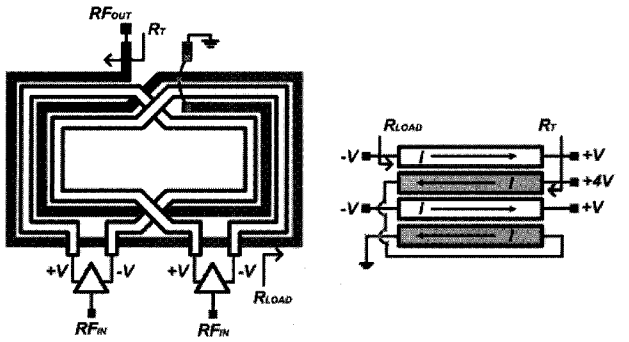
results. The size of chip is 0.85×0.53 mm^2. The efficiency versus output power was measured while the supply voltage varies from 0.5 to 3.3 V. As shown in Fig. 4, the mode of the power amplifier is changed automatically and smoothly according to the V_{DD}.

Ⅲ. CMOS Power Amplifier Using a Split Secondary 1:2 Transformer with an Integrated Passive Device Process

3-1 Split Secondary Two Turn Transformer

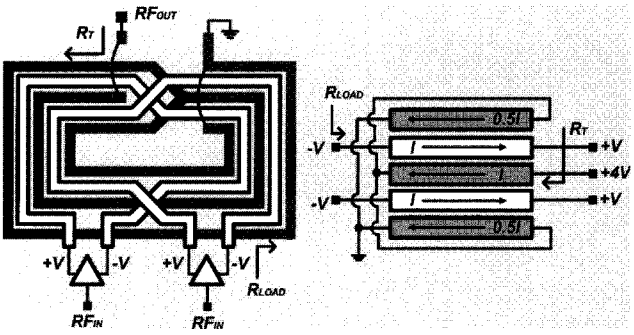
The parasitic resistance of the transformer using IPD is lower than that of the conventional RF CMOS process. Additionally, the coupling factor is also increased since the edge-side area of metal line for the transformer is increased. The designed power amplifier consists of a CMOS chip which comprises all active devices and input matching networks and integrated passive devices for transformer. To increase the output power, we need to increase the number of power stages or decrease the load impedance. Low load impedance can be obtained by increasing the number of turns in the secondary part of the transformer. Our PA design, therefore, includes a 1:2 transformer with two power stages.

In Fig. 5, one primary part is located between two secondary parts, and the other is on only one side of a secondary part. The difference in the magnetic couplings can cause a difference in the mutual inductances between the secondary part and the primary part, which can create asymmetric impedances in the differential amplifier. This can increase second harmonics and the maximum power is limited by a few transistors at the onset of breakdown[11]. Thus we divided the secondary part into two parts, where one is located inside and the other is located outside of the primary part, as shown in



(a) Simplified two turn transformer (b) Equivalent structure of the two turn transformer

Fig. 5. Conventional two turn transformer.



(a) Simplified split secondary two turn transformer (b) Equivalent structure of the split secondary two turn transformer

Fig. 6. Split secondary two turn transformer.

Fig. 6. Since all the primary parts are now located between two secondary parts, greater symmetric load impedance of differential pairs can be achieved. The symmetric differential pair is known to allow very small even harmonics.

3-2 Implementation and Measured Results

Fig. 7. shows the implemented power amplifier. The core power amplifier is based on 0.18 μm RF CMOS technology and the transformer is based on the IPD process. They are connected by bond-wires and there are no additional off-chip matching components, with the exception of the transformer. The size of the CMOS chip, including all the pads, is 1.6×1.1 mm^2 and the transformer is 1×1.1 mm^2. The output power is larger than 32.1 dBm, which has 0.1 dB flatness and the power added efficiency is higher than 52 % in operation frequency from 1.71 GHz to 1.91 GHz. The power added efficiency is 57 % at a maximum output power of 32.3 dBm in the DCS band. The harmonic response is shown in Fig. 8(a). The second harmonic is −39 dBc and the third harmonic is −31 dBc at the worst case. Fig. 8(b) shows the power added efficiency and the

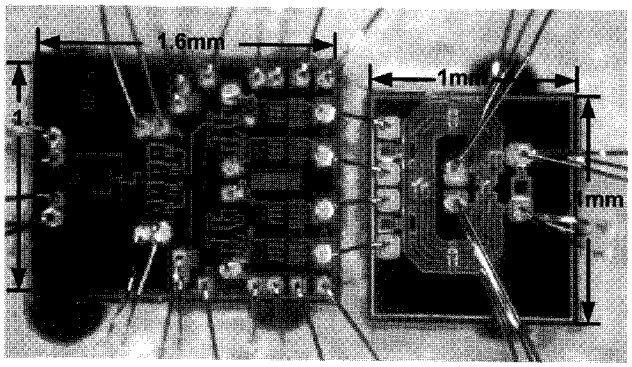
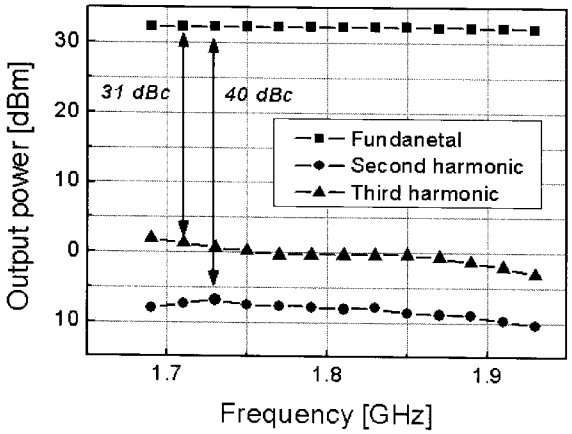
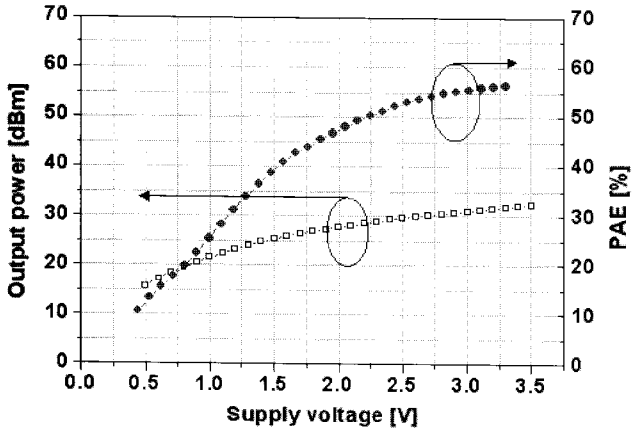


Fig. 7. Photograph of the implemented power amplifier.



(a) Harmonic characteristics versus frequency



(b) Output power and PAE versus supply voltage

Fig. 8. Measurement results.

output power while the supply voltage of the power stage varies from 0.5 V to 3.3 V at 1.81 GHz.

Ⅳ. Quasi 4-Pair Class-E CMOS RF Power Amplifier with an Integrated Passive Device Transformer

4-1 Quasi-Four-Pair Structure

The GSM/EDGE PA requires the output power to be above 33 dBm over a frequency range of 1.71~1.91 GHz. The output power P_{OUT} of an ideal class-E amplifier is determined by the output load impedance R_T, the supply voltage V_{DD}, number of the amplifiers N, and the efficiency of PA, η, as in [12]

$$P_{OUT} = 1.365 \times \frac{V_{DD}^{\ 2}}{R_T} \times N \times \eta \tag{3}$$

The output power of the two differential pairs in the voltage combining method can be calculated as in (3). When the load impedance is 50 Ω, the supply voltage 3.3 V, and the assumed efficiency of PA is 50 %,

$$P_{OUT} = 1.365 \times \frac{3.3^2}{12.5} \times 4 \times 0.5 = 2.38 \approx 33.8\, dBm \tag{4}$$

Thus, at least two differential pairs are needed to satisfy the power requirement. A larger number of differential pairs are necessary to generate enough output power with margins. A three-pair constitution can be a candidate. However, it is difficult to obtain symmetry and to form input feed lines. Therefore, we designed a four-pair structure with sufficient power. In spite of the high output power of the structure with more than two plural pairs, there were several problems. Above all, to constitute the circuitry of the power stage, many components are needed. This makes the size too big. Moreover, the driver stages and input feed-lines for the power transistors should be more complicated. It may cause loss of the circuit or generate an instability issue due to coupling.

Fig. 9 illustrates the simplified quasi-four-pair structure. Two common gate transistors are connected to one common source transistor. The additional common gate transistor of the cascade form makes multiple paths of amplification in the power stage. Thus, by composing differential pairs with this configuration as in Fig. 9, plural output combining can be accomplished using one-differential common-source pair in the power stage. It

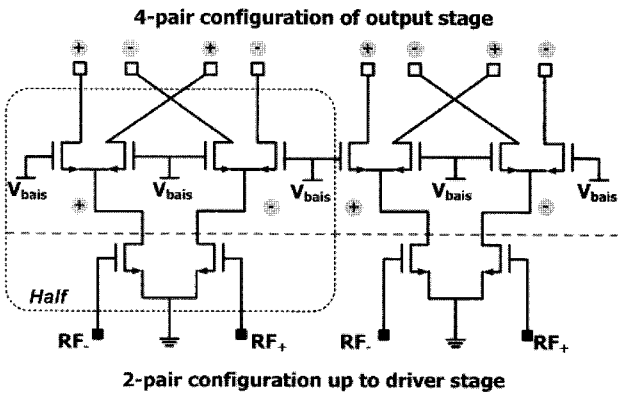


Fig. 9. Circuit diagram of the quasi-four-pair structure.

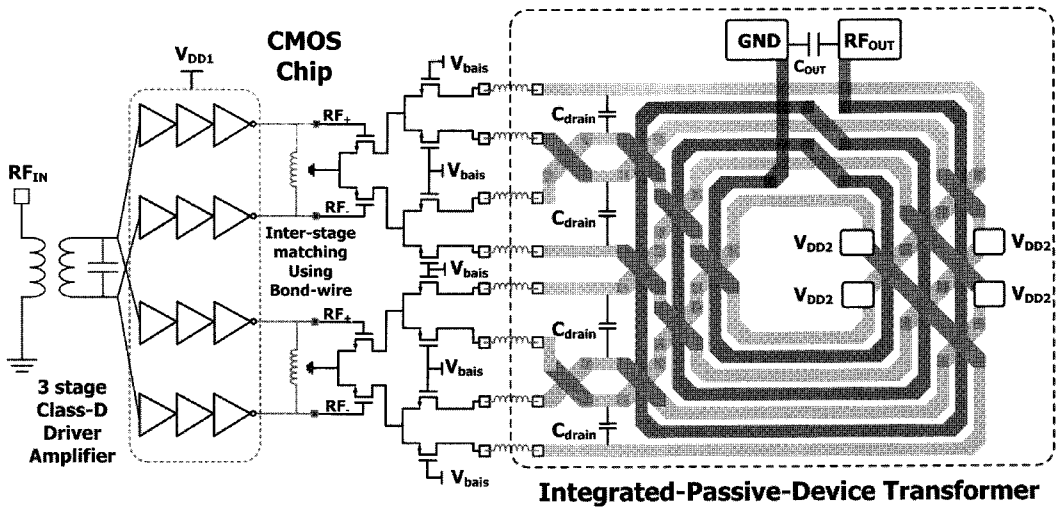


Fig. 10. Schematics of the quasi-four-pair power amplifier.

can increase the impedance transforming ratio and the number of differential pairs under the ideal voltage combining method.

Thus, additional combining of pairs in the output stage can increase output power. The constitution of the circuit for the driving power stage is the same as the two-pair structure. Accordingly, both the capability of high output power in the four-pair structure and simple implementation can be obtained.

4-2 Implementation and Measured Results

Fig. 10 shows the overall schematics of the designed PA and a photograph of the implementation is shown in Fig. 11. The designed PA utilized the IPD transformer for output matching. The IPD transformer has lower parasitic resistance than those of the RF CMOS process. Power combining of the output matching network can

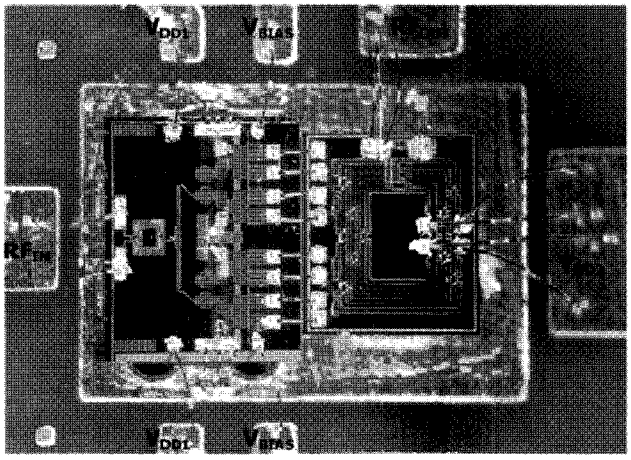


Fig. 11. Photograph of the implemented overall power amplifier.

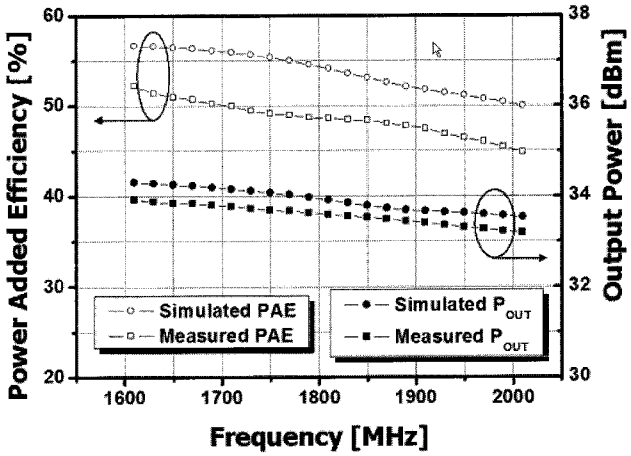


Fig. 12. Measured output power and PAE versus frequency.

be efficiently accomplished using this solution. In addition, stability issues induced by unwanted feedback loops can be solved by the two-chip solution. The chip area is 1.6×1.2 mm^2 including the input transformer and the bonding pads. The input on-chip balun was designed to support differential operation of the driver and power stages. For the three-stage driver amplifiers, the topology of class-D amplifier chain with stabilized bias was used [13]. The transformer is 1.4×1.2 mm^2 in size and was fabricated in an integrated passive device process.

Fig. 12 shows the measured output power(P_{OUT}) and Power-Added Efficiency(PAE) with respect to the input frequency, for which the supply voltages are 3.3 V for the power stage and 1.8 V for the driver stage. The single-ended output power is always higher than 33.4 dBm in the frequency band from 1.71~1.91 GHz with 0.4 dB gain flatness. The maximum output power is 33.8 dBm at the 1.71 GHz.

Ⅴ. Conclusion

Various Class-E CMOS PAs for GSM applications were designed. These are based on a transmission line transformer using magnetic coupling. A transformer significantly influences the output power and efficiency in a CMOS power amplifier. A stage-convertible transformer for a dual mode power amplifier increases the efficiency in the low-output power region. A split secondary 1:2 transformer with an integrated passive device process is proposed to obtain efficient and symmetric power combining. A quasi-four-pair structure with an integrated passive device transformer is proposed to overcome complexities in the power stage and efficiency problems.

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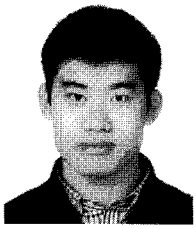

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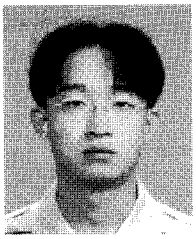

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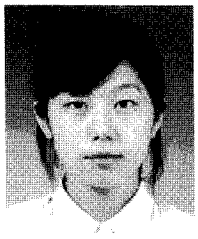

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