Design Issues of CMOS VCO for RF Transceivers

Seonghan Ryu

Abstract

This paper describes CMOS VCO circuit design procedures and techniques for multi-band/multi-standard RF transceivers. The proposed techniques enable a 4 GHz CMOS VCO to satisfy all requirements for Quad-band GSM/EDGE and WCDMA standards by achieving a good trade-off among important specifications, phase noise, power consumption, modulation performance, and chip area efficiency. To meet the very stringent GSM T/Rx phase noise and wide frequency range specifications, the VCO utilizes bond-wire inductors with high-quality factor, an 8-bit coarse tune capbank for low VCO gain(30~50 MHz/V) and an on-chip 2nd harmonic noise filter. The proposed VCO is implemented in 0.13 μm CMOS technology. The measured tuning range is about 34 %(3.17 to 4.49 GHz). The VCO exhibits a phase noise of −123 dBc/Hz at 400 kHz offset and −145 dBc/Hz at 3 MHz offset from a 900 MHz carrier after LO chain. The calculated figure of merit(FOM) is −183.5 dBc/Hz at 3 MHz offset. This fully integrated VCO occupies 0.45×0.9 mm^2.

Key words : CMOS, Phase Noise, Wide Tuning Range, Complementary and NMOS Only Type VCO, Bondwire Inductor, Second Harmonic Filtering.

Ⅰ. Introduction

The worldwide wireless communication market today requires miniaturized and cost-effective RF transceivers for global mobility and wide coverage of the proposed communication service. The very wide operating frequency range of the device solution is also required to meet the needs of next-generation(3 G/4 G) communication service, which has very high data rates. CMOS is the potent candidate technology meeting these demands since continuous scaling down of CMOS technology make it possible to increase complexity and operating speed of silicon integrated circuits.

Among the efforts for highly integrated wireless CMOS transceivers, the implementation of a low phase noise Voltage Controlled Oscillator(VCO) is crucial for information transfer integrity. The spectral purity of a VCO actually limits the maximum number of users and channels of the communication system, which means that the VCO performance has a considerable effect on the economic feasibility of the system configuration. Fortunately, the theory and analysis for the physical processes of the phase noise in VCOs have significantly progressed these days and the techniques to lower the phase noise have been advanced by understanding of these phase noise mechanism[1]~[3].

Despite these attainments, there are still some issues to designing a CMOS VCO generating multi-band/multi-standard carrier. Usually, GSM operations require a single VCO to support both the transmitter(Tx) part and the receiver(Rx) part. To meet demand for spurious tones and single tone desensitization of the receiver mode, the phase noise at 3 MHz offset must be below −140 dBc/Hz. For the transmitter mode, the modulated spectrum must fit within a spectral transmission mask that requires the phase noise at 400 kHz offset to fall to below −118 dBc/Hz. Tx and Rx bands of GSM are 20 MHz apart. To prevent amplified phase noise in Tx VCO from overwhelming a signal being received in another nearby handset, the phase noise at 20 MHz offset should be less than −162 dBc/Hz. In addition to these stringent phase noise requirements, the VCO should have very wide tuning range of about 25 % for multi-band/multi-standard operation such as quad-band GSM/EDGE and WCDMA. Even though these two main issues are settled, some issues remain such as VCO gain variation and linearity issues for EDGE modulation spectrum mask requirements and low power dissipation issue, which is indispensable in integrated system for mobile terminals.

In this paper, circuit design issues and procedures to acquire an optimum trade-off between the above specifications are discussed, and a fully integrated CMOS VCO with bond-wire inductors satisfying all of these requirements for Quad-band GSM/EDGE and WCDMA standard is proposed.

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II. VCO Design Procedures

The mobile integrated system for quad-band GSM/EDGE and WCDMA requires the VCO having a very wide tuning range and very low phase noise at both close in offset and higher offset from the carrier frequency.[4] Since complex carrier generation structures using a harmonic mixer have various non-ideal effects including harmonics coupling, a simple frequency planing based on only divide-by-two prescaler is favored these days. This simple LO chain structure is the optimum solution to minimize the cost in terms of system complexity, power consumption and area in comparison with other solutions such as quadrature VCO(QVCO) and a polyphase filter. QVCO requires doubling both area and power consumption. The polyphase filter has similar defects to lose dependency on the process variation and mismatches[5].

In the simple prescaler only LO chain, even though carrier frequency doubling is needed to generate quadrature *I/Q* signal, side effects of other structures such as self-mixing, DC-offset and frequency pushing/pulling can be minimized.

Fig. 1 depicts a frequency planning for the carrier generation of quad-band GSM/EDGE and WCDMA standards. WCDMA Rx band is excluded in this frequency planning since WCDMA Tx and Rx are active at the same time for operation. The VCO with a frequency tuning range of 684 MHz, which is from 3,296 MHz (GSM850Tx×4) to 3,980 MHz(PCS1900Rx×2), is needed for prescaler-only scheme.

To design a wide tuning range VCO with good phase noise performance and low power dissipation, a complementary structure and an NMOS-only structure are compared. These two types depicted in Fig. 2 are mostly favored for differential CMOS VCO.

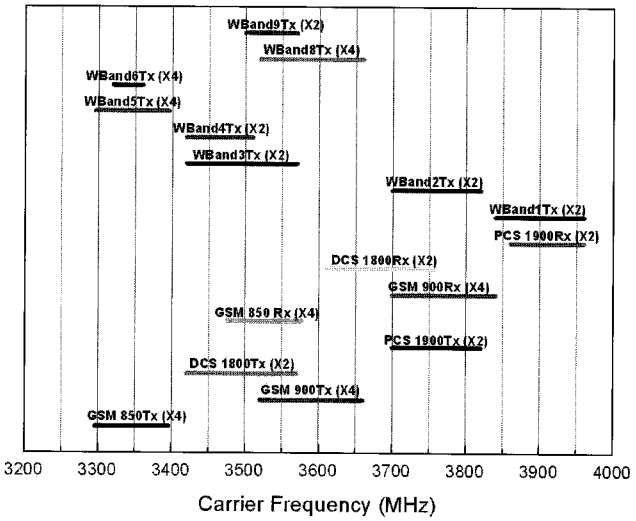

Fig. 1. Frequency planning for the carrier generation of quad-band GSM/EDGE and WCDMA standards.

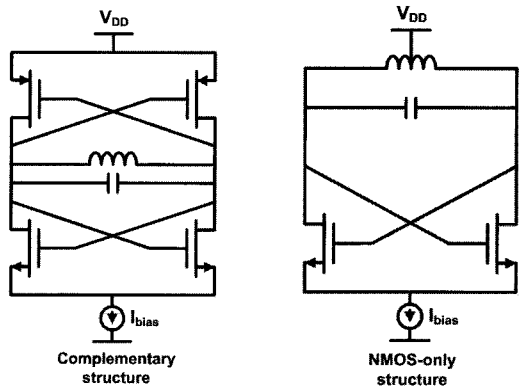

Fig. 2. Comlementary and NMOS-only VCO structure.

In general, the performance of the complementary type is known as superior, since the complementary structure has higher transconductance(G_M) for a given current and a smaller $1/f^3$ noise corner by better rise- and fall-time symmetry[6]. Nonetheless, the phase noise of the complementary type at each offset frequency may become worse than that of the NMOS-only type as the bias current increases. Fig. 3 shows this phase noise performance reversal at 400 kHz, 3 MHz, and 20 MHz offset frequencies from the carrier of around 4 GHz, respectively.

The well-known phase noise model for an oscillator is Leeson's proportionality[7].

$$L\{\triangle\omega\} \propto \frac{1}{V_0^2} \cdot \frac{kT}{C} \cdot \left(\frac{\omega_0}{Q}\right)^2 \cdot \frac{1}{\omega_m^2} \quad (1)$$

Where the phase noise is given by *kT/C* noise that is shaped in frequency domain by LC tank and normalized to the power in the tank. This expression reveals the

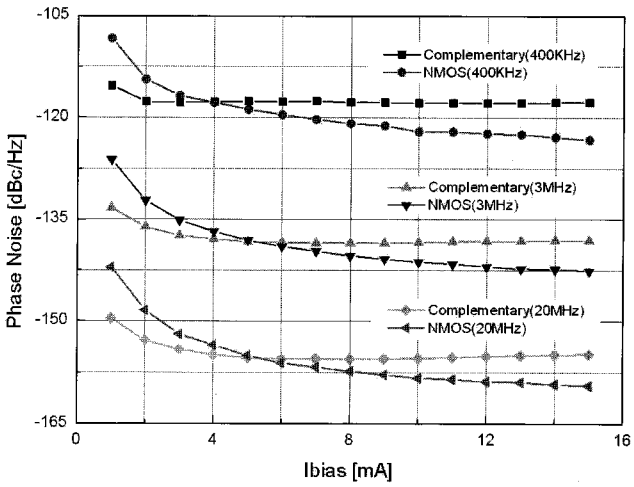

Fig. 3. Simulated phase noise of the VCOs at each offset frequency as a function of bias current.

dependency of the phase noise upon the signal amplitude V_o. For the complementary type VCO, as the bias current increases, signal amplitude is limited by V_{DD} in the voltage limited regime, while the NMOS-only type VCO enables higher voltage swing above V_{DD} limit. This explains the reversal of the phase noise characteristics.

Although the complementary type still maintains better phase noise performance for relatively small bias current, below 4~5 mA, with V_{DD} of 1.8 V as depicted in Fig. 3, this bias current is not enough to satisfy the requirements for multi-band/multi-standard operation. In addition, considering various lossy components of the real circuits, enough phase noise margin is necessary to satisfy the harsh phase noise constraints of GSM standard.

Accordingly, the NMOS-only type is adopted. With this VCO type, a wider tuning range can also be attained due to minimized parasitic capacitances of active devices. In lower V_{DD} operation which is inevitable with scaled-down CMOS technology, the reversal of the phase noise characteristics takes place at much lower bias current. Therefore, the NMOS-only type VCO is a potent candidate for multi-band/multi-standard carrier generator.

From equation (1), phase noise is also strongly dependent on Q, the quality factor of the resonator, which can be expressed as

$$\frac{1}{Q}=\frac{1}{Q_L}+\frac{1}{Q_C} \tag{2}$$

where Q is dominated by Q_L, quality factor of inductor since Q_C, the quality factor of capacitor is high enough. Fig. 4 shows simulated phase noise of the VCOs at 400 kHz and 20 MHz offsets from the carrier signal frequency around 4 GHz, respectively, as a function of inductor Q factor. The inductance value is about 1 nH for oscillation frequeny around 4 GHz. As shown in Fig. 4, phase noise is reduced as Q_L increases. General CMOS process technology provides Q_L of below 10 for this relatively low inductance value, and this Q_L value is too low to satisfy phase noise requirement of GSM. For custom single-turn inductor designed using EM simulator, Q_L of around 15~20 is feasible with reasonable inductor size, out-diameter of around 400~500 μm.

Though phase noise reduction rate becomes reduced as Q_L increases, proper Q_L value above 20 is needed for enough phase noise margin. Increasing metal strip width and out-diameter of spiral inductor enhances quality factor, however, an inductor that is too large has a much higher parasitic capacitance and is not fit for highly integrated transceivers. In order to increase Q_L without these problems, a bond wire inductor is proposed in this work. Fig. 5 shows the comparison of simulated Q_L for inductors. The bondwire inductor shows good quality factor above 30 in the frequency range of interest, 3~4 GHz.

Planar spiral and bondwire structures are simulated by 3D EM simulator. These inductors are designed to have an inductance of around 1 nH. The inductance of the bondwire structure is linearly increased with the bondwire length and can be modified by changing the distance between the two bondpads and bondwire height. Though there may be some inductance variation of around 10 %, more than 20 % of the inductance value can be tuned even after chip fabrication process by inserting dummy tuning pads in the circuit layout and changing the bondwire length or height. Though Q of the inductor is well above 30 in the operating frequency range, this is still much lower than that of capacitors, and thus, the equivalent parallel resistance of the tank,

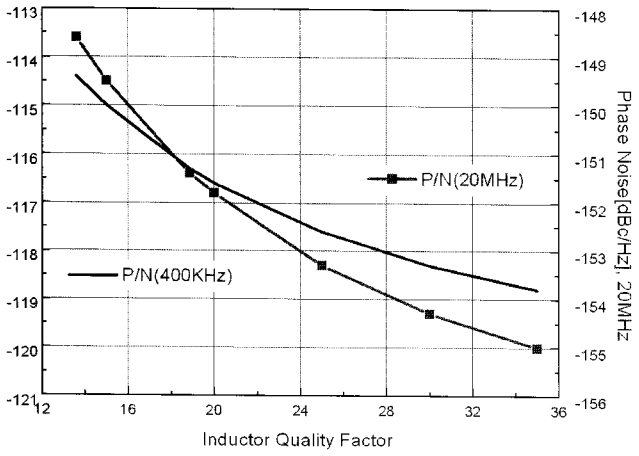

Fig. 4. Simulated phase noise of the VCOs at each offset frequency as a function of inductor Q factor.

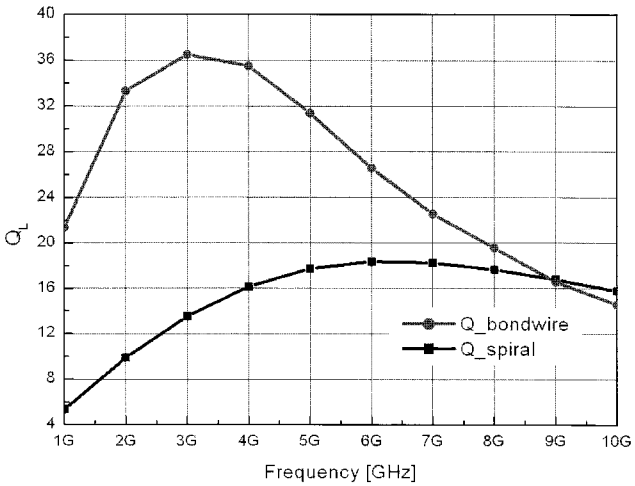

Fig. 5. Simulated Q_L for inductors.

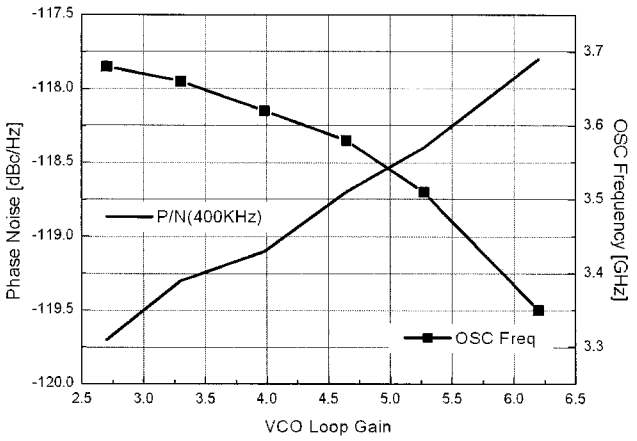

Fig. 6. Simulated phase noise at 400 kHz offset and oscillation frequency as a function of loop gain.

R_P, can be expressed as equation (3)[8]:

$$R_p = \frac{(L_{eq}\omega_{res})^2}{R_S} \tag{3}$$

with this R_P, the loop gain of the feedback circuit, oscillator, can be expressed as

$$Loop\ Gain = G_M \cdot R_p \tag{4}$$

where G_M is the transconductance of the switching differential pair. From Barkhausen's criteria, it is possible to start up oscillation with the loop gain magnitude of unity at oscillation frequency. For stable oscillation, the active device should continuously recover the energy lost in R_P. Considering various parasitic losses in the real VCO circuit, enough loop gain is needed. With the same bias current, loop gain can be increased by larger gate width, however, this decreases oscillation frequency with more active parasitics as shown in Fig. 6.

Though phase noise is better for lower loop gain, the value of about 4 is selected to avoid oscillation start-up failure and to attain robust stable oscillation with proper carrier frequency.

In the design of a resonator for quad-band GSM/EDGE and WCDMA, it is very difficult to satisfy a very wide tuning range and stringent phase noise requirement as well. In addition to attaining a high Q inductor, a switched capacitor bank and varactor should be properly designed to avoid phase noise degradation and to acquire reasonable K_{VCO}, the vco gain, for stable PLL operation. The proposed VCO structure is shown in Fig. 7. Two accumulation-type MOS varactors are used for fine tuning and data modulation, respectively. A binary-weighted switched capacitor bank with enough frequency margin is used for coarse tuning to overcome frequency shift due to PVT variations. For EDGE modulation, error vector magnitude(EVM) is degraded as nonlinearity of K_{VCO} increases. Because K_{VCO} linearity is better near the center point of the VCO control voltage (V_{CON}), PLL locking near center V_{CON} is very helpful for good transmitted signal quality. Thus, a rather large number, 8-bit binary-weighted switched capacitor bank is used in this VCO. Though large off capacitance parasitics result from the large number of coarse tuning bits, it is possible to minimize these parasitics by increasing the reverse bias of the drain and source junctions with inverters in each capacitor bank unit when the switch is off.

The VCO core current is controlled by varying the 3-bit binary weighted bias resistors, and this is helpful for minimizing power consumption by varying the bias current between the transmit and receive slots. This programmability allows the trade-off between power consumption and phase noise, which is necessary for multi-band/multi-standard VCOs.

For the phase noise concern, though the bias resistors replace active current source generating troublesome $1/f$ noise, thermal noise around the second harmonic($2\omega_o$) of the oscillation is still down converted to fundamental frequency(ω_o) by the switching pair. Filtering capacitor C_1 shorts the thermal noise to around $2\omega_o$. However, this allows degradation of the resonator Q by loading the resonator with a differential pair of FETs in the triode region. Thus, a $2\omega_o$ resonator, L_1 and C_2, is used to prohibit this degradation by providing high impedance at common source node of switching pair[3].

The design of the LO chain is another important issue since there is a significant challenge, maintaining the noise floor all the way from the low phase noise VCO to the ouput pads for GSM/GPRS noise specification.

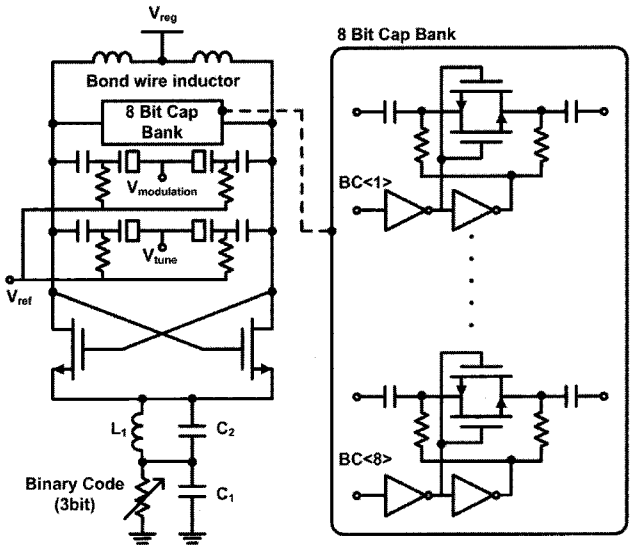

Fig. 7. Proposed VCO structure with bond-wire inductors.

Full-swing digital-logic-like circuit structures are helpful for this issue[9]. Thus, these structures are adopted for buffers and frequency dividers of the LO chain.

Ⅲ. Measurement Results

A fully integrated wideband VCO circuit for Quad-band GSM/EDGE and WCDMA standards is designed in 0.13 μm CMOS technology with the proposed circuit techniques and procedures. The microphotograph of the fabricated chip with a 0.45×0.9 mm^2 area is shown in Fig. 8.

The VCO is tunable between 3.17 GHz and 4.49 GHz and the VCO gain is 30~50 MHz/V. The resulting range is 34 % of the mid frequency. The VCO operates from 1.8 V supply and biases at 7 mA. Fig. 9 plots the measured phase noise for the test VCO with the carrier frequency of 900 MHz after LO chain.

The VCO achieves −123 dBc/Hz and −145 dBc/Hz at 400 kHz and 3 MHz offset frequencies from the carrier, respectively. Phase noise at 400 kHz offset frequency is important for Tx spectrum mask and phase noise at 3 MHz offset frequency is important for single tone test for Rx mode. The measured frequency tuning range and phase noise performances satisfy all requirements for Quad-band GSM/EDGE and WCDMA standard. Table 1 shows the summary of the measurement results compared to those of other low phase noise VCOs.

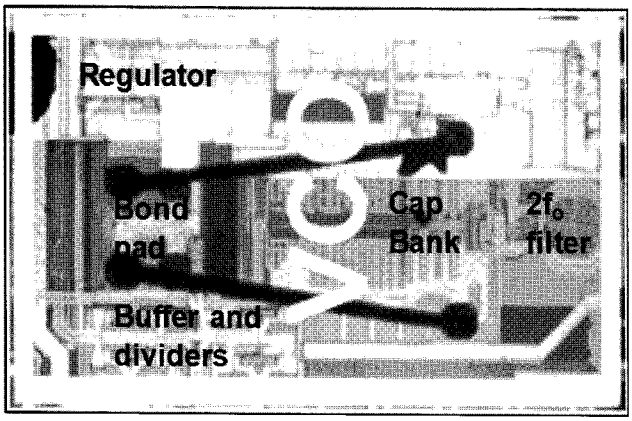

Fig. 8. Microphotograph of the VCO.

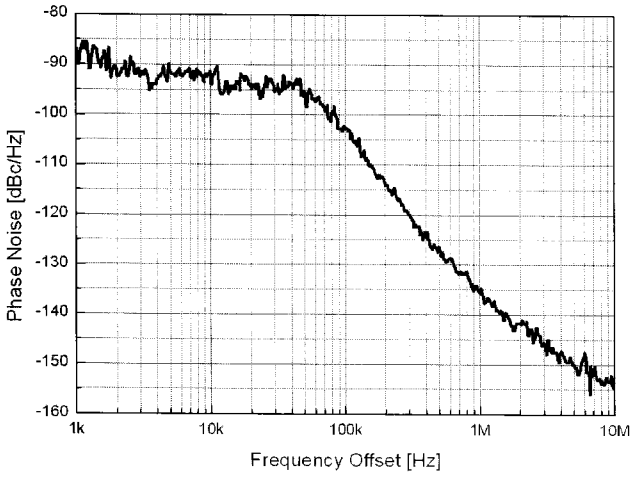

Fig. 9. Measured phase noise of the proposed VCO at 900 MHz carrier frequency.

Table 1. VCO performance summary and comparison.

VCO	Tech.	Freq. [GHz]	Power [mW]	P/N [dBc/Hz]	FOM
[11]	0.35 um Bi-CMOS	1.91	10	−121 @600 KHz	−181.1
[12]	0.35 um Bi-CMOS	5.6	13.5	−117 @1 MHz	−180.7
[13]	0.13 um CMOS	3.0~5.6	2	−114.5 @1 MHz	−186.5
[14]	0.35 um CMOS	2.19	12.6	−139 @3 MHz	−185.3
This Work	0.13 um CMOS	3.17~4.49	12.6	−145 @3 MHz	−183.5

A normalized Figure Of Merit(FOM) has been defined[10] to compare the VCO performance with other VCOs as

$$FOM = L(\triangle\omega)\left[\frac{dBC}{Hz}\right] + 10\log\left(\frac{P_{DC}}{1mW}\right) - 20\log\left(\frac{\omega_0}{\triangle\omega}\right) \quad (5)$$

where $L(\Delta\omega)$ is the total single-sideband phase-noise spectral density at an offset frequency $\Delta\omega$, P_{DC} is total VCO power consumption, and ω_0 is the frequency of oscillation. The calculated FOM of this VCO is about −183.5 dBc/Hz at 3 MHz offset. Considering the wide tuning range of 34 %, this FOM is quite comparable to the previously published results.

Ⅳ. Conclusions

In this work, a low phase noise, wideband CMOS VCO for a Quad-band GSM/EDGE and WCDMA single-chip transceiver has been presented. Circuit design procedures and techniques for achieving a good trade-off among important specifications, phase noise, power consumption, modulation performance, and chip area efficiency are proposed. An NMOS-only structure and high Q bond wire inductor are adopted for enough phase noise margin, wide frequency tunability, and chip area efficiency, and programmable 3-bit bias resistors are used for a trade-off between phase noise and power consumption. A noise filtering technique is also used to avoid phase noise degradation. The design and manu-

facturing has been achieved with 0.13 μm CMOS process. The experimental results show that the tuning range is from 3.17 GHz to 4.49 GHz. The phase noise performances of the VCO are -123 dBc/Hz at 400 kHz offset and -145 dBc/Hz at 3 MHz offset(measured from a 900 MHz carrier after LO chain), exceeding the most stringent GSM Tx/Rx specification while simultaneously achieving 34 % tuning range. The FOM of -183.5 dBc/Hz confirms that the good phase noise/ power consumption trade-off is achieved.

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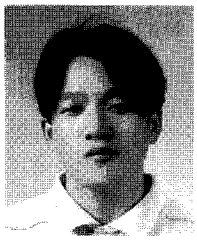

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