Investigation of Frequency Dependent Sensitivity of Noise Figure on Device Parameters in 65 nm CMOS

MinSuk Koo, Hakchul Jung, HeeSauk Jhon, Byung-Gook Park, Jong Duk Lee, and Hyungcheol Shin

***Abstract*—We have investigated the noise sensitivity of low noise amplifier (LNA) at different frequency. This noise sensitivity analysis provides insights about noise parameters and it is very beneficial for making appropriate design trade-offs. From this work, the circuit designer can choose the adequate noise parameters tolerances.**

***Index Terms*—Noise sensitivity, CMOS, low noise amplifier, LNA, optimization**

I. INTRODUCTION

RF circuit design is difficult in advanced technology because of process variability and lack of accuracy of model. Therefore, we should take such unpredictable process variations into account during the circuit design stage in deep submicron technology. Noise sensitivity analysis could provide the design approach to reduce these variations for better circuit design. A low-noise Amplifier (LNA) is one of the most critical circuit blocks in a wireless transceiver. As the first stage in the receiver architecture, noise figure of LNA dominates overall noise performance of the system [1]. Therefore, we analyzed frequency dependent sensitivity of noise figure of LNA. For more accuracy, we adopted small signal equivalent circuit with gate-to-drain capacitance consideration and analytic noise model of MOSFET. This work is done by measurement data of 65 nm CMOS devices.

Manuscript received Mar. 2, 2009; revised Mar. 11, 2009.
Inter-University Semiconductor Research Center (ISRC), and School of Electrical Engineering, Seoul National University, Seoul, Korea
E-mail : korcom33@gmail.com

II. NOISE FIGURE OF LNAS

Conventional LNAs schematic is shown in Fig. 1. And small signal equivalent circuit with C_{gd} is shown in Fig. 2.

As the technology is scaled down, the effect of the C_{gd} is not ignored any more. From that equivalent circuit, noise figure equation can be derived as below [2]. The channel thermal noise, S_{id}, is analytically modeled and predicts the measured channel thermal noise well [3,4].

$$NF-1=\frac{R_1}{R_S}+\frac{S_{id1}}{4kT}\frac{(R_S+R_1)^2}{R_S}\left(\frac{f}{f_{T1}}\right)^2+\frac{S_{id2}}{4kT}(4R_S)\left(\frac{f}{f_{T1}}\right)^2\left(\frac{f}{f_{T2}}\right)^2 \quad (1)$$

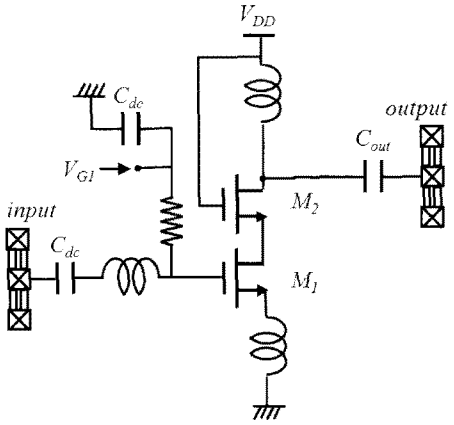


Fig. 1. Schematic of a conventional cascode LNA.

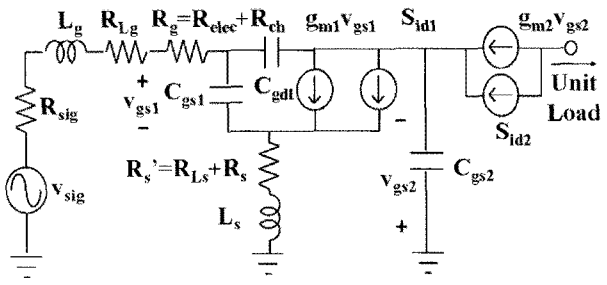


Fig. 2. Small signal equivalent circuit of cascode LNA with C_{gd}.

$$NF-1=\frac{R_1}{R_{sig}}+4R_{sig}\frac{\alpha}{\gamma}\frac{S_{id1}}{4kT}+4R_{sig}\frac{\beta}{\gamma}\frac{S_{id2}}{4kT} \quad (2)$$

$$S_{id}=4kT_0\left(\frac{m}{(V_{GT}-V_0)}+\frac{mV_0}{V_{GT}(V_{GT}-V_0)}\right)I_D \quad (3)$$

where $V_{GT}=V_{GS}-V_{TH}$, $V_O=I_{DS}/WC_{ox}v_{sat}$, and m is the body-effect coefficient. R_1 is sum of parasitic resistance of gate and source inductor (R_{Lg}, R_s), gate electrode resistance (R_{elec}) and source resistance (R_s). The equation (1) is extended to equation (2) with C_{gd} consideration. And parameters such as α, β and γ are as shown below where $C_{gs}' = C_{gs1} + C_{gs2}$ and $R_{tot} = R_1 + R_{sig}$ [2].

$$\alpha=\frac{\left[(1+\frac{C_{gd1}}{C_{gs1}})R_{tot}\right]^2}{\left[(\frac{g_{m1}L_s}{C_{gs1}}+R_{tot})+\frac{C_{gd1}}{C_{gs1}}(1+\frac{g_{m1}}{g_{m2}})R_{tot}\right]^2+\left[\omega L_s(1+\frac{C_{gd1}}{C_{gs1}}g_{m1}R_{tot})+\frac{\omega}{g_{m2}}(C_{gs2}(\frac{g_{m1}L_s}{C_{gs1}}+R_{tot})+\frac{C_{gd1}}{C_{gs1}}(g_{m1}(L_g+L_s)))\right]^2} \quad (4)$$

$$\beta=\frac{\left(-\omega C_{gs2}\left(-\frac{1}{\omega C_{gs1}}+\omega L_g\right)+\omega C_{gd1}\left(\frac{g_{m1}R_{tot}}{\omega C_{gs1}}\right)\right)^2+\omega^2\left(C_{gs2}(\frac{g_{m1}L_s}{C_{gs1}}+R_{tot})+\frac{C_{gd1}}{C_{gs1}}\left(g_{m1}L_g+C_{gs}'R_{tot}\right)\right)^2}{\left(-\omega C_{gs2}\left(-\frac{1}{\omega C_{gs1}}+\omega L_g\right)+g_{m2}(\frac{g_{m1}L_s}{C_{gs1}}+R_{tot})+\frac{C_{gd1}}{C_{gs1}}\left(\frac{1-\omega^2 g_{m1}g_{m2}L_gL_s+(g_{m1}+g_{m2})R_{tot}}{-\omega^2 L_g C_{gs}'}\right)\right)^2+\omega^2\left(C_{gs2}(\frac{g_{m1}L_s}{C_{gs1}}+R_{tot})+\frac{C_{gd1}}{C_{gs1}}\left(g_{m1}L_g+C_{gs}'R_{tot}\right)\right)^2} \quad (5)$$

$$\gamma=\left(\frac{g_{m1}}{\omega[C_{gs1}+C_{gd1}(1+\frac{g_{m1}}{g_{m2}})]}\right)^2 \quad (6)$$

There are two noise terms with different noise sources; resistor source and transistor source [4]. Therefore, we could classify parameters as two noise sources. Q-factor and L_g are related to resistor noise term and V_{th}, width of device, C_{ox}, v_{sat} and drain current are related to transistor noise term. And other parameters such as C_{gs}, C_{gd}, g_m are multiplied with noise terms. Since there are dominant noise terms at different frequency, we could obtain the sensitivity of these parameters. As frequency increases, $1/\omega^2C_{gs}$ decreases and L_g, L_s and it's parasitic resistance get smaller. Therefore, resistor noise term decreases while the transistor noise term increase as f/f_t increases in simplified noise figure equation (1). As a result, parameters related to transistor noise term would be more sensitive than others at high frequency while parameters related to resistor noise term are more sensitive at low frequency [5].

III. Optimization with FoM and Sensitivity Analysis

At higher frequency, we generally use smaller device width. Since the noise sensitivity varies as width of device changes, we should first determine the optimum width of device and bias point of LNA for more similarity to real design situation. The figure of merit (FoM) represented as below is index of performance of LNA [6].

$$FoM_{LNA}=\frac{G\cdot f}{(NF-1)\cdot P} \quad (7)$$

where G is signal power gain in absolute unit, NF is noise factor in absolute unit, P is power dissipation, and f is operation frequency. We can obtain the FoM of LNA using following gain equation and FoM optimization for 17 GHz is shown as Fig. 3-(a), (b) where f_{T1} and f_{T2} are cut-off frequency of M_1 and M_2 transistor.

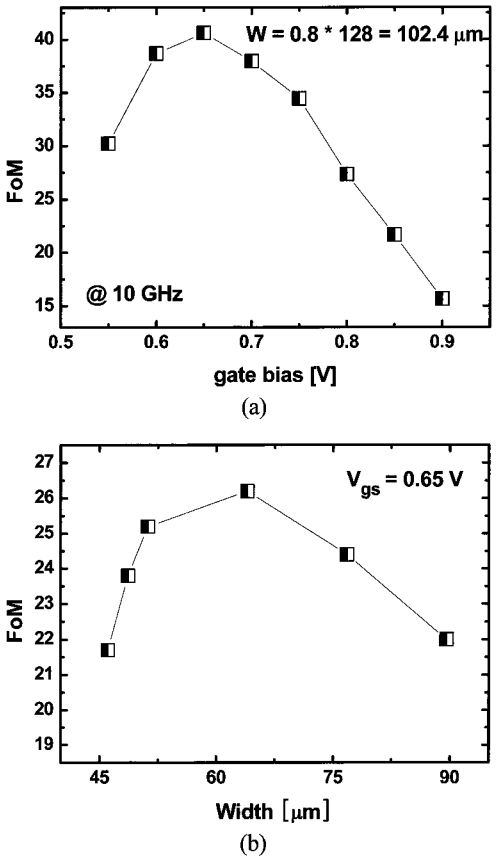
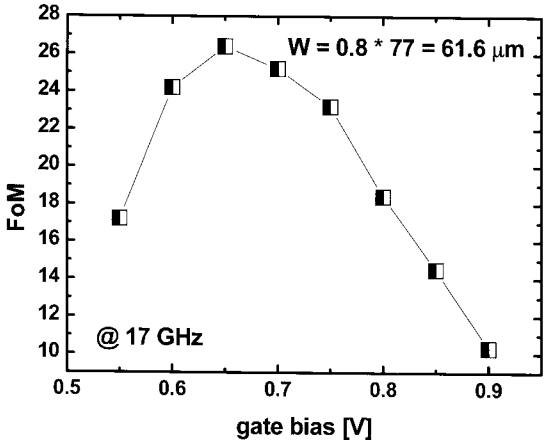
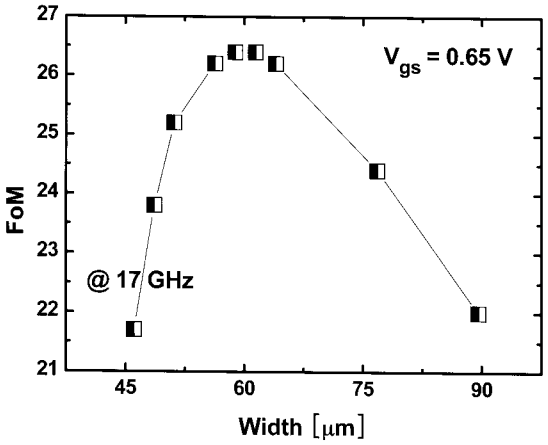


Fig. 3-1. FoM Optimization of LNAs (a) width optimization and (b) gate bias optimization for 10 GHz.

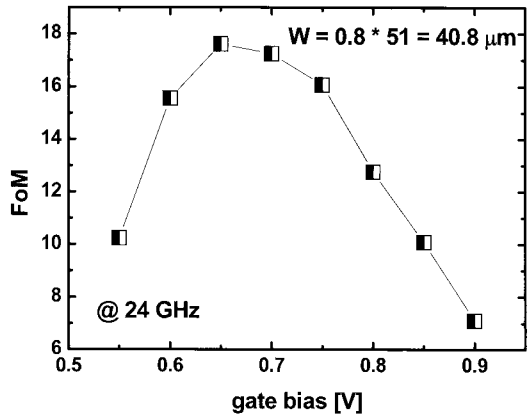


(a)

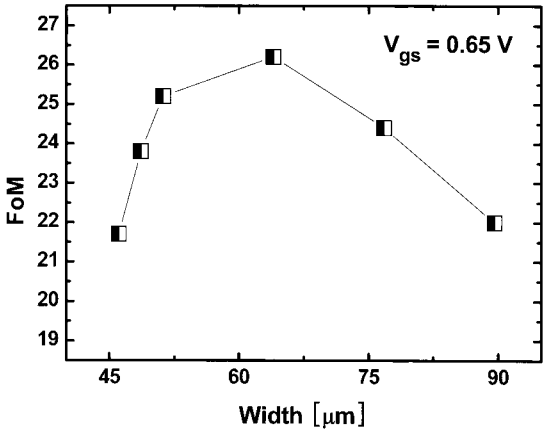


(b)

Fig. 3-2. FoM Optimization of LNAs (a) width optimization and (b) gate bias optimization for 17 GHz.



(a)



(b)

Fig. 3-3. FoM Optimization of LNAs (a) width optimization and (b) gate bias optimization for 24 GHz.

$$G = \frac{1}{4}\left(\frac{f_{T1}}{f}\right)^2 \Big/ \left(1+\left(\frac{f}{f_{T2}}\right)^2\right) \quad (8)$$

We can also obtain the FoM of LNA for 10 GHz and 24 GHz for comparison. Optimum device width of 102.4 μm for 10 GHz, 61.6 μm for 17 GHz and 40.8 μm for 24 GHz were obtained at V_{gs} = 0.65 V. Fig. 4 shows the effect of S_{id} on noise figure. The ±50% variation of S_{id1} makes deviation of 0.35 dB at 10 GHz, 0.56 dB at 17 GHz, 0.76 dB at 24 GHz. At higher frequency, channel thermal noise is sensitive on noise figure and S_{id1} is more sensitive than S_{id2} for all frequency range. However, the effect of S_{id2} on noise figure is increased more rapidly than that of S_{id1}.

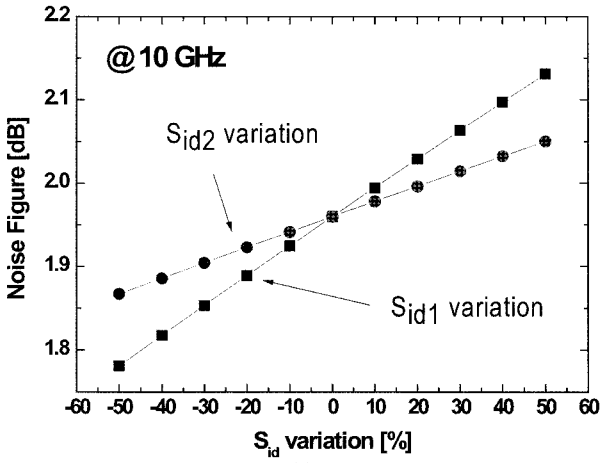
To invest frequency dependent sensitivity of other design parameters, all parameters have been changed by 10% from the norminal value and see the variation of total noise figure.

Fig. 5-(a), (b), (c) shows deviations of noise figure by 10% of change of each parameter. Gate inductor, Q factor, Cgs1, Cgd1, Cgs2, gm1 and gm2 are considered as important parameters on noise figure.

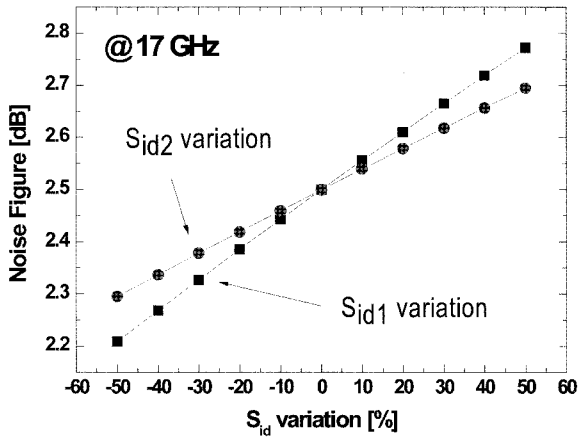
The norminal values of noise figure are 1.96 dB at 10 GHz, 2.5 dB at 17 GHz, 3.58 dB at 24 GHz. These results provide which parameter should be considered firstly for noise tolerable design.

As we expected, parameters related to resistor noise term such as L_g and Q-factor are more sensitive at lower frequency. And parameters multiplied with noise terms such as C_{gs}, C_{gd} and g_m are more sensitive at higher frequency.

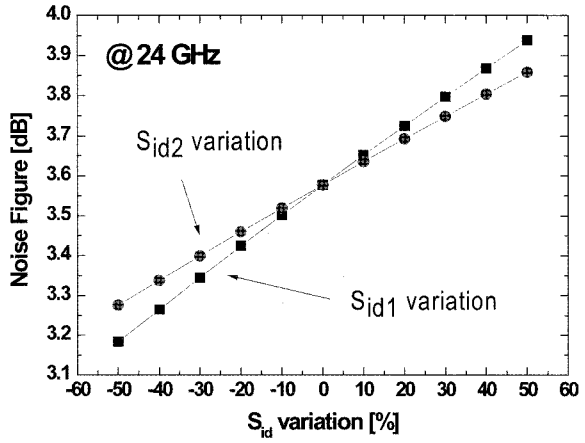
From these results, it is found that parameters which are extracted from DC model such as V_{th}, I_D and g_m are important for all frequency and should be modeled carefully for accurate noise expectation. And parameters related to resistor noise term are important at low frequency while parameters multiplied with transistor noise term are important at high frequency.



(a)

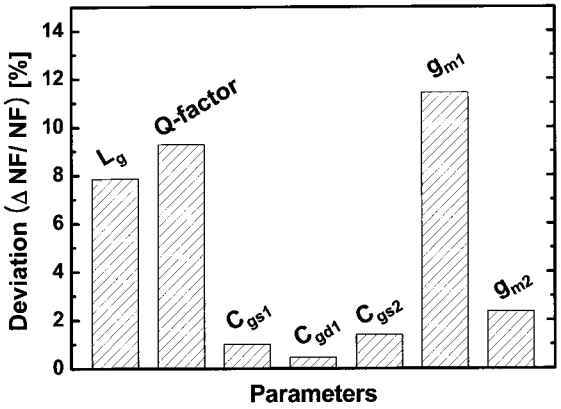


(b)

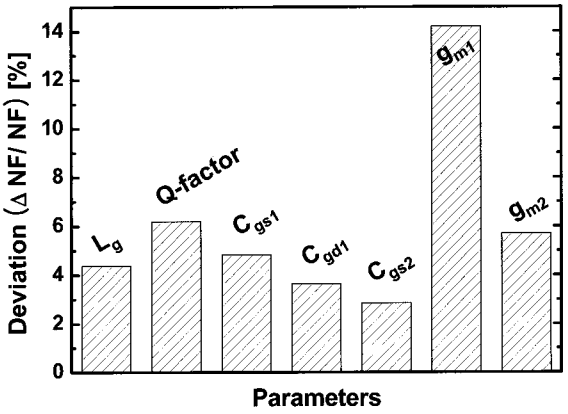


(c)

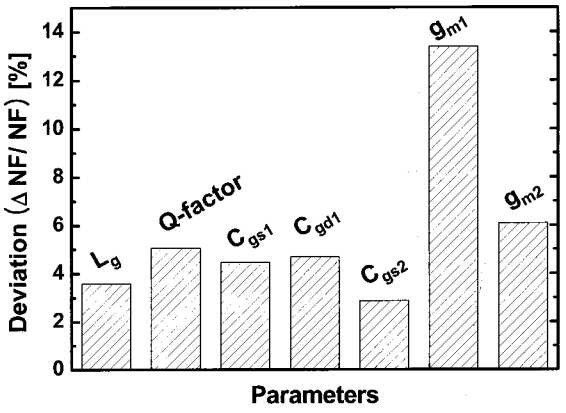
Fig. 4. NF deviation vs. parameters for S_{id} at (a) 10 GHz, (b) 17 GHz and (c) 24 GHz.



(a)



(b)



(c)

Fig. 5. NF deviation versus parameters for (a) 10GHz, (b) 17GHz and (c) 24 GHz.

IV. CONCLUSIONS

In this paper, we designed LNA with FoM optimization and analyze noise sensitivity of LNAs for frequency. Parameters extracted from DC model such as V_{th}, I_D and g_m should be accurate to reduce the unpredictable variation for all frequency. And parameters related to resistor noise term are more sensitive at low frequency while parameters multiplied with transistor noise term are more sensitive at high frequency. From this work, circuit designers can determine which parameters are important and focused on. In addition, parasitics which effect on important parameter should be considered firstly.

ACKNOWLEDGMENTS

This work was supported by Samsung Electronics Ltd., and Inter-University Semiconductor Research Center (ISRC).

REFERENCES

[1] B. Razavi, "RF microelectronics," *Prentice Hall*, USA, 1998.

[2] H. Jung, H. Jhon, I. Song, M. Koo, and H. Shin, "Design optimization of a 10 GHz Low Noise Amplifier with gate drain capacitance consideration in 65 nm CMOS Technology," *IEEE International Conference on Solid State and Integrted Circuit Technology*, pp.1480-1483, 2008.

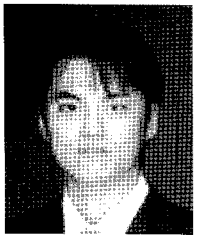
[3] J. Jeon, J. Lee, C. Park, J Yoon, H. Lee, H. Oh, B.-G. Park, and H. Shin, "Accurate Channel Thermal Noise Modeling in BSIM4," *International Conference on Solid State Devices and Materials*, pp. 490-491, 2008.

[4] J. Jeon, J.D. Lee, B.-G. Park, and H. Shin, "Analytical noise parameter model of short-channel RF MOSFETs," *International Conference on Solid State Devices and Materials*, pp. 490-491, 2008.

[5] M. Koo, I. Song, J. Jeon, H. Jhon, and H. Shin, *Korean Conference on Semiconductors*, p.108 (2008).

[6] Saman Asgaran, M. Jamal Deen, and Chih-Hung Chen, *IEEE Transaction on Circuit and Systems*, vol.54, no.3, (2007).

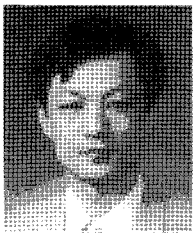
MinSuk Koo was born in Korea on July 15, 1983. He received B.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2007. He is currently pursuing the M.S. degree in Seoul National University, Seoul, Korea. His major interest is design of low noise amplifier and its noise characteristics.



Hakchul Jung received the B.S, degree in electrical engineering from Korea University, Seoul, Korea. He is currently pursuing the M.S. degree in the same department from Seoul National University, Seoul, Korea. His research interests include RF CMOS integrated circuit design and modeling.

Hee Sauk Jhon (S'08) received the B.A degree in electronic engineering from the University of Kangwoon, Seoul, Korea in 2001. He received the M.A degree in electrical and electronic engineering from the University of Yonsei, Seoul, Korea in 2004. He is currently working toward Ph.D. degree in the department of electrical engineering, Seoul National University, Gwanak-gu, Seoul, Korea.

His research interests include the design of low cost and power efficient RFICs and the modeling of Si-based active/passive devices.

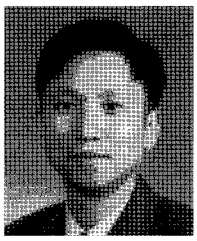


Byung-Gook Park received his B.S. and M.S. degrees in Electronics Engineering from Seoul National University (SNU) in 1982 and 1984, respectively, and his Ph. D. degree in Electrical Engineering from Stanford University in 1990. From 1990 to 1993, he worked at the AT&T Bell Laboratories, where he contributed to the development of 0.1 micron CMOS and its characterization. From 1993 to 1994, he was with Texas Instruments, developing 0.25 micron CMOS. In 1994, he joined SNU as an assistant professor in the School of Electrical Engineering (SoEE), where he is currently a professor. In 2002, he worked at Stanford University as a visiting professor, on his sabbatical leave from SNU. He has been leading the Inter-university Semiconductor Research Center (ISRC) at SNU as the director from June 2008.

His current research interests include the design and fabrication of nanoscale CMOS, flash memories, silicon quantum devices and organic thin film transistors. He has authored and co-authored over 580 research papers in journals and conferences, and currently holds 34 Korean and 7 U.S. patents. He has served as a committee member on several international conferences, including Microprocesses and Nanotechnology, IEEE International Electron Devices Meeting, International Conference on Solid State Devices and Materials, and IEEE Silicon Nanoelectronics Workshop (technical program chair in 2005, general chair in 2007). He is currently serving as an executive director of Institute of Electronics Engineers of Korea (IEEK) and the board member of IEEE Seoul Section. He received "Best Teacher" Award from SoEE in 1997, Doyeon Award for Creative Research from ISRC in 2003, Haedong Paper Award from IEEK in 2005, and Educational Award from College of Engineering, SNU, in 2006.

Jong Duk Lee was born in Youngchun, Kyungpook, Korea. He received the B.S. degree in physics from Seoul National University in 1966. He received the Ph.D. degree from the Department of Physics at the University of North Carolina at Chapel Hill in 1975. He served at the Military Communication School as a ROTC officer from 1966 to 1968. He then worked at the Engineering College of Seoul National University as a teaching assistant in the Department of Applied Physics until 1970. He was an Assistant Professor in the Department of Electronics Engineering at Kyungpook National University from 1975 to 1978. In 1978, he studied microelectric technology in HP-ICL at Palo Alto, CA, USA, and soon afterward worked for the Korea Institute of Electronic Technology (KIET) as the director of the semiconductor division. He established the KIET Kumi Facility and introduced the first polysilicon gate technology in Korea by developing 4K SRAM, 32K and 64K Mask ROM's, and one-chip 8-bit microcomputer.

In July 1983, he moved to the Department of Electronics Engineering of Seoul National University, which has been merged to School of Electrical Engineering in 1992, where he is now a Professor. He started to establish the Inter-University Semiconductor Research Center (ISRC) in 1985, and served as the director from 1987 to 1989. He served as the chairman of the Electronics Engineering Department from 1994 to 1996. He worked for Samsung SDI Co., Ltd. as the Head of Display R&D Center for a year on the leave of SNU in 1996. He was the member of the steering committee for IVMC(International Vacuum Microelectronics Conference) from 1997-2001 and KCS(Korean Conference on Semiconductors) from 1998-2008. He was the conference chairman of IVMC'97 and KCS'98 who led the IVMC'97 and the KCS'98 successfully. He was also the member of IEDM(International Electron Devices Meeting) Subcommittee on Detectors, Sensors and Displays operated by IEEE Electron Devices Society from 1998 to 1999, he has been elected to the first president of the Korean Information Display Society in June 1999 to serve until Dec. 31, 2001. He concentrated his study on the image sensors such as Vidicon type, MOS type, and also CCD to help Samsung SDI Co. and Samsung Electronics Co. since 1985. His current research interests include sub 0.1 um CMOS structure and technology, CMOS image sensors and FED(Field Emission Display), and organic LEDs and TFTs. He published more than 221 papers in the journals such as IEEE-ED and EDL, Journal of Vacuum Science and Technology, Applied Physics and Journal of Electrochemical Society, including 160 SCI journal papers. He presented more than 361 papers including 213 international conference papers. He also registered 12 US, 4 Japanese, and 28 Korean patents. Now he is a member of IEEE, ECS, AVS, SID, KPS, KVS, IEEK, and KSS.



Hyungcheol Shin received the B.S. (*magna cum laude*) and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1985 and 1987, respectively, and the Ph.D. degree in electrical engineering from the University of California, Berkeley, in 1993. From 1994 to 1996, he was a Senior Device Engineer with Motorola Advanced Custom Technologies. In 1996, he was with the Department of Electrical Engineering and Computer Sciences, Korea Advanced Institute of Science and Technology (KAIST), Daejeon. During his sabbatical leave from 2001 to 2002, he was a Staff Scientist with Berkana Wireless, Inc., San Jose, CA, where he was in charge of CMOS RF modeling. Since 2003, he has been with the School of Electrical Engineering and Computer Science, Seoul National University. He has published over 300 technical papers in international journals and conference proceedings. He also wrote a chapter in a Japanese book on plasma charging damage and semiconductor device physics.

His current research interests include Nano CMOS, Flash Memory, DRAM cell transistors, CMOS RF, and noise. Prof. Shin was a committee member of the International Electron Devices Meeting. He also has served as a committee member of several international conferences, including the International Workshop on Compact Modeling, and as a committee member of the IEEE EDS Graduate Student Fellowship. He is a Lifetime Member of the Institute of Electronics Engineers of Korea (IEEK). He received the Second Best Paper Award from the American Vacuum Society in 1991, the Excellent Teaching Award from the Department of Electrical Engineering and Computer Sciences, KAIST, in 1998, The Haedong Paper Award from IEEK in 1999, and the Excellent Teaching Award from Seoul National University in 2005 and 2007. He is listed in *Who's Who in the World.*