Design of 32 bit Parallel Processor Core for High Energy Efficiency using Instruction-Levels Dynamic Voltage Scaling Technique

Yil Suk Yang*, Tae Moon Roh*, Soon il Yeo*, Woo H. Kwon**, and Jongdae Kim*

Abstract—**This paper describes design of high energy efficiency 32 bit parallel processor core using instruction-levels data gating and dynamic voltage scaling (DVS) techniques. We present instruction-levels data gating technique. We can control activation and switching activity of the function units in the proposed data technique. We present instruction-levels DVS technique without using DC-DC converter and voltage scheduler controlled by the operation system. We can control powers of the function units in the proposed DVS technique. The proposed instruction-levels DVS technique has the simple architecture than complicated DVS which is DC-DC converter and voltage scheduler controlled by the operation system and a hardware implementation is very easy. But, the energy efficiency of the proposed instruction-levels DVS technique having dual-power supply is similar to the complicated DVS which is DC-DC converter and voltage scheduler controlled by the operation system. We simulate the circuit simulation for running test program using Spectra. We selected reduced power supply to 0.667 times of the supplied power supply. The energy efficiency of the proposed 32 bit parallel processor core using instruction-levels data gating and DVS techniques can improve about 88.4% than that of the 32 bit parallel processor core without using those. The designed high energy efficiency 32 bit parallel processor core can utilize as the coprocessor processing massive data at high speed.**

Index Terms—**Parallel processor core, energy efficiency, dynamic voltage scaling technique, data gating technique**

I. INTRODUCTION

The digital SOC has the higher density, the higher performance and the more multi-function due to the convergences of the digital technology. Hot issues which are principal in the current digital SOC are flexibility, scalability and high energy efficiency. The energy efficiency is obtained by dividing the capability of a processor to process data by consumption power and can be expressed in terms of MIPS/mW or MOPS/mW.

A parallel architecture is the one of the candidates in order to satisfy both high performance and low power consumption. The parallel architecture can be categorized into a single instruction multiple data (SIMD) architecture and a multiple instruction multiple data (MIMD) architecture. SIMD and MIMD architecture make use of the data level parallelism. Recently, the parallel architecture in digital SOC is required because of the low power and the high operation computing capability. The processor core performing data processing is the core circuit in parallel processor. Parallel processor is composed of the array of the processor core. Parallel processors using SIMD or MIMD architecture are mainly used for the multimedia data processing in which the calculation performance is much required in the portable devices.

The most effective method of low power consumption drops the power supply voltage V_{DD}. But, the delay time

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increased and the performance decreased by reducing power supply voltage in general. Low power consumption techniques have been proposed. Clock gating, frequency gating, and multiple power technique has been reported. The clustered voltage scaling (CVS), extended CVS, and the variable supply-voltage (VS) scheme have the multiple power supply voltages structure [1]. It is that the scalable power supply structure prefers to the constant supply structure in order to high energy efficiency [1]. When the required performance of the target system is lower than the maximum performance, power supply voltage can be dynamically reduced to the lowest possible extent that ensures a proper operation of the system by using the DVS technique [2-8]. The DVS technique has dynamically varying power supply voltage according to the workload. The power in the DVS technique transits the power supply voltage to the reduced power supply voltage dependent on workload. Therefore, the workload prediction and detection are to the essential in DVS technique. Many workload prediction algorithms for the high energy efficiency have been published [4,5]. The reduced power supply V_{DDL} is determined to the workload, process, and delay time. The minimum reduced power supply voltage V_{DDL} should be scaled to approximately 0.3 times of the power supply V_{DD}. But, the reduced power supply V_{DDL} in reported DVS-based processors is commonly 0.5 times of the power supply V_{DD}. And energy efficiency in published DVS-based processors can be improved about 20% to 93% using DC-DC converter and voltage scheduler controlled by the operation system [2-8]. The power-delay and energy-delay product are the very important factors in DVS technique because the speed penalties due to lowering voltage can be occurred. The reduced voltage can be selected between 1.5 times of the threshold voltage and 3 times of the threshold voltage for the optimization of the delay and performance in DVS technique and the energy-delay product is minimum in the energy-power supply V_{DD} plot when the power supply V_{DD} is equal to the 2 times of the threshold voltage [9,10]. The Intel XScale [6], the IBM PowerPC [7], and the Transmeta Crusoe [8] are commercial processors using DVS technique. The DC-DC converter and the voltage scheduler controlled by the operation system are used in the commercial processors using DVS technique.

In this paper, we describe design and circuit simulation of the high energy efficiency 32 bit parallel processor core. We present instruction-levels data gating and DVS techniques for the high energy efficiency 32 bit parallel processor core. We design and circuit simulation the 32 bit parallel processor core using data gating and the DVS technique at the instruction levels in order to the high performance and the low power consumption.

II. Design of the Proposed Processor Core using Instruction-Levels Data Gating and DVS Techniques

Fig. 1 shows a block diagram of the proposed 32 bit parallel processor core applying the instruction-levels data gating technique. The proposed 32 bit parallel processor core is composed of the instruction register, instruction decoder, register files, load/store unit, and several function units. The power supply of the proposed 32 bit parallel processor core has fixed-voltage supplied power supply voltage 1.2 V. The several function units are composed of the 32 bit adder, 16 bit multiplier, and 32 bit shifter. Each function units has the enable gating signal in order to reduce the power consumption and each enable gating signal of the several function units has role in control the switch activity of the function units for the low power consumption. The instruction decoder produces enable gating signals ADDEN, SHEN, and MULEN for cont-

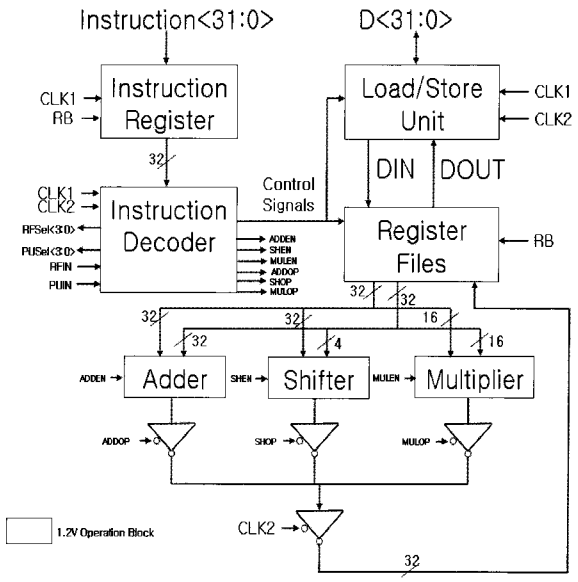

Fig. 1. Block diagram of the proposed 32 bit processor core applying the instruction-levels data gating technique. The power supply of the proposed 32 bit processor core has fixed-voltage 1.2 V.

rolling 32 bit and 16 bit function units.

Fig. 2 shows a block diagram of the proposed 32 bit parallel processor core applying the instruction-levels data gating and the DVS technique. The proposed 32 bit processor core is composed of the instruction register, instruction decoder, register files, load/store unit, function units, and several dynamic voltages scaling power supply (DVSPS). The proposed DVS technique is not needed voltage scheduler and DC-DC converter because instructtions are determined to the voltage level. The proposed 32 bit parallel processor core has the DVSPS and the proposed DVSPS circuit supplies the entirely function units of the 32 bit parallel processor core to the power supply voltage according to the instructions.

The output power of DVSPS transits the supplied power supply V_{DD} to the reduced power supply V_{DDL} according to the instruction. The power supplies of the 32 bit parallel processor core have 2 voltage levels, supplied power supply V_{DD} and the reduced power supply V_{DDL}. The reduced power supply voltage V_{DDL} is about 60 ~ 70% that of power supply voltage in this paper. The power supply of the instruction register, instruction decoder, register files, and load/store unit has fixed-voltage supplied power supply 1.2 V. The power supplies of the several function units and several DVSPS have 2 voltage levels, supplied power supply 1.2 V and the reduced power supply 0.8 V. Each function units has the enable gating signal and DVSPS in order to reduce the power consumption, respectively. The control signals ADDEN, SHEN, and MULEN control the power of the function units, respectively and the proposed DVSPS circuit supplies the entirely function units to the power supply voltage according to the control input signal PMCNT. The control input signal PMCNT of DVSPS is connected to the enable gating signals of the function units, respectively. As the enable gating signals of the function units are HIGH, the power of the function units is the supplied power supply voltage V_{DD}. But, as the enable signals of the function units are LOW, the power of the function units is the reduced power supply voltage V_{DDL}. The power of function units transits the supplied power supply V_{DD} to the reduced power supply V_{DDL} according to the instructions. Fig. 3 shows the block diagram and operation of the proposed DVSPS circuit.

We proposed the data gating technique at the instruction-levels for low power consumption. We can select only one function unit of the function units in the processing unit according to the enable signals using the proposed data gating. The selected function unit only executes the real data according to the instructions. All input data of the non-selected function units have zero regardless of the instruction so they do not activation and switching activity.

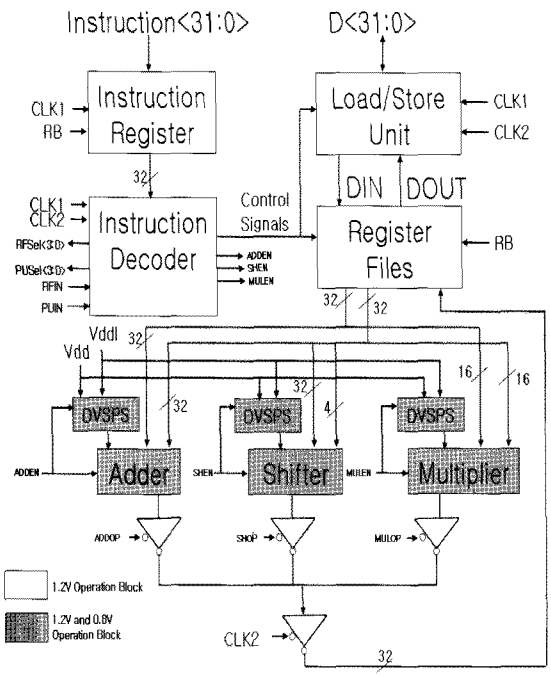

Fig. 2. Block diagram of the proposed 32 bit processor core applying the instruction-levels data gating and DVS techniques. The power supplies of the proposed 32 bit processor core have 2 voltage levels, 1.2 V and 0.8 V.

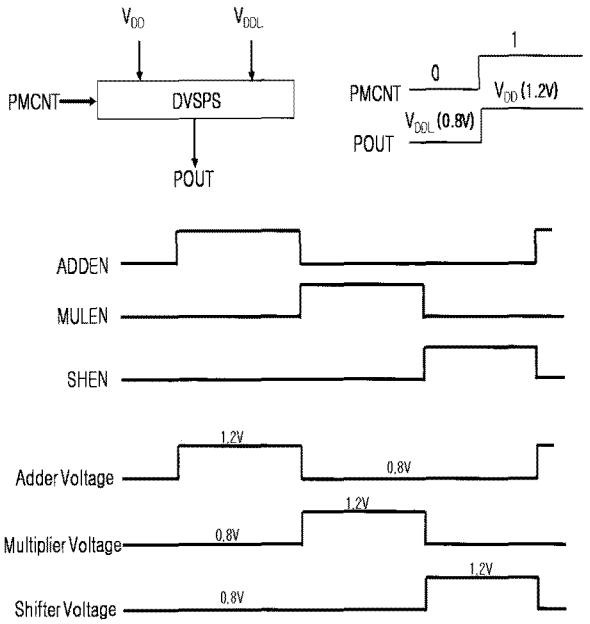

Fig. 3. Block diagram of the DVSPS circuit and operation of the proposed DVSPS circuit.

We proposed instruction-levels dual voltage- levels DVS technique without voltage fluctuations in the power rails and level converter or level shifter circuit between power supply V_{DD} blocks and the reduced power supply V_{DDL} blocks. The power consumption of the proposed 32 bit parallel processor core decreases using instruction-levels data gating and dual voltage-levels DVS techniques. Therefore, the energy efficiency of the proposed 32 bit parallel processor core can be maximized.

We applied the data gating and DVS technique to the proposed 32 bit parallel processor core at the instruction-levels for high energy efficiency. The power consumption of the proposed 32 bit parallel processor core d decreases using data gating and the DVS techniques.

III. Simulation Results

We simulated the power and circuit simulation for running test program using Spectra with layout extraction data which does not include PAD. We simulated power simulation with varying to the reduced voltage using Spectra. The reduced voltage can be selected between 1.5 times of the threshold voltage and 3 times of the threshold voltage for the optimization of the delay and performance in DVS technique. We used 0.4 V threshold voltage process in this paper. Fig. 4 shows the normalized power consumption of the designed 32 bit parallel processor core in condition that the power supply is 1.2 V and the reduced voltage is varied. X-axis represents reduced voltage and Y-axis represents normalized power consumption. As shown Fig. 4, the normalized power consumption has minimum value as the reduced voltage has 0.8 V. So, we selected 0.8 V to the optimum reduce voltage in this paper.

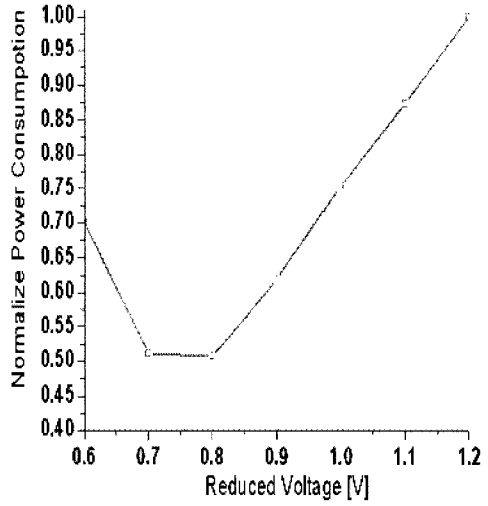

Fig. 4. Simulation result of the normalized power consumption of the designed 32 bit parallel processor core varying to the reduced voltage.

We simulated the circuit simulation for running test program using Spectra with layout extraction data which does not include PAD. Fig. 5 shows the circuit simulation results of the designed 32 bit parallel processor core. The power supply V_{DD} is the 1.2 V and the reduced power supply V_{DDL} is 0.8 V. The 32 bit adder power is the reduced power supply voltage 0.8 V V_{DDL} during 32 bit adder is non-activation. But, the 32 bit adder power is the supplied power voltage 1.2 V V_{DD} during adder is activetion. Therefore, the 32 bit adder power transits the reduced power supply voltage 0.8 V V_{DDL} to the supplied power voltage 1.2 V V_{DD} according to the ADDEREN control signal.

Table 1 shows the normalized energy efficiency of the designed 32 bit parallel processor core with the data gating and DVS techniques. The Case 1 represents the designed 32 bit parallel processor core with the instruction-levels

Table 1. The normalized energy efficiency of the designed 32 bit Parallel processor core with the data gating and DVS techniques.

	Power Supply	Operation Frequency	Normalized Power Consumption	Performance	Normalized Energy Efficiency
Case 1	1.2V	100 MHz	1mW	100 MIPS	100 MIPS/mW
Case 2	1.2V/ 0.8V	100 MHz	0.531mW	100 MIPS	188.4 MIPS/mW

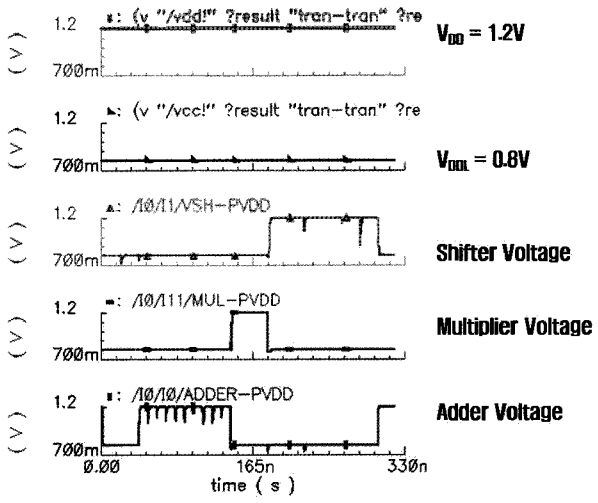

Fig. 5. Circuit simulation result of the designed 32 bit parallel processor core.

data gating techniques. The Case 2 represents the designed 32 bit parallel processor core with the instruction-levels data gating and DVS techniques. The power supply of Case 1 is 1.2 V. The power supplies of Case 2 are 1.2 V and 0.8 V. The operation frequency of Case 1 and Case 2 is 100 MHz. The normalized energy efficiency of Case 1 is 100 MIPS/mW and that of Case 2 is 188.4 MIPS/mW. The energy efficiency of the proposed 32 bit parallel processor core using instruction-levels data gating and DVS techniques can improve about 88.4% than that of the 32 bit processing unit without using instruction-levels data gating and DVS techniques.

IV. CONCLUSIONS

This paper describes design and simulation of 32 bit parallel processor core at the instruction levels for high energy efficiency. We presented an instruction-levels data gating technique and dynamic voltage scaling technique for the high energy efficiency 32 bit parallel processor core. We proposed data gating technique at the instruction levels. We can select only one function unit of the function units in the processing unit according to the enable signals using the proposed data gating. The selected function unit only executes the real data according to the instructions. All input data of the non-selected function units have zero regardless of the instruction so they do not activation and switching activity. We proposed instruction-level DVS technique without using DC-DC converter and voltage scheduler controlled by the operation system. The power of the selected function unit is the supplied power supply voltage V_{DD} and that of the non-selected function units are the reduced power supply voltage V_{DDL} in the proposed DVS technique. We selected reduced power supply to 0.667 times of the supplied power supply. The power supply voltages of function unit can transits the supplied power voltage 1.2 V to the reduced power supply voltage 0.8 V according to the instructions using the dynamic voltage scaling power supply. The energy efficiency of the proposed 32 bit parallel processor core using instruction-levels data gating and DVS techniques can improve about 88.4% than that of the 32 bit parallel processor cores without using instruction-levels data gating and DVS techniques. The proposed instruction-level DVS technique has the simple architecture than complicated DVS which is DC-DC converter and voltage scheduler controlled by the operation system and a hardware implementation is very easy. But, the energy efficiency of the proposed instruction-level DVS technique having dual-power supply is similar to the complicated DVS which is DC-DC converter and voltage scheduler controlled by the operation system.

The designed high energy efficiency 32 bit parallel processor core can utilize as the coprocessor processing massive data at high speed. The high energy efficiency multimedia chips can apply the multimedia data processing in which the calculation performance is much required in the portable devices.

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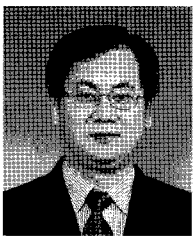

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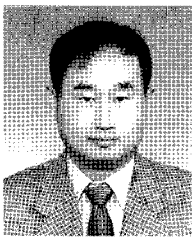

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