# A CPW-Based 77 GHz Power Amplifier with Cascode Structure Using a 130 nm $In_{0.88}GaP/In_{0.4}AlAs/In_{0.4}GaAs$ mHEMTs

Youngmin Kim · Yumin Koh · Youngrak Park · Siyoung Lee · Kwangseok Seo · Youngwoo Kwon

## Abstract

In this paper, we present a CPW-based 77 GHz 3-stage power amplifier MMIC for automotive radar systems. The power amplifier MMIC has been realized using a 130 nm $In_{0.88}GaP/In_{0.4}AlAs/In_{0.4}GaAs$ metamorphic high-electron mobility transistors(mHEMTs) technology and an output stage with a cascode configuration. This produced a good output power and gain performance at 77 GHz. The fabricated power amplifier MMIC exhibited a small-signal gain of 18 dB, an output power of 17 dBm and 9 % power added efficiency(PAE) at 77 GHz with a total gate width of 800 $\mu$m in the output stage. These performances could be useful to low-cost and small-sized components for 77 GHz automotive radar systems.

***Key words*** : Millimeter Wave, Automotive Radar, Cascode, mHEMT, MMIC, Power Amplifier, Coplanar Wave Guide.

## Ⅰ. Introduction

Power amplifier MMICs are key components in W-band applications like phased array or synthetic aperture radar, wideband communication systems and automotive sensors. Recently, the 77 GHz automotive radars has become popular, as reflected in the literatures[1]~[5]. In a typical automotive radar application, the transmitting power from the transceiver is 10 dBm at the antenna port. The main problems that we have to consider are the LO power path to the FMCW radar-type mixer, switch loss, lens loss for beam steering, and so forth. Therefore, the required output power of the power amplifier is usually 16 to 19 dBm. Due to the high combining losses[6]~[8], it is desirable to obtain high output power from a single chip. Recently, studies of power amplifier MMICs with transistors in a common source configuration on GaAs, InP and metamorphic HEMT technologies have been reported to have excellent results at W-band frequencies. An mHEMT a has higher gain and lower phase noise characteristics than an pHEMT. Moreover, compared to InP substrates, mHEMT technology on a GaAs substrate is cost effective, taking advantage of the high crystal quality, greater mechanical strength and the large size of GaAs wafers of up to 6 inches.

In this paper, we report on the development of a CPW-based 77 GHz 3-stage power amplifier MMIC with cascode structure that has been successfully fabricated by using 130 nm $In_{0.88}GaP/In_{0.4}AlAs/In_{0.4}GaAs$ m-HEMTs technology.

Compared to conventional HEMTs in a common source configuration, the cascode structure requires approximately the same chip area, while offering twice the gain even with large gate width, which is essential for high-output power. The coplanar waveguide technology utilized is very attractive at millimeter-wave frequencies, due to its simplified fabrication without backside processing, the high isolation between adjacent lines and its superior performance in flip-chip packaging than microstrip based MMIC.

## Ⅱ. Device Fabrication and Performance

The CPW based 77 GHz power amplifier circuit was fabricated using a InAlAs/InGaAs material system with $In_{0.88}GaP/In_{0.4}AlAs/In_{0.4}GaAs$ composite-channel HEMTs grown by MBE on a 625 $\mu$m-thick GaAs substrate. The metamorphic buffer consisted of a 1 um thick linearly graded InAlAs layer with a final indium content of 50 %. To reduce the surface trap effects, we adopted $In_{0.88}GaP$ with low surface defect density, which also functioned as an etch stop layer[9]. This structure achieved a sheet carrier density of $3.27\times10^{12}$ $cm^{-2}$ and an electron mobility of 7,490 $cm^2$/V-s at 300 K. The 130 nm T-gates were defined by e-beam lithography using a trilayer structure with ZEP/PMGI/ ZEP resist. A ultrasonic-assisted technique was used in a narrow recess, so that high uniformity and yield of devices could be achieved[10],[11]. And then, devices were passivated by using a $Si_3N_4$ of 600 Å(Fig. 1). For passive

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Institute of New Media and Communications, School of Electrical Engineering, Seoul National University, Seoul, Korea.

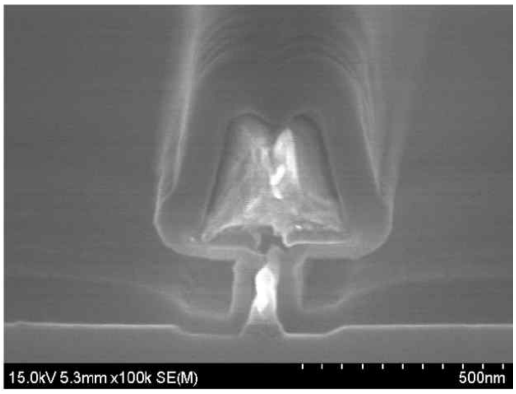
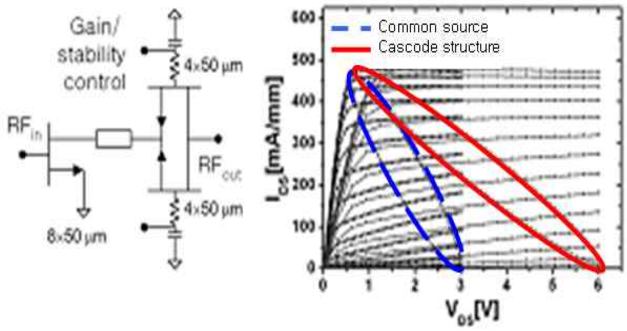



Fig. 1. SEM image of 130 nm T-gate with the passivation.




(a) (b)

Fig. 2. (a) Schematic of cascode cell, (b) Comparison of common-source mHEMT and cascode cell mHEMT.

devices, we used a NiCr of 610 Å as thin-film resistor with 20Ω/□ and used a $Si_3N_4$ of 900 Å as a MIM capacitor with 0.8 nF/mm$^2$. Finally, 0.5 μm and 2 μm-thick Au were deposited as the first and second metallization layers, respectively.

The average extrinsic transit frequency of $f_T$=220 GHz and a maximum oscillation frequency of $f_{max}$= 360 GHz were achieved for a 250 μm common source device at a drain voltage $V_{DS}$ of 1.4 V and a gate voltage $V_{GS}$ of 0 V. The mHEMT exhibits a maximum extrinsic $g_m$ of 750 mS/mm. The gate-drain breakdown voltage was over 4 V and the forward turn-on voltage was 0.9 V, measured at a gate current density of 1 mA/mm.

## Ⅲ. Design and Measurement

A 77 GHz cascode-connected PA with 130 nm mHEMT technology has been successfully fabricated. The small signal equivalent circuit of the cascode cell consists of a common-source transistor(850 μm) and a pair of transistors(2,450 μm) in a common gate configuration, as illustrated in Fig. 2(a). In order to achieve higher output power than that of the common source structure, a cascode cell was used in the power stage. This cascode configuration gives rise to almost twice ther output power of conventional HEMTs in a common source configuration because of increased output voltage swing Fig. 2(b). However, the cascode cell inherently has a positive feedback capacitance, $C_{DS}$ of the common-source transistor. This makes it more prone to instability and thus more difficult to use in an amplifier circuit than a common-source HEMT[12]. Therefore, it is so important to sacrifice the some gain to achieve further circuit stability[13]. In order to stabilize the cascode cell, we used a resistor in the gate bias line of a common gate. This resistor of the cascode cell was optimized to maximize the output power in a stable condition.

In this work, to predict the nonlinear behavior of the HEMT at millimeter-wave frequencies, the nonlinear mHEMT model was implemented in ADS using a symbolically defined device[14].

A chip photograph of the 77 GHz power amplifier is shown in Fig. 3. The size of the PA MMIC is 2.57 ×1.4 mm. The amplifier consists of 3 gain stages, of which the output stage is designed for maximum output power by using cascode structure and the other stages are designed for maximum gain. The coupled line has been employed to guarantee low-frequency stability and to minimize the variation of circuit performance caused by fabrication. The gate widths in the first stage and second stage are 250 μm and 450 μm, respectively. The bias condition in the first and second stage is $V_{GS}$ of 0 V and a $V_{DS}$ of 2.1 V. The output stage's total gate periphery is 800 mm and the total gate width of the mHEMT in the PA MMIC is as long as 1.1 mm.

A linear gain of approximately 18 dB was obtained at 77 GHz by applying a $V_D$ of 4.1 V, a common source FET's gate voltage of 0 V and a common gate FET's gate voltage of 2 V in the cascode cell

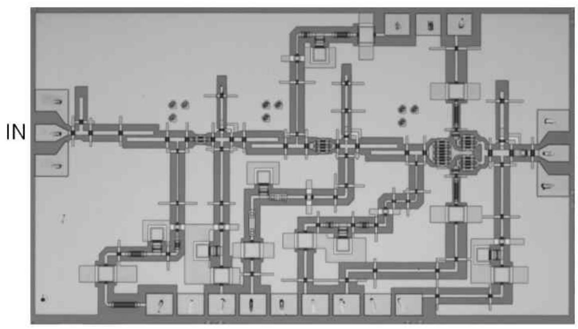



Fig. 3. Chip photograph of the fabricated CPW-based 77 GHz power amplifier with 3-stage. Chip size is 2.57×1.4 mm.

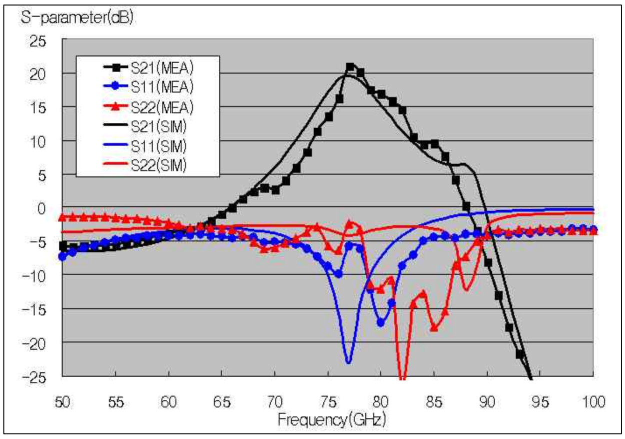



Fig. 4. On-wafer measured small-signal parameters of cascode-connected power amplifier with 3-stage.

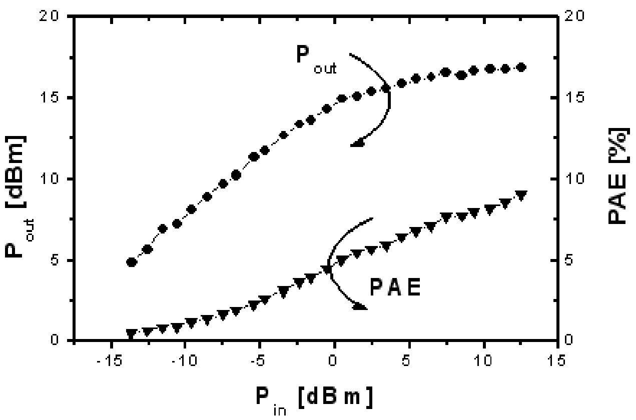



Fig. 5. Measured power performance of 77 GHz cascode-connected power amplifier with 3-stage.

Fig. 4. The drain current for the output stage was113 mA and the total drain current was 193 mA. Both input return loss($S_{11}$) and output return loss($S_{22}$) were better than 17 dB at 77 GHz. In particular, input return loss($S_{11}$) of over 10 dB from 75 to 81 GHz was achieved. The on-wafer measured output power($P_{out}$) and power added efficiency(PAE) of the CPW-based 77 GHz power amplifier is shown in Fig. 5.

With a drain voltage of only 4.1 V, we achieved a saturated output power of 17 dBm, and a maximum PAE of 9 % at 77 GHz.

Table 1 shows a comparison of published results on state-of-the-art 77 GHz power amplifier MMICs. These power amplifier results demonstrated the highest saturated output power among the all reported 77 GHz power amplifier MMICs using GaAs mHEMT technology and the all reported 77 GHz power amplifier MMICs using coplanar waveguide(CPW) technology without the external thermal dissipation. The power-stage die size of this amplifier is especially small except for the dimension of the combining lines, because only one cascode cell was applied in this fabricated 77 GHz high-power amplifier for increasing the output voltage swing.

## Ⅳ. Conclusion

This paper describes the successful development of a CPW-based 77 GHz power amplifier MMIC with a cascode structure. It used a 130 nm $In_{0.88}GaP/In_{0.4}AlAs/I_{n0.4}GaAs$ mHEMTs. This was grown by MBE on a 650 mm-thick GaAs substrate for in a 77 GHz automotive radar system. The devices showed an extrinsic trans-conductance $g_m$ of 750 mS/mm and an off-state gate-drain breakdown voltage of 8 V. A cut-off frequency($f_T$) of 220 GHz and a maximum oscillation frequency($f_{max}$) of 360 GHz were achieved. The fabricated power amplifier MMIC with a cascode configuration demonstrated a small-signal gain of 18 dB, a maximum output power of 17 dBm and 9 % power added efficiency. This power amplifier MMIC is highly suitable for 77 GHz automotive radar applications that require beam steering, longer range and higher range resolution.

Table 1. Comparison of previously published 77 GHz power amplifier with this work.

| Transmission line | Technology | Max. output power(dBm) | PAE (%) | Chip size (mm×mm) | Power stage die size (mm$^2$) | Ref. |
|---|---|---|---|---|---|---|
| M/S | 0.1 um pHEMT | 23 | 9 | 2.3×1.6 | >0.19 | [15] |
| M/S | 0.1 um pHEMT | 21.5 | 10 | 3×2 | >023 | [16] |
| M/S | 0.2 um pHEMT | 16 | N/A | 2.9×1.2 | 0.16 | [17] |
| M/S | 0.15 um mHEMT | 15.5 | N/A | 2×2 | Single transistor | [18] |
| CPW | 0.12 um mHEMT | 12.3 | N/A | 2.5×1 | Single transistor | [19] |
| CPW | 0.13 um mHEMT | 17 | 9 | 2.57×1.4 | 0.035 | This work |

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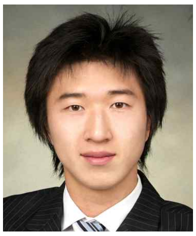
Youngmin Kim

was born in Masan, Korea in 1979. He received the B.S. degree in electronic engineering from Sung Kyun Kwan University, Suwon, Korea, in 2001 and the M.S. degree in electrical engineering fron Seoul National University, Seoul, Korea, 2005. He is currently working toward in the Ph.D. degree in electrical engineering fron Seoul National University. His current research interests include the design of MMICs for millimeter-wave systems using GaAs and Si device and their system integration.

Yumin Koh

received the B.S. degree in electrical engineering from Kyungpook National University, Daegu, Korea, in 2004, and the M.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2008, where she is currently working toward the Ph.D. degree in electrical engineering. From 2004 to 2006, she was a Research Engineer at the LG Electronics. Her research interests include the design and fabrication of MMICs for millimeter-wave applications and system integration using system-on-packaging technology.

Young-rak Park



was born in Ulsan, Korea, in 1986. He received the B.S. degree in electronic engineering from Information & Communication University, Dae-jeon, Korea, in 2008. He is currently working toward the Master degree in the School of Electrical Engineering and Computer Science, Seoul National University. His current research interests include the power amplifier design for millimeter-wave systems using GaAs and Si devices.

Siyoung Lee

was born in Seoul, Korea in 1986. He received the B.S. degree in the school of Electrical Engineering and Computer Science from Seoul National University, Seoul, in 2009. He is currently working toward the Master degree in the School of Electrical Engineering and Computer Science, Seoul National University. His current research interests include the design of millimeter-wave integrated circuits, especially Power Amplifier, using GaAs and Si devices.

Kwang-seok Seo

received the B.S. degree from Seoul National University in 1976, and the M.S. degree from the Korea Advanced Institute of Science and Technology in 1978, and the Ph.D. degree on electrical engineering from the University of Michigan, Ann Arbor in 1987. From 1978 to 1982, he was a senior research engineer at the korea Institute of electronics Technology. From 1987 to 1988, he was a postdoctoral fellow at the IBM T.J. Watson Research Center. Since 1989, he has been with Seoul National University, where he is now an Associate Professor in the School of Electrical engineering. His current interests include high speed device physics and technology, compound semiconductor materials, and high frequency circuit design.

Youngwoo Kwon

was born in Korea, in 1965. He received the B.S. degree in electronics engineering from Seoul National University in 1988, and the M.S. and Ph.D. degrees in Electrical Engineering from the University of Michigan, Ann Arbor, in 1990 and 1994, respectively. From 1994 to 1996, he was with Rockwell Science Centeras a member of technical staff, where he was involved in the development of millimeter-wave monolithic integrated circuits. In 1996, he joined the faculty of School of Electrical Engineering, Seoul National University, where he is currently a Professor. Dr. Kwon is currently a senior member of the IEEE, and has been working as an Associate Editor for IEEE Transactions on Microwave Theory and Techniques. He has authored and co-authored over 150 technical papers in the internationally renowned journals and conferences. He has also served as a technical program committee member of various microwave and semiconductor conferences including IMS and IEDM. Over the past years, he has directed a number of RFresearch projects funded by Korean government and US companies. In 1999, he was awarded a Creative Research Initiative program by Korean Ministry of Science and Technology with a nine year term to develop new technologies in the interdisciplinary area of millimeter-wave electronics, MEMS and biotechnology. Dr. Kwon is a co-inventor of switchless stage-bypass power amplifier architecture called "CoolPAMTM" and co-founded Wavics, a power amplifier design company, which is now fully owned by Avago Technologies. He holds more than 20 patents on RF MEMS and power amplifier technology. He was the recipient of Presidential Young Investigator award from Korean government in 2006.