The Analysis and Implementation of DVB-S2 BC mode ystem

In Ki Lee, Dae Ig Chang

요 약

2005년 DVB-S2 규격이 최종 마무리 되었지만 이미 보급된 기존의 수많은 DVB-S 수신기는 새로이 완전한 DVB-S2 수신기로 교체되기까지는 여전히 DVB-S 신호는 수신되어야 한다. 이를 위해서 방송사업자는 기존의 DVB-S 수신기에는 DVB-S 신호를, DVB-S2 수신기에는 DVB-S2 신호를 전송해야 한다. DVB-S2 수신기에서 DVB-S서비스를 수용하기 위해서는 DVB-S2 chip에 DVB-S 모듈이 구현되어야 한다. 이런 역호환성을 위해서 시스템에서는 계층적 변조 방식을 적용해야 하며, 시스템 마진을 만족하기 위해 본 논문에서는 편향각에 따른 시스템의 성능을 분석하였으며 또한 성능을 검증해 보았다. 그리고 본 방식을 검증하기 위해서 FPGA chip을 이용하여 테스트베드를 구현하였으며 이를 보인다

.

Key Words : 역호환성, DVB-S2, LDPC, FPGA

ABSTRACT

In 2005, DVB-S2 spec. was finalized. But with a large number of DVB-S receivers already installed, backwards compatibility may be required for a period of time, where old receivers continue to receive the same capacity as before, while the new DVB-S2 receivers could receive additional capacity broadcasts. To facilitate the reception of DVB-S serviced by DVB-S2 receivers, implementation of DVB-S in DVB-S2 chips is highly recommended. For the backward compatibility the system adapt the hierarchical modulation scheme. And the system has to meet system margin, so in this paper analyzes the effect according to the deviation angle and shows the BER performance. And finally this paper shows the result of the system implement using FPGA chip.

Key Words : Backward compatibility, DVB-S2, LDPC, FPGA

I. Introduction

In 1999 the Technical Module of the DVB project started an investigation on the potential of the new schemes, to increase the bit-rate and power efficiency in future satellite television broadcasting and contribution services. The preliminary objective of a new broadband satellite modulation and coding scheme is to enable delivery of a significantly higher data rate in a given transponder bandwidth than the current DVB-S standard. This project is called DVB-S2. In fact, with a large number of DVB-S receivers already installed, backwards compatibility may be required for a period of time, where old receivers continue to receive the same capacity as before, while the new DVB-S2 receivers could receive additional capacity broadcasts. When the complete receiver population has migrated to DVB-S2, the transmitted signal can be modified to a non-backwards compatible mode, thus exploiting the full potential of DVB-S2. To facilitate the reception of DVB-S serviced by DVB-S2 receivers, implementation of DVB-S in DVB-S2 chips is highly recommended. In this paper, we analyze the BC mode performance of DVB-S2 and show the result of the system implement.

2. Hierarchical Modulation System configuration

2.1. Hierarchical Modulation Scheme for Backward-Compatible mode

In the DVB-S2 spec. the hierarchical modulation technology was studied because it

* Electronics and Telecommunications Research Institute 161 Gajeong-dong, Yuseong-gu, Daejeon, 305-700, KOREA
Email: popularity1@etri.re.kr, dchang@etri.re.kr
논문번호 : K3-2-7 , 접수일자 : 2008년 11 월 28일, 최종게재논문통보일자 : 2008 년 12 월 26일

can impose higher-order modulations over conventional modulations without a big impact. In the hierarchical modulation, the present data stream is assigned as high-priority (HP) channel whereas newly added data are put to low-priority (LP) channel. When both data streams are mapped by 8PSK symbols, HP stream conveys the bits of both MSB(Most Significant Bit, 'b0' in Figure 1) and CSB(Center Significant Bit, 'b1' in Figure 1) whereas LP stream determines the LSB(Least Significant Bit, 'b2' in Figure 1). A visualized concept of this mapping process is shown in Figure 1.

This hierarchical 8PSK can be regarded as a non-uniform 8PSK splitting each QPSK-modulated symbol into 2 symbols separated by the amount of deviation angle θ as shown in Figure 1. As the deviation angle becomes larger, the performance of LP increases because of a longer distance between two symbols at the cost of HP performance. So it turns out the most important key design parameter to achieve an optimized structure design to this capacity expansion problem while minimizing the impact to the existing channel performance.

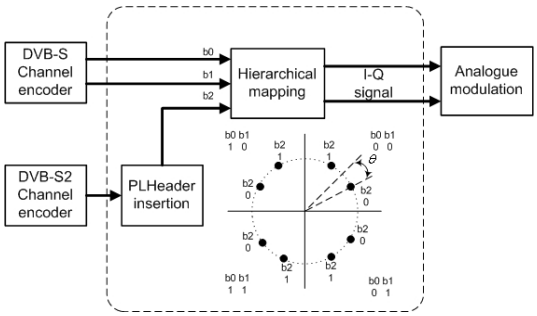


Figure 1: DVB-S2 BC mode hierarchical modulation scheme

2.2. The analysis of the Backwards-compatible system

In case of an error when transmitter sends quadrant 1, the receiver would take quadrant 1 for quadrant 2 or quardrant4. The probability is shown in equation (a),(b) and (c) where P12 and P14 are probability when system takes quadrant1 for quadrant 2, 4 respectively and Pe is the total error probability.

$$P_{14} = \int_0^{\infty} \frac{1}{\sqrt{\pi N_0}} \exp\left(-\frac{(x+\sin(45-\theta))}{N_0}\right) dx$$
$$= \frac{1}{\sqrt{2\pi}} \int_{\sqrt{\frac{2}{N_0}}\sin(45-\theta)}^{\infty} \exp(-\frac{t^2}{2}) dt \quad \text{(a)}$$
$$= Q\left(\sqrt{\frac{2}{N_0}}\sin(45-\theta)\right)$$

$$P_{12} = Q\left(\sqrt{\frac{2}{N_0}}\sin(45+\theta)\right) \quad \text{(b)}$$

$$P_e = P_{14} + P_{12}$$
$$= Q\left(\sqrt{\frac{2}{N_0}}\sin(45-\theta)\right) + Q\left(\sqrt{\frac{2}{N_0}}\sin(45+\theta)\right) \quad \text{(c)}$$

As seen from Figure 1, a predefined angle, θ, controls the performance of the system, and its value can be set from 0 to 22.5 degree. This means the deviation angle plays as the system parameter by which the system should be designed to give a trade-off of overall performance. From the system optimization point of view, a new encoding method for LP stream should have been developed to optimize the performance of both HP and LP stream at the same time.

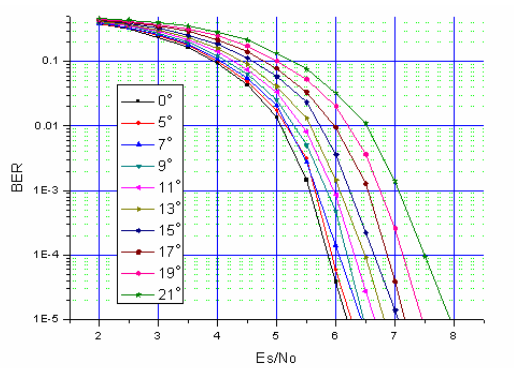


Figure 2: The BER graph of HP

Figure 2 shows the Bit Error Rate (BER) graphs of the present system, calculated when the deviation angle is set at an interval of 2° from 5° to 21°. Because the deviation angle 0° can be

interpreted as QPSK and the result in that case means the performance of the present system and the proposed system. Considering that the worst link margin is around 4dB, the deviation angle 15° is proper in the deterioration tolerance of 1.5dB and 11° is proper in case of 1.0dB at 10E-6. From this consideration, the performance analysis of the added stream has been tested with the deviation angle varying from 5° to 21°.

We have tested the added system by applying total 6 code rates from 1/3 to 8/9, using LDPC bits coding method. The result of the test shows that the performance in case of the deviation angle 15o provides the satisfiable service both to HP and LP, as seen in Figure 3. Particularly at code rate 1/3, compared to HP 15°, the added system can provide services at the same quality as the present system with hierarchical modulation. In this particular case, it is confirmed that the increase in transmission bandwidth is about 36%. With 36% increase in transmission bandwidth, we expect that about 1/3 more number of channels or higher quality screen service could be available than the present system.

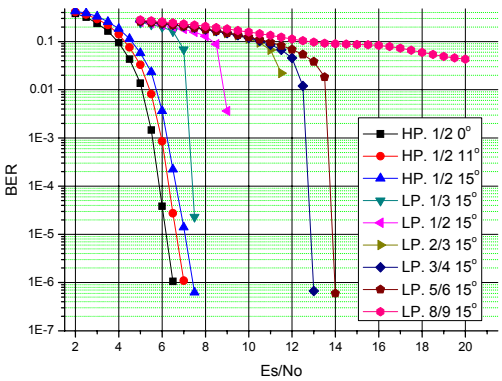


Figure 3: The BER graph of LP

3. The Implementaion of the Backwards-Compatible mode and IF loopback Test

Figure 4 shows the block diagram of the BC mode for the implementation and Test. We have implement the transmit/receive system test-bed. The test-bed is consist of Power module, Baseband board, RF board. And the Baseband board is consist of mode&stream adaptation module, channel CODEC and MODEM. Figure 5 shows the best-bed. As shown, Mode & Stream adaptation and channel encoder are implement on the FPGA#1(XC2V3000). And Modem is implemented on the FPGA#2(XC2V3000). Finally LDPC decoder is implemented on the FPGA#3(EP1S80F1508C6ES). For the test of IF(140MHz) loopback and Satellite the system parameters are as follow. Figure 6 shows the test of the BC mode system.

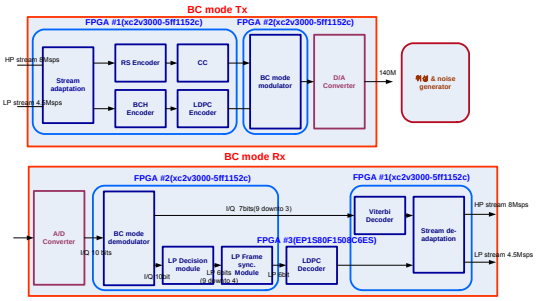


Figure 4: The block diagram of the BC mode forimplementation

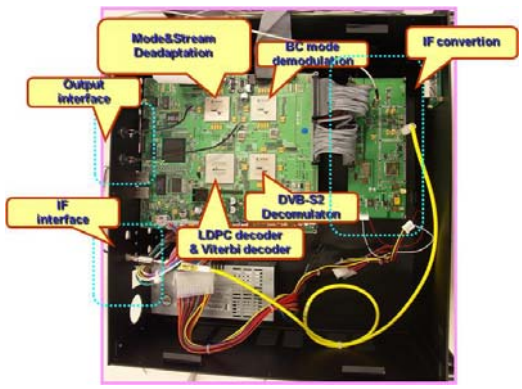


Figure 5: The block diagram of target board for BC mode implementation

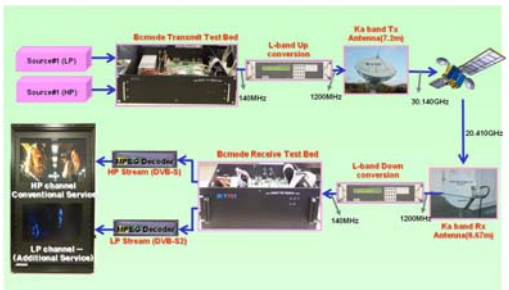


Figure 6: The Configuration diagram of the BC mode system

◆ System Parameter
- HP
  - Tx : RS + CC(1/2)
  - Rx : only implement Viterbi decoder
- LP
  - Tx : BCH + LDPC(2/3)
  - Rx : only implement LDPC(iteration number = 8)
- Hierarchical 8PSK(deviation angle = from 0 to 15
- Symbol rate : 9Msps
- Source bit rate
  - HP : 8.5 Mbps LP : 4.5 Mbps
- Working clk
  - FPGA #1 : 9M,27M FPGA #2 : 9M,27M
  - FPGA #3 : 54M
- Satellite imform.
  - KoreaSat #3, transponder #1
  - Uplink Freq. : 30.140GHz
  - Downlink Freq. : 20.410GHz

4. Conclusions

In this paper we describe the need of backward compatibility for DVB-S2. And we analyze the key parameter, deviation angle. As the deviation angle becomes larger, the performance of LP increases because of a longer distance between two symbols at the cost of HP performance. As shown figure 3, the BER performance was analyzed. Finally we implement the BC mode system.

5. Acknowledge

This work was partly supported by the IT R&D program of MIC/IITA[2008-S008-01, Development of 21GHz Band Satellite Transmission Technology]

Reference

[1] ETSI EN 302 307 v1.1.1, "Digital Video Broadcasting (DVB) : Second Generation Graming Structure, Channel Coding and Modulation System for Broadcasting, Interative Service, News Gathering and other broadband satellite application," June 2004.

[2] Stephen B. Wicker, "Error Control Systems for digital communication and storage", Prentice Hall, New Jersey, 1995.

[3] E. Casini, R. D. Gaudenzi, and A. Ginesi, "DVB-S2 modem algorithm design and performance over typical sattlite channel," ESA, ESTEC.

[4] M. Luise and R. Reggiannini, "Carrier frequency recovery in all digital modem for burst mode transmissions," IEEE Trans. Commun., vol. 43, pp.1169-1178, Feb./March./ Apr. 1995.

[5] U. Mengali and M. Morelli, "Data-aided frequency estimation for burst digital transmission, " IEEE Trans. Comm., vol. 45, pp. 23-25, Jan. 1997.

[6] F. M. Gardner, "A BPSK/QPSK timing-error detector for sampled receivers," IEEE Trans. Commun., vol. com-34, pp. 423-429, May 1986

[7] D. R. Pauluzzi and N. C. Beaulieu, "A comparision of SNR estimation techniques for AWGN channel," IEEE Trans. Commun., vol. 48, pp. 1681-1691, Oct. 1986.

[8] F. M. Gardner, "Interpolation in digital modems-Part I: Fundamentals." IEEE Trans. Commun., vol. 41, NO. 3, Mar. 1993.

[9] F. M. Gardner, "Interpolation in digital modems-Part II: Implementation and performance." IEEE Trans. Commun., vol. com-41, NO. 6, June 1993.

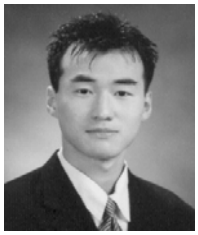
[10] E. Casini, R. De Gaudenzi, and A. Ginesi, "DVB-S2 performance in presence of satellite channel impairment," European Space Agency, Apr. 2004.

[11] F.-W. Sun, Y. Jiang, and L.-N. Lee, "Frame synchronization and pilot structure for second generation DVB via satellites," Int. J. Satell. Commun. Network, 22:319-339. 2004.

.

저 자

이 인 기(In Ki Lee)



Received his BS in 2003, MS in 2005, from Korea Maritime University, Busan, Korea. Since July 2005, he joined the Electronics and Telecommunications Research Institute (ETRI), Daejeon, Korea, where he is currently a Researcher. His interests is channel coding scheme, especially Turbo code, TPC, LDPC and QPSK demodulator scheme. His research in present is FPGA implementation of DVB-S2 MODEM.

장 대 익(Dae-Ig Chang) 정회원

1985년 2월: 한양대학교
전자통신공학과 학사
1989년 2월: 한양대학교
전자통신공학과 석사
1999년 2월: 충남대학교
전자공학과 박사
1990년 2월～현재: 한국전자
통신연구원
광대역무선멀티미디어연구팀 팀장
1991년~1993년 캐나다 MPR Teltech 연구소
VSAT팀 연구원
2005년~현재 과학기술연합대학원대학교(UST)
이동통신 및 디지털방송공학전공 교수

<관심분야> 위성통신시스템,위성방송,
디지털통신, 디지털 변복조등