A 9 mW Highly-Digitized 802.15.4 Receiver Using Bandpass ΣΔ ADC and IF Level Detection

Yong-IL Kwon[1] · Ta-Joon Park[1] · Hai-Young Lee[2]

Abstract

A low power(9 mW) highly-digitized 2.4 GHz receiver for sensor network applications(IEEE 802.15.4 LR-WPAN) is realized by a 0.18 μm CMOS process. We adopted a novel receiver architecture adding an intermediate frequency (IF) level detection scheme to a low-power complex fifth-order continuous-time(CT) bandpass ΣΔ modulator in order to digitalize the receiver. By the continuous-time bandpass architecture, the proposed ΣΔ modulator requires no additional anti-aliasing filter in front of the modulator. Using the IF detector, the achieved dynamic range(DR) of the overall system is 95 dB at a sampling rate of 64 MHz. This modulator has a bandwidth of 2 MHz centered at 2 MHz. The power consumption of this receiver is 9.0 mW with a 1.8 V power supply.

Key words : Receiver, ΣΔADC, Modulator, Bandpass Sigma Delta ADC, Complex Filter.

Ⅰ. Introduction

Given that the current trend is toward multi-standard receivers handling a variety of modulation formats, receiver specifications must increasingly accommodate the specifications of several standards. The results are that all the requirements of bandwidth, linearity and noise are becoming more difficult and that receiver flexibility is a must; in a similar vein, cost, size and power pressures have put increased emphasis on system simplicity and efficiency. Therefore, compared to mobile communications, sensitivity and interference levels are moderated. ZigBee appears as a prime candidate for the adoption of a full-digital implementation of the receiver baseband[1].

Fig. 1 shows a signal processing chain of the type found in a conventional receiver. As depicted in the figure, the incoming signal is repeatedly filtered, amplified and mixed down to a lower frequency before finally being digitized and sent to a digital signal processor(DSP). The baseband chain performs two major roles, channel selection and gain adjustment to accommodate close to a 90 dB dynamic range(DR) input signal. In this architecture, the increased filtering can relax both the bandwidth and the dynamic range requirements of the ADC, and the wanted signals are recovered by further analog demodulation and by consecutive quantization. All analog stages add noise and distortion; moreover, their offset and gain/phase errors accumulates and many calibrations are required for the correction. This increases the design time, the complexity and the risk resulting in increased cost and current consumption[2].

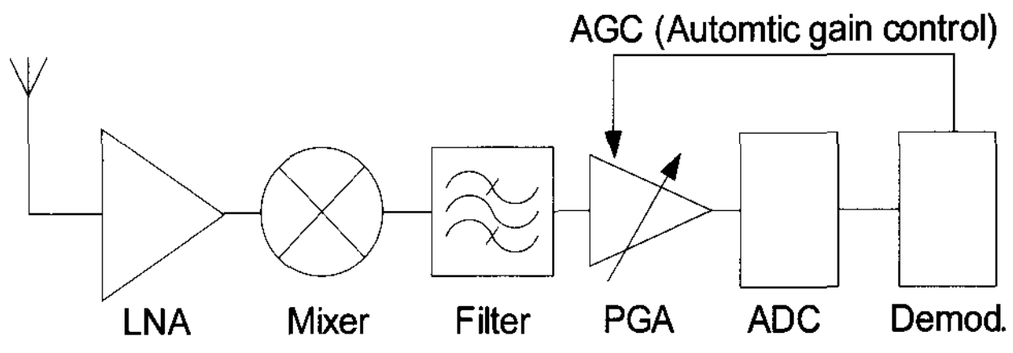

Fig. 1. The conventional receiver architecture.

Solutions for the burdens have been to minimize analog processing stages and to rely on the digital signal processing using the ADC. Performing analog-to-digital conversions early in the signal chain requires conversion of either narrowband bandpass or narrowband quadrature signals, while the high dynamic range requirements mandate the use of ΣΔ techniques.

In this paper, a new digital receiver architecture using a continuous-time(CT) ΣΔ ADC and an IF level detection scheme is proposed as shown in Fig. 2. The CT ΣΔ ADC features the channel selection and programmable gain amplification(PGA) functions and uses a CT bandpass scheme to eliminate the anti-alias filter(AAF). The input-referred dynamic range(95 dB) of the receiver system using ΣΔ ADC is further improved by incorporating an IF level detection scheme.

Ⅱ. Receiver Architecture

2-1 Derivation of the Main Specifications

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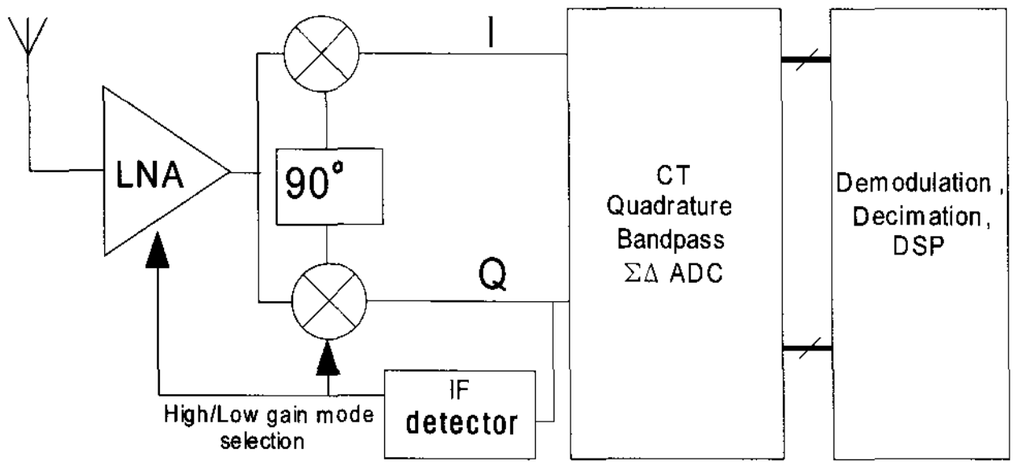


Fig. 2. The proposed receiver architecture.

An analysis of the noise in cascaded stages can be explained by the Friis equation[3]. Eq. (1) shows the sensitivity as the minimum input signal that yields a specific output signal-to-noise ratio(SNR). Therefore, the analog front-end requires 22 dB noise figure(NF) on the −85 dBm sensitivity specification in a 2 MHz bandwidth of the ZigBee standard[1].

$$P_{in,\min} = -174 \ \text{dBm/Hz} + NF + 10\log B + SNR_{\min} \quad (1)$$

At the demodulator input, a 3 dB SNR is needed for an input signal with a packet error rate(PER) of 1 %, as the processing gain is 9 dB. Taking into account a 10 dB margin, the NF of the analog front-end must be less than 12 dB. When a conventional receiver is used, a DR of above 95 dB is needed to meet the ZigBee standard considering the margin. A receiver with modest requirements for an instantaneous dynamic range will mostly rely more on AGC, the LNA and the mixer.

In the proposed receiver, the LNA and the mixer take charge of the 35 dB DR and the ΣΔ ADC takes charge of the 60 dB DR. Specifically, the ΣΔ ADC must receive the input power from 0 dBm to −60 dBm for a reasonable specification. In order to realize the input-referred DR of 95 dB, a novel receiver architecture adding IF level detector is implemented. The linearity and the interference specifications of the front-end are also based on ZigBee. This implies the specified third-order input-referred interception point(IIP3) of −34 dBm(not considering the margin)[1]. Detailed specifications of each block are shown in Table 1.

2-2 ΣΔ ADC Topology

According to the plots in Fig. 3 and Eq. (2), either a fifth-order single-bit modulator, a fourth-order 2-bit modulator, or a third-order 3-bit modulator can be used to achieve this signal-to-quantization-noise ratio(SQNR)[4]. In practice, each of these architecture types should be tried and evaluated in terms of power and/or area efficiency. Hence, the first configuration(5^{th}, 1-bit) and the over sampling rate(OSR) of 32 are used considering the

Fig. 3. Empirical SQNR limit for 1 bit mod. of order N.

margin. The variable gain amplifier(VGA) can be eliminated if the ADC has sufficient dynamic range, and the AAF can be eliminated if the ADC is of the continuous-time variety.

$$M = \left(\frac{2}{3} \cdot \frac{DR^2}{2L+1} \cdot \frac{\pi^{2L}}{2^B - 1} \right)^{\frac{1}{2L+1}} \quad (2)$$

Here, M is the oversampling rate, DR is the dynamic range, B is the quantization bit and L is the modulator order.

Therefore, the system can be simplified greatly using the power-efficient and high-dynamic-range continuous-time bandpass ΣΔ ADC. As the cascade of integrators

Table 1. Receiver budget.

	Unit	PCB loss	Balun	LNA	Mixer	SD ADC
Voltage Gain (Av)	dB	−1	2.5	24.3	9.5	-
Cascaded Av	dB	−1	1.5	25.8	35.3	-
Block NF	dB	1	0.5	4	9.1	-
Cascaded NF	dB	1	1.5	5.5	6.1	-
Thermal Noise power	dBm	−11.8	−112.3	−99.1	−97.1	-
IIP3(Rout)	dBm	100	100	−20	−2	-
Cascaded IIP3	dBm	100	97.5	−18.5	−19.7	-
P1dB	dBm	-	90	−30	−12	
Max. input	Vpp	-	-	-	-	1
DR	dB	-	-	25	10	60
SNDR	dB	-	-	-		70

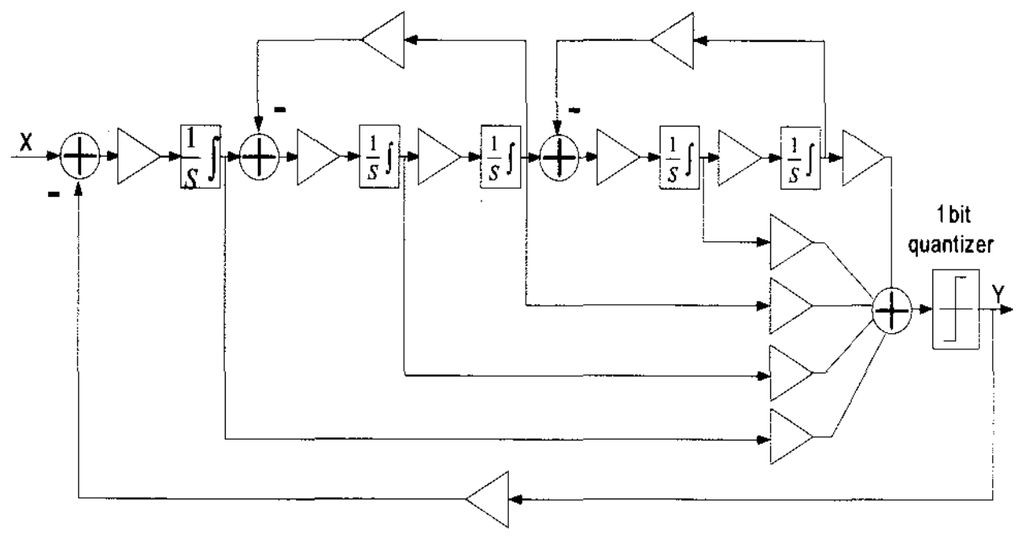


Fig. 4. A simplified block diagram of ΣΔ modulator.

feedforward form(CIFF) is better for linearity, CIFF is used [5]. In this paper, coefficients for such standard structures are found using the ΣΔ Toolbox[4],[6].

A simplified block diagram of the ΣΔ modulator is shown in Fig. 4. A bandpass filter (BPF) can be realized by the complex function[3]. The signal transfer function(STF) and the noise transfer function(NTF) can be calculated by the Mason's gain rule[7].

2-3 Effects of Non-idealities in CT ΣΔ ADC

The major error contributors are the feedback digital-to-analog converter, the filters, and integrators within a ΣΔ modulator loop. As the feedback pulse is affected by timing errors, constant delays of the pulse are generated. These increase the actual modulator order, which decreases the maximum stable amplitude and decreases the noise shaping performance. To offset the increased modulator order due to the excess looping, an additional feedback path is used [5]. Though 1-bit continuous-time modulators show good linearity, a 1-bit CT modulator is affected severely by clock jitter compared to discrete-time counterparts; thus, a tradeoff is needed. In this paper, a 1-bit quantizer is implemented. STF and NTF change due to the nonlinearity of the integrator; hence, tuning of the passive components(Capacitor, Resistor) is used [8],[9].

III. Design of Receiver

Fig. 5 shows a detailed description of the CMOS receiver with CT ΣΔADC adding IF level detector.

3-1 Low-Noise Amplifier and Down Conversion Mixer

The LNA topology(Fig. 6) uses a common-source amplifier tuned to 2.4 GHz with cascode transistors to maximize the reverse isolation and an inductor degeneration scheme that uses a bond wire to achieve real-part impedance up to 50 ohm[10]. The gain is programmable between 25 dB and 11 dB. The NF is 1.5 dB in the high-gain mode.

Given that MOS transistors have much higher IIP3 values than bipolar transistors, it is possible to integrate "linear" mixers. Therefore, more gain can be assigned to the LNA, which relaxes the noise specifications of the mixers. In the circuit topology of Fig. 7, the down-conversion mixer employs a Gilbert cell mixer topology[3]. The quadrature architecture reduces LO leakage and LO self-mixing. The gain is programmable between 9.5 dB and −10 dB. The measurement results of the front- end

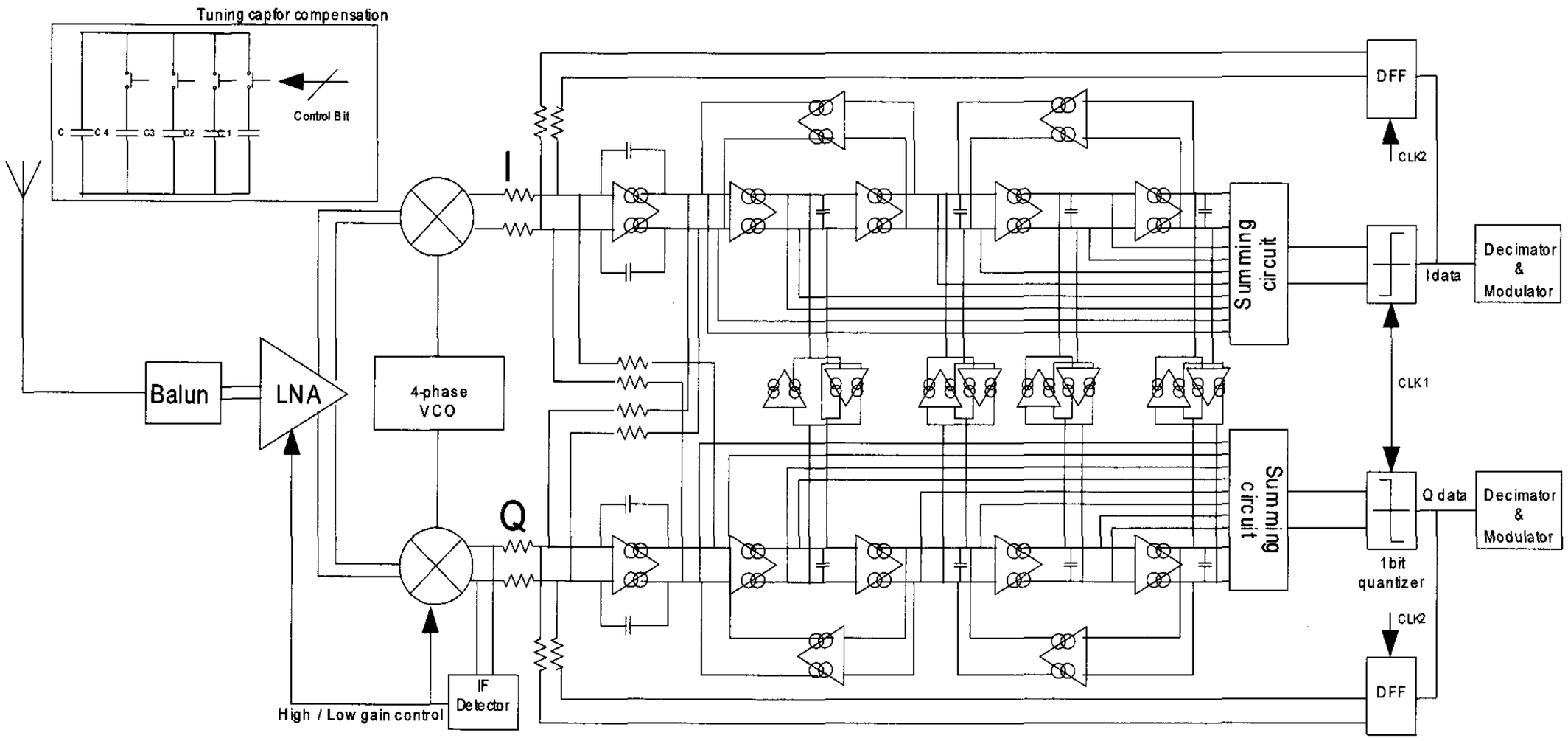


Fig. 5. A detailed circuit description of the CMOS RF receiver using ΣΔ modulator.

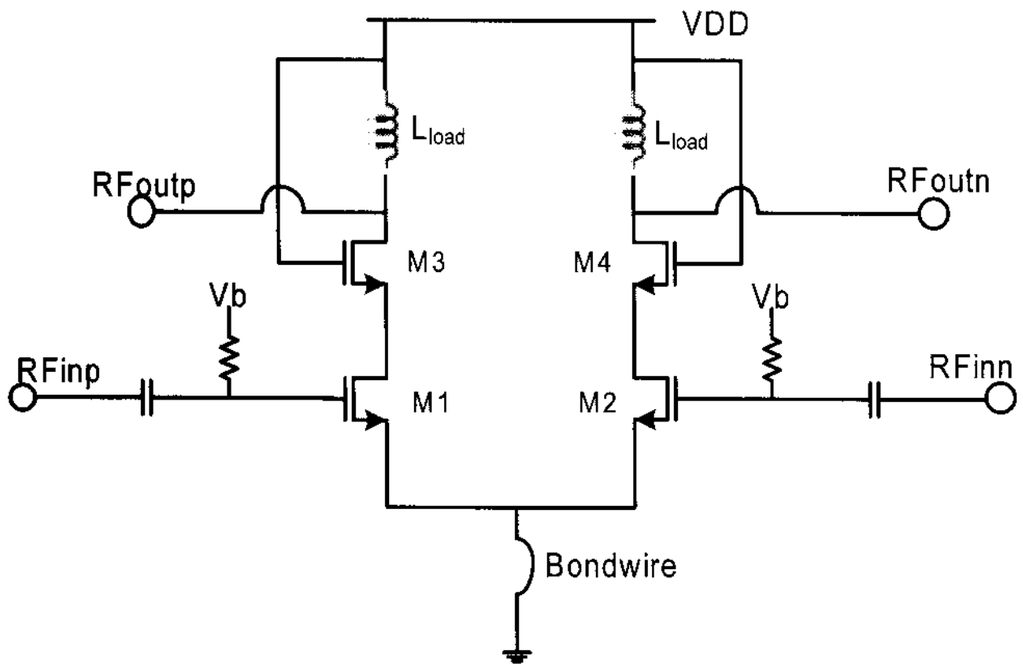


Fig. 6. LNA topology.

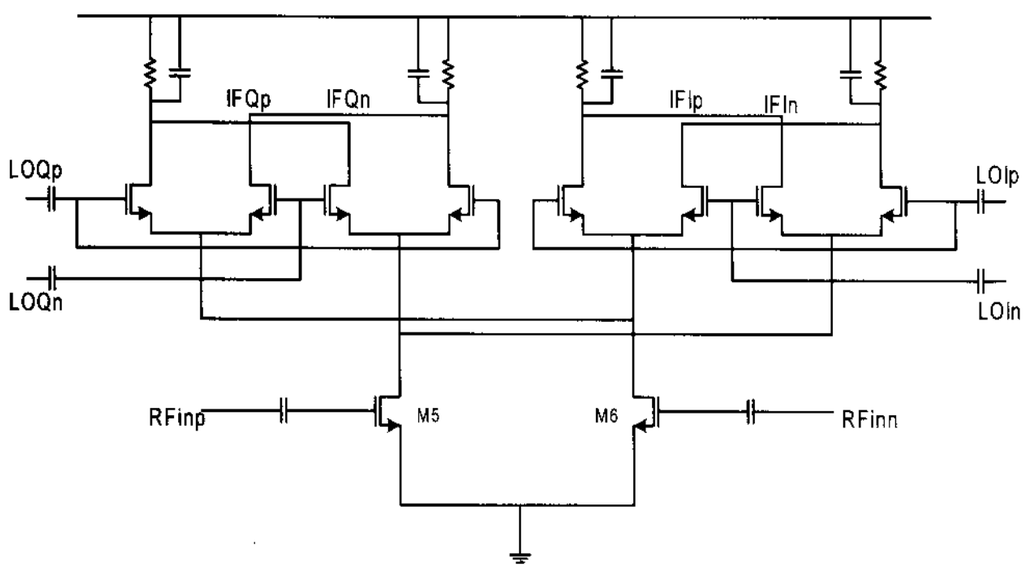


Fig. 7. Down conversion mixer topology.

Table 2. Measurement results (LNA & Mixer).

Parameters	LNA+Mixer (sim.)	LNA+Mixer (Mea.)
Die size	0.49 mm^2	0.49 mm^2
Signal freq	2.4 GHz	2.4 GHz
Power supply	1.8 V	1.8 V
Power consumption	2.8mA @ 1.8 V	2.5mA @ 1.8 V
Voltage gain	37 dB	3
NF	3.5 dB	4.5 dB
IIP3	−15 dB	−16 dB

are shown in Table 2.

3-2 Continuous Time Bandpass ΣΔ ADC

This ΣΔ ADC has five integrators, of which the first of these is an active RC integrator and the four subsequent integrators are gm-C integrators. Therefore, the cross-coupling of the first integrator is realized by the resistor and that for the gm-C integrators is realized by OTAs in a gyrator structure. A complex BPF can be realized by frequency shifting of a lowpass filter. The transfer function of the BPF(Hbp) can be obtained from the lowpass filter(Hlp) as shown in [11].

$$H_{bp}=(j\omega)=H_{lp}(j\omega - j\omega_c) \tag{3}$$

Where, $fc=\omega c/2\pi$ is the center frequency. The frequency shift in the transfer function is done via cross-coupling of two real filters, as shown in Fig. 8.

A schematic of the gm-cell in the loop filter is shown in Fig. 9. There are numerous design methods for a gm-cell. As the first integrator(active RC) is charged in terms of linearity, the following integrators do not need to have good linearity. Thus, considering the power consumption, a conventional gm-cell is implemented.

A summing circuit was also designed by modifying the gm-cell, as shown Fig. 10. The analog output signal of the summing circuit is sampled by a 1-bit quantizer (comparator) followed by a master-slave D-flip-flop. The 1-bit quantizer consists of a comparator core and an SR latch, which stores the differential output signals. The SR latch is implemented with a NOR gate[13]. The phase difference of clocks (CLK1, CLK2) is optimized by func-

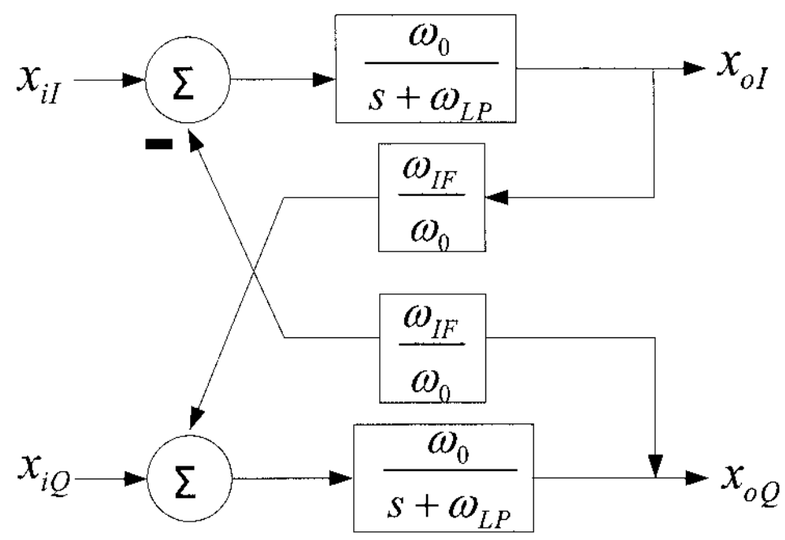


Fig. 8. Block diagram of a complex filter.

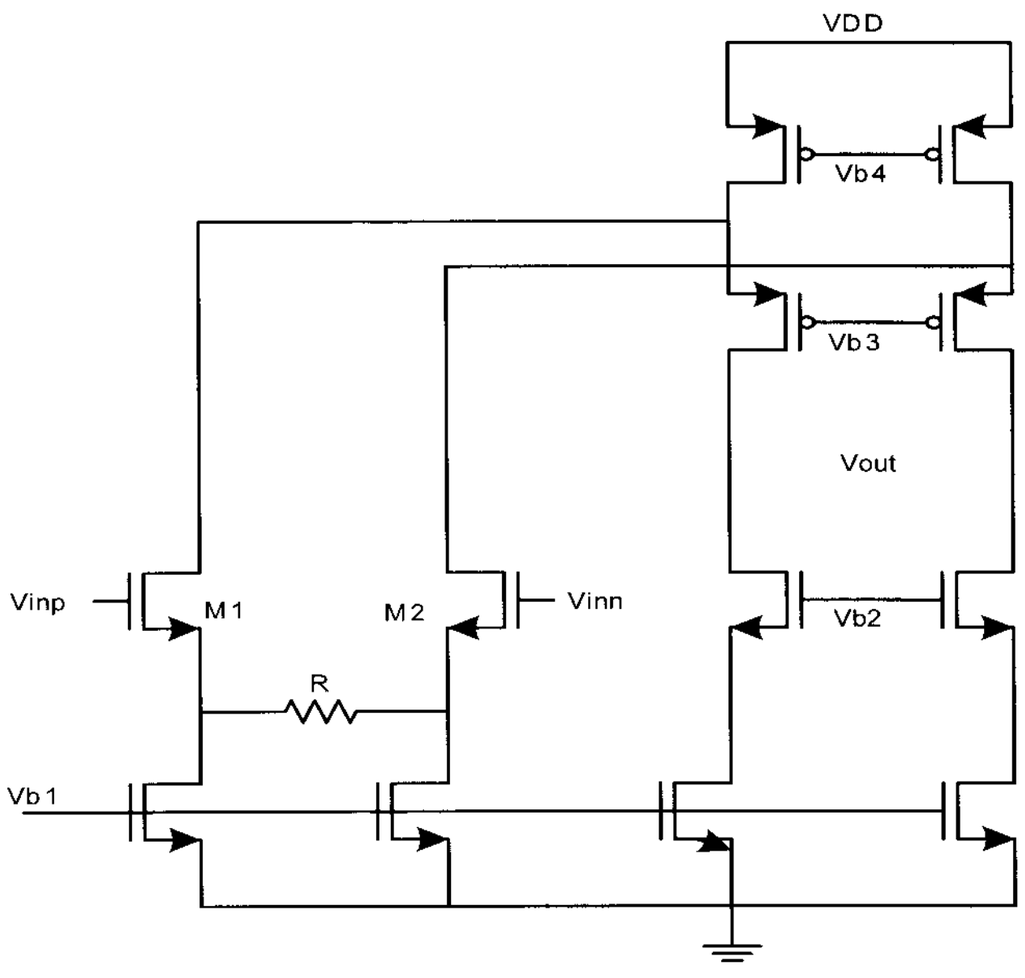


Fig. 9. A simplified gm-cell.

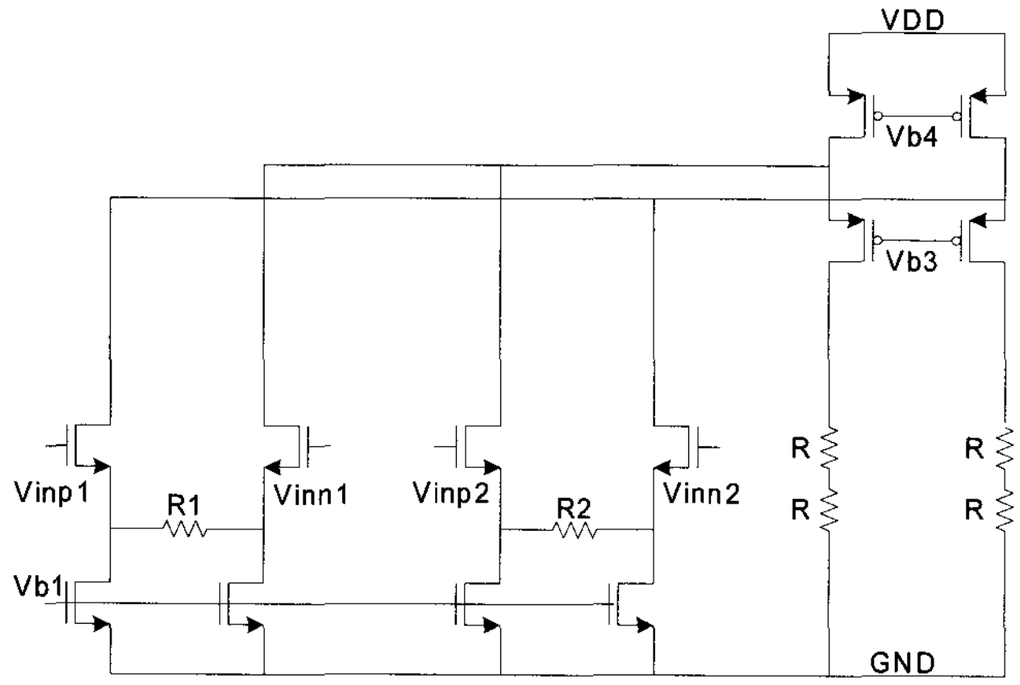


Fig. 10. A simplified summing circuit.

tion generators to avoid excess loop delay and the reference clock using a crystal oscillator is used to reduce the clock jitter and to get better SNR.

3-3 IF(Intermediate Frequency) Level Detector

The IF detector in this system is utilized to increase the dynamic-range using gain control. Depending on the amplitude of the input signal, IF detector selects the high or low gain mode for LNA and Mixer. The IF detector is composed of a full-wave rectifier and comparator. If the input power is higher than −50 dBm LNA and Mixer has low gain mode, else LNA and Mixer have a high gain mode . The triggering range is changed from −40 dBm to −60 dBm by the Vref. The IF level detector circuit and measurement results are shown in Fig. 11 and Fig. 12[15].

Ⅳ. Experimental Results

4-1 Measurements Methods

Fig. 13 shows the measurement setup used to test the receiver using ΣΔ ADC. A signal generator provides a signal at 2.4 GHz. Two pulse generators drive the two input clocks(CLK1, CLK2) which use identical frequencies and different phases. The differential 1-bit I/Q bitstreams are captured by a logic analyzer and are then analyzed using MatLab[6],[13].

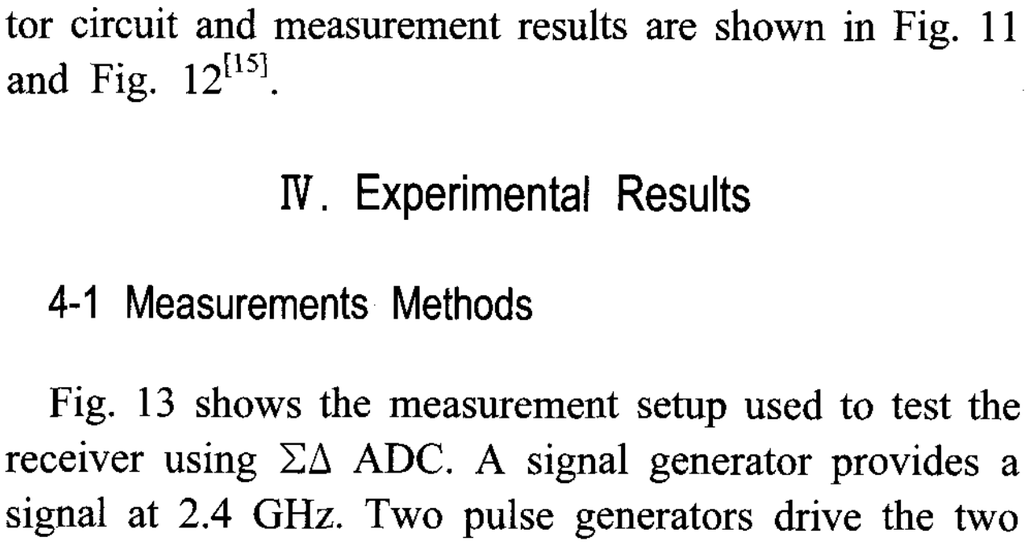


Fig. 11. A simplified IF detector circuit.

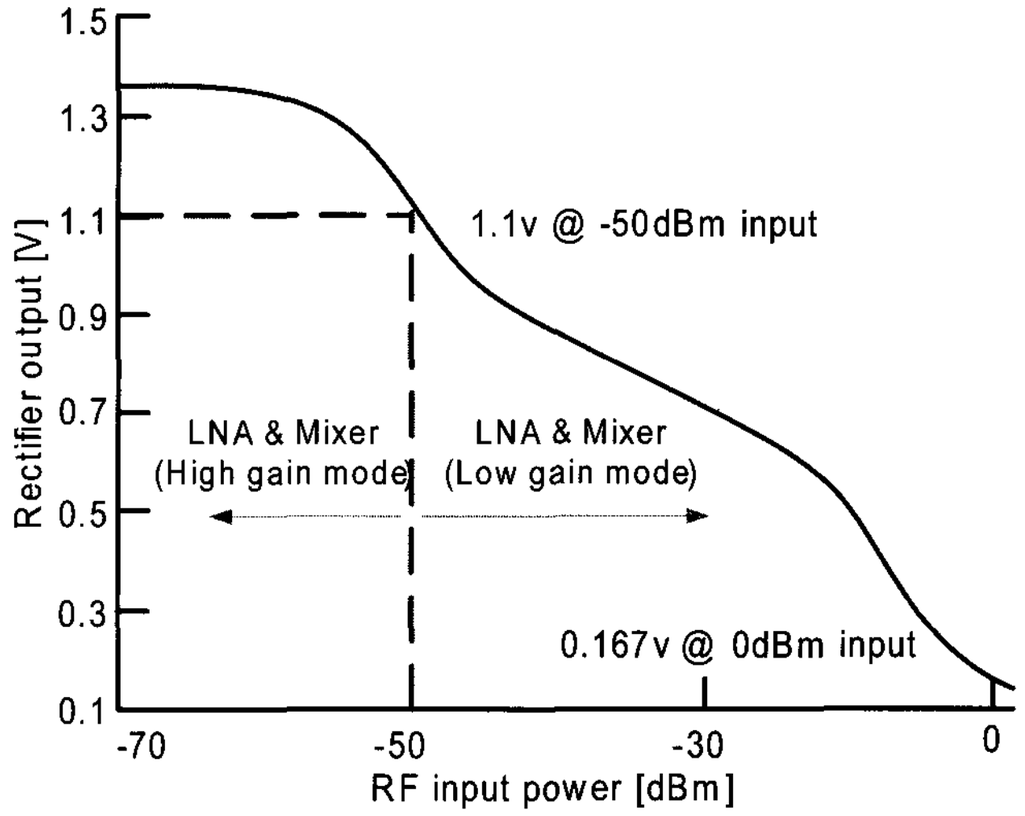


Fig. 12. The measurement results of the IF detector.

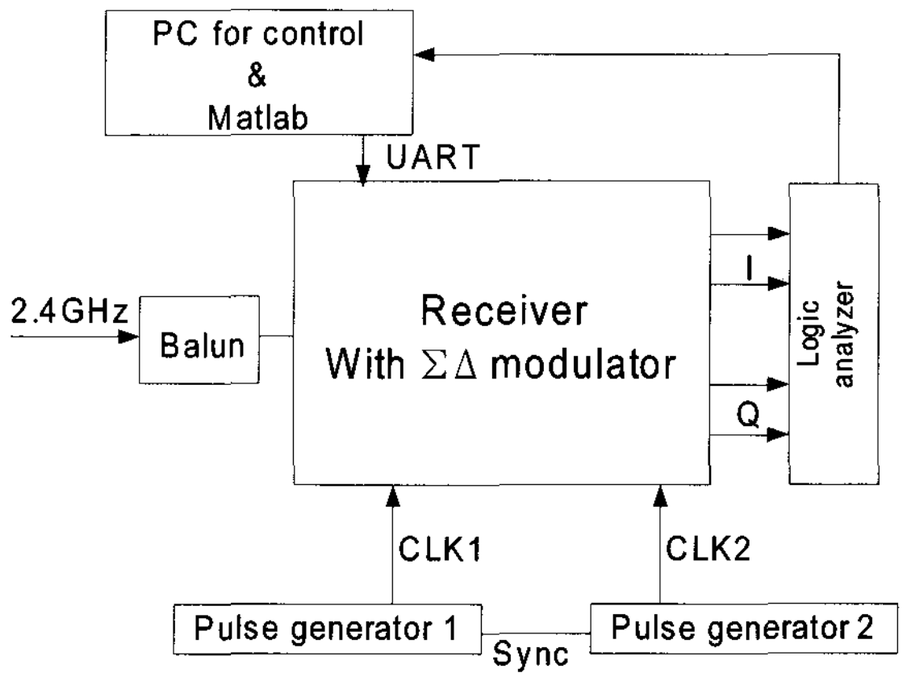


Fig. 13. Measurement setup.

4-2 Chip Performance

Fig. 14 shows the simulated signal-to-noise ratio(SNR) as the amplitude of the input level. An overall receiver DR higher than 95 dB is achieved.

The complex spectrum in Fig. 15 shows the desired complex noise-shaping and IF frequency centered at 2 MHz with 2 MH bandwidth. A block diagram of the digital filter and demodulator is shown in Fig. 16. The I and Q output bit streams from the ADC are clocked at 64 MHz. After filtering and decimation in the cascaded block, the signal frequency is recovered at 2 MHz. Fig. 17 shows the results of the decimator output.

These spectra and waveforms were generated with MatLab using a 16384 FFT and Spectre RF tools. This CMOS receiver using ΣΔ ADC achieves comparable perfor-

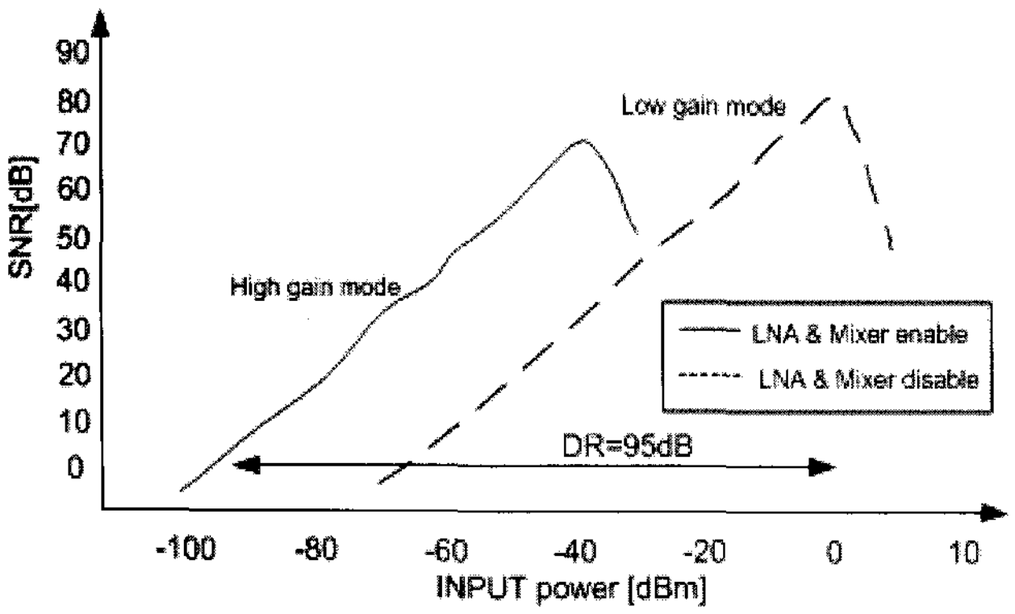
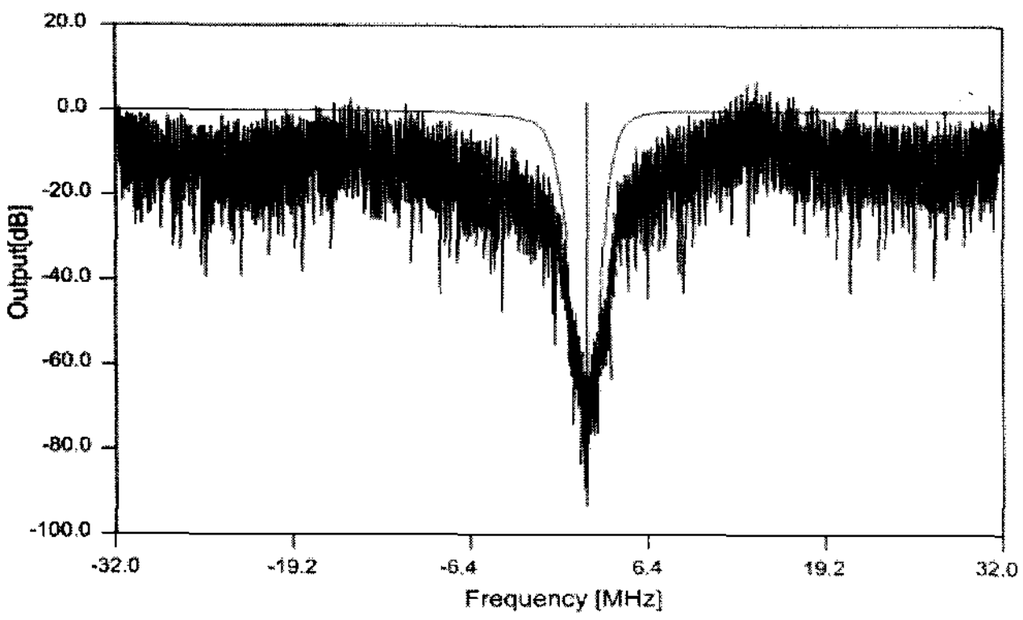
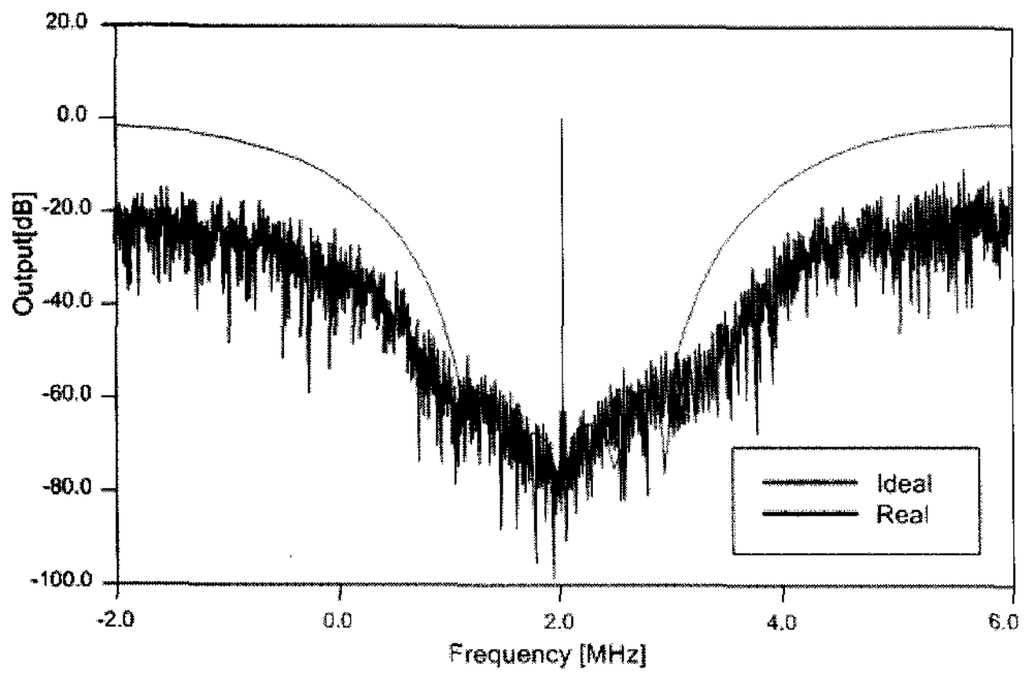


Fig. 14. SNR versus input swing for the overall DR using IF level detector.



(a) Wide view



(b) Detailed view

Fig. 15. Results.

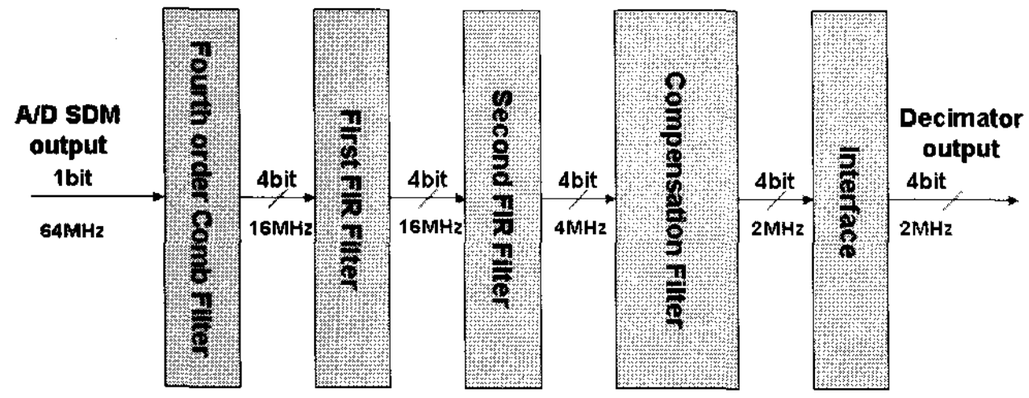


Fig. 16. A block diagram of the decimator.

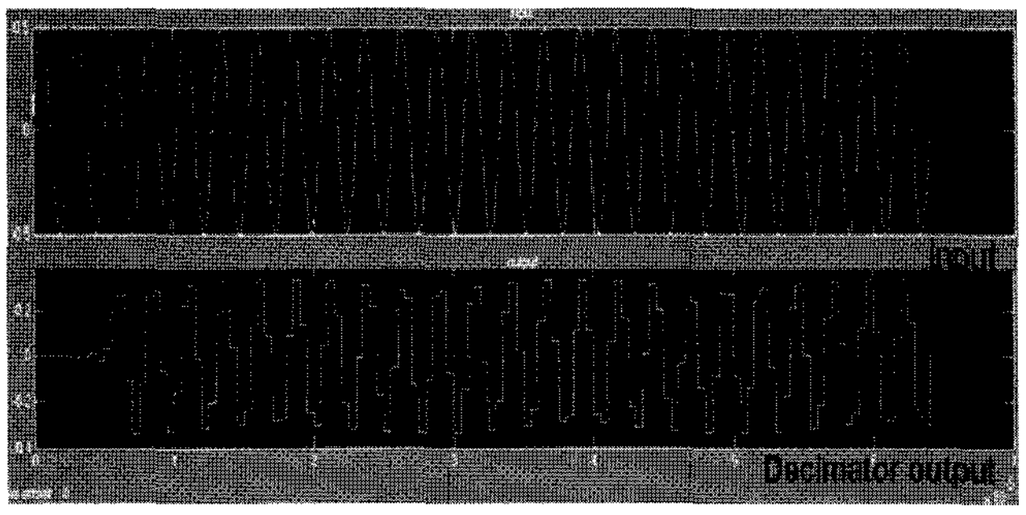


Fig. 17. The output of the decimator.

mance to a conventional receiver. The compared measurement results and the chip photomicrograph are shown in Table 3 and Fig. 18. This receiver has achieved comparable performance to the other receiver using conventional ADC as shown in Table 4[16].

Table 3. Measurement results summary.

	Ref. [2]	Ref. [11]	Ref. [13]	This work	Unit
RF	-	-	-	2.4~2.48	GHz
Type	CT	CT	CT	CT	
Order	4	2	4	5	
IF	0.5	1	0.1	2	MHz
Signal BW	1	1	0.27	2	MHz
Sampling clock	64	100	13	64	MHz
Peak SNDR	-	56.7	78.4	82	dB
Overall dynamic range	89	63.8 (ADC)	-	≥95	dB
Max. Input signal	-	-	3 or 2	1	Vpp
IRR	-	-	-	≥40	dB
Power dissipation @1.8 V	2 (ADC only)	21.8 @2.7V	4.6 @2V	9 (Including RF)	mW
Technology	0.18	0.65	0.25	0.18	
Chip area @ SD ADC	0.14	-	0.389	0.352	mm^2

Table 4. Performance comparison of receivers.

Ref.	Freq. [GHz]	Pro. [μm]	Sensi-vity. [dBm]	Power con. [mW] @ RX (not include PLL)	Chip area [mm^2]
[16]	2.4	0.18	−95	15.6	5.76
This work	2.4	0.18	−94	9	5.7

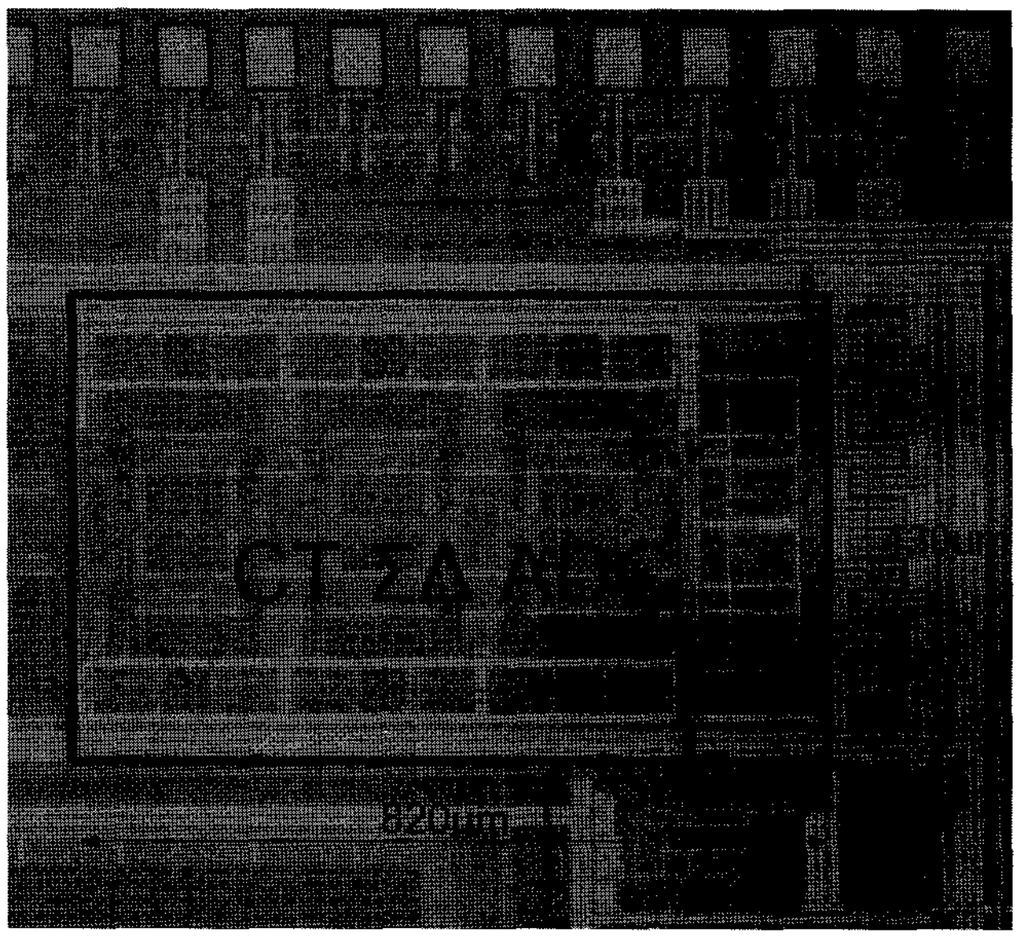


Fig. 18. Chip micrograph.

V. Conclusion

A 9 mW highly-digitized receiver for ZigBee applications in the 2.4 GHz ISM band was realized in 0.35 mm^2 using a 0.18 μm CMOS technology. This modulator has a bandwidth of 2 MHz centered around 2 MHz. The novel receiver architecture is realized by adding the IF level detection scheme to a 5^{th} CT $\Sigma\Delta$ ADC, this results in the input-referred DR of 95 dB at a sampling rate of 64 MHz. The main advantages of the highly- digitized architecture are the simplicity and the low power of the RF front-end, as well as the flexibility in the areas of new wireless standards.

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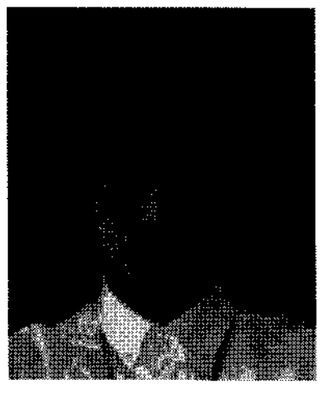

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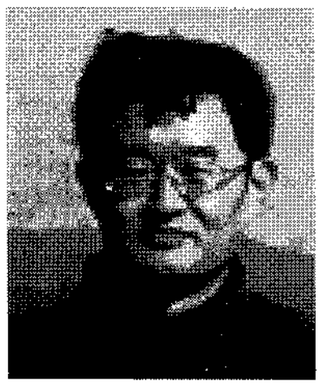

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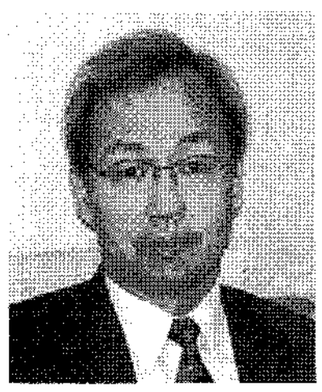

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