# A Study on Improvement of the Channel Efficiency of FH-SS Transceiver Based on DDS Technique

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***Abstract***—A novel high channel efficiency transceiver based on a fast acquisition frequency synthesizer has been designed. The direct digital synthesis (DDS) technique is applied and a simple memory look-up table is incorporated to expedite channel acquisition. The technique simplifies the frequency control process in the transceiver and thus reduces the channel switching time. As a result, the channel efficiency is improved. The designed transceiver is ideal for frequency hopping mobile communication applications.

***Index Terms***—DDS, FH-SS, Transceiver, PLL, Frequency Hopping

## I. INTRODUCTION

Fast switching frequency synthesizer design is important in a frequency hopping spread spectrum (FH-SS) transceiver. Several techniques of frequency synthesis for using in transceiver were proposed. The specifications of frequency synthesis are frequency stability, phase noise, settling time, hopping time. The settling time and hopping time of frequency synthesis are important in the transceiver for high speed communication to improve the channel efficiency. As shown in Fig. 1, the phase locked loop (PLL) technique [1,2] has been used widely in conventional transceiver but is not suitable for the high speed digital communication with FH-SS [3]. Because it has specifications of the high frequency stability, and wide band width, but phase noise is not so good and channel switching time is long causes loop feedback.

Digital signal processor pre-tuned phase locked loop [1] is fast enough to fulfill the requirement of FH-SS but the design requires heavy software and is expensive.

The dual PLL frequency synthesizer [4,5] can virtually reduce the settling time, and hence speeding up the channel switching, by employing two individual PLL to work alternatively. Nevertheless dual PLL frequency synthesizer can not support fast hop. Direct digital synthesizer (DDS) [6-9] is the fastest frequency synthesis technique. We proposed the FH-SS transceiver with DDS frequency synthesizer, and the proposed design is suitable for the existing industrial standards, such as IEEE 802.11 frequency hopping spread spectrum (FH-SS) specification. In the design of a typical 2.4GHz ISM band, 1MHz channel spacing FH-SS transceiver is applied. The settling time of synthesizer for each frequency hop is 200 micro-seconds. If hop rate is higher, more time is spent on channel switching and thus less time can be used for data transmission. The relation channel efficiency, hop rate and settling time of a frequency synthesizer using DDS technique is shown in Figure 10. It is shown that even if the settling of synthesizer is as fast as 50 micro-seconds, the channel efficiency is reduced to 50% while the system is operating at 10,000 hops per second.

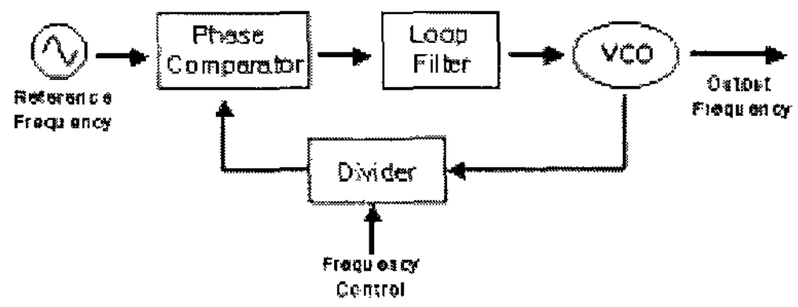


Figure 1. PLL Frequency Synthesizer

## II. Direct Digital synthesizer (DDS) Technique

A DDS is a common component in various communication systems, especially in which fast frequency hopping, low power dissipation, and a narrow resolution are necessary. The DDS is a technique for using digital data processing block to generate a frequency tunable output signal. The major advantage of DDS is the frequency switching speed which is important in spread spectrum or frequency hopping system. The DDS architecture can be implemented from a phase accumulator, ROM look up table, DAC, and Filter, as shown in Figure 2.

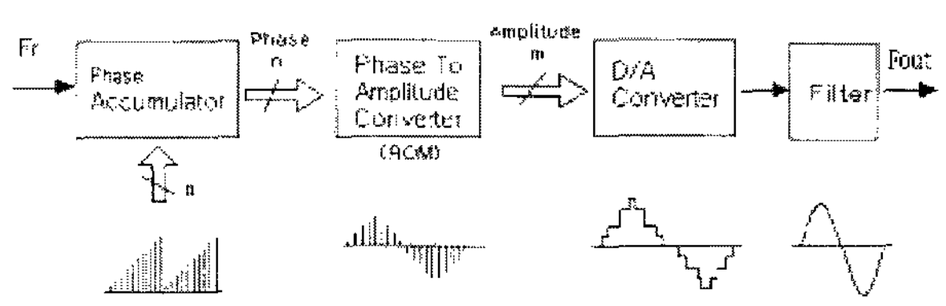


Figure 2. Architecture of Direct Digital Synthesizer

The phase accumulator is implemented with a n-bit adder with the output fed back as one of the input, the other input the phase increment value. Outputs of the adder must be aligned, such that the data is presented as one parallel word to the ROM. This can be accomplished

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by a series of delay elements. The output increases linearly until the accumulator has been reached on the maximum counter and the accumulator starts from zero again. Therefore, the phase accumulator output has been represented as a periodic saw tooth pattern. The ROM is driven by the requirement to maintain a high data throughput. The digital amplitude information that corresponds to a complete cycle of a sine wave is stored in the ROM. The ROM is functioning as a sine lookup table. A ROM converts the digital phase value at the output of the phase accumulator to a digital amplitude value according to the sine lookup table in the ROM.

The DAC has the unique capability to transform the digital information to the analog signal [9,10]. Especially, the vertical resolution of the DAC determines the quality of the analog signal.

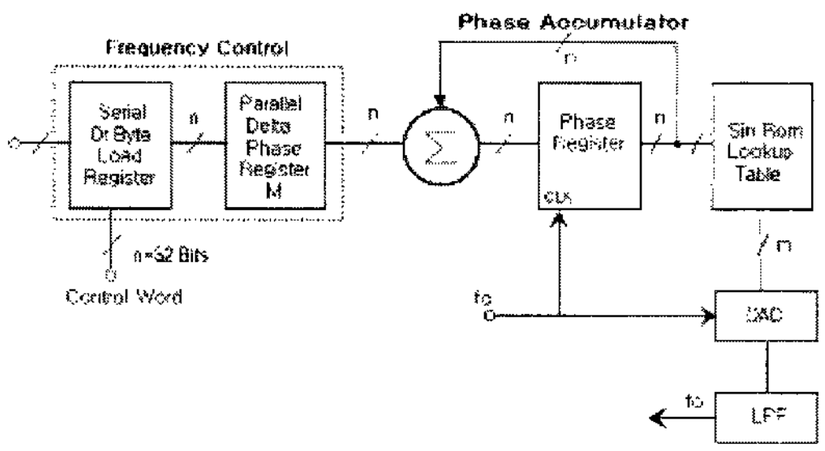



Figure 3. Functional Block Diagram of DDS

## III. DESIGN AND RESULTS OF DDS

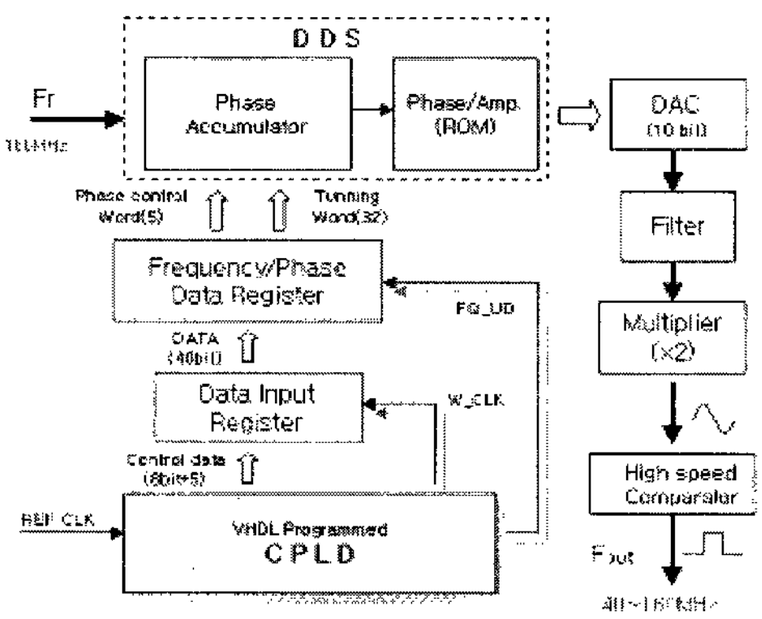
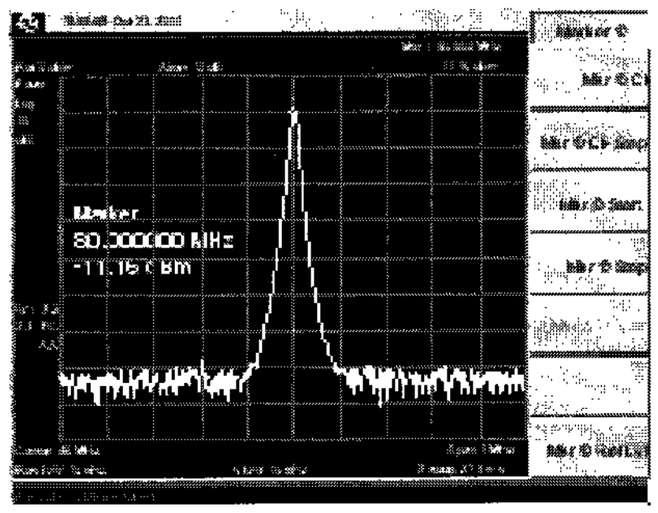


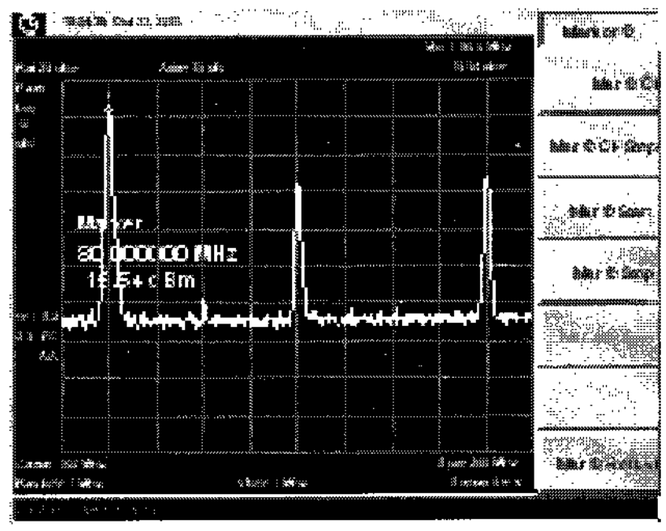

Figure 4. Architecture of Frequency Synthesizer

In this paper, we designed the frequency synthesizer using the DDS technique that generates the frequency from 40MHz to 160MHz with the 200KHz channel spacing and 1600 hops per second speed. The architecture of synthesizer is as shown in figure 5. The frequency resolution of synthesizer is 0.0372529Hz $(160\times10^6/2^{32})$ because reference clock is 160MHz and tuning word is 32bit. Output frequency of DDS is controlled by VHDL program in CPLD.

Output spectrum at 80MHz of the designed synthesizer is shown in Figure 5(a), and frequency harmonics of output are shown in Figure 5(b), Also, Figure 6 is photograph of designed board.



(a) Fundamental Output Spectrum at 80MHz



(b) Harmonics of Fundamental Frequency

Figure 5. Spectrums of the designed DDS

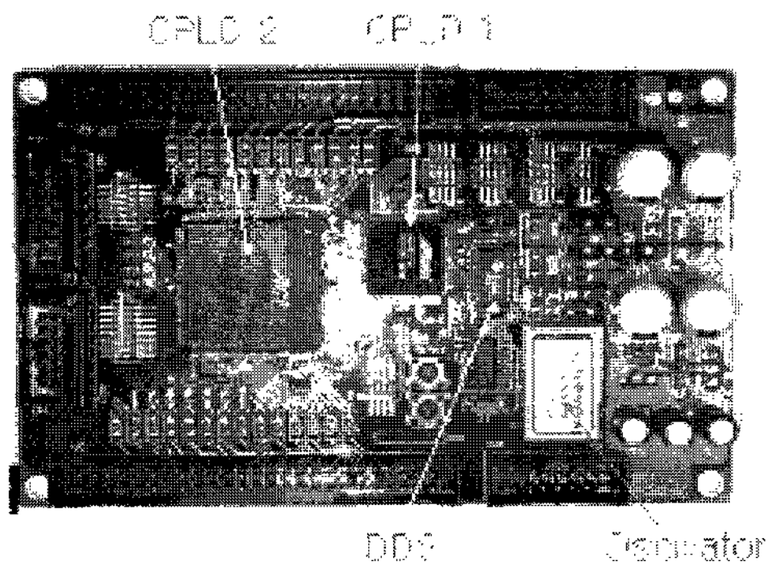


Fig. 6 Photograph of Designed Board

## IV. Design and performance of Transceiver

The target design specifications are listed below:

- Operating Frequency : 2400 to 2480MHz
- Frequency Error : +/-50KHz
- Channel Spacing : 1MHz
- Transmitting power : +20dBm (0.1W)
- Data rate : 1Mbps
- Channel efficiency : 90% at 20K hops per second
- Receiving Sensitivity : -90dBm
- Adjacent Channel rejection : 30dB
- Supply voltage : 3.0V

The receiver design is of single conversion super-heterodyne structure. The sensitivity and selectivity is

well proven. The IF frequency is 110MHz. The simple LC filter to be applied in the RF front end for sufficient image rejection. In the transmitter design, direct frequency modulation is adopted. The VCO operates at half of the transmission frequency. The output signal of the VCO is frequency doubled, filtered and then amplified for transmission. In the frequency synthesizer design, PLL structure is attractive due to the advantages of low power consumption and low spurious radiation. The direct access frequency synthesizer is designed on the top of PLL. To minimize the channel switching time during each frequency hop, special data conversion and memory access circuits are designed and inserted between the loop filter and the voltage controlled oscillator as shown in Figure 8.

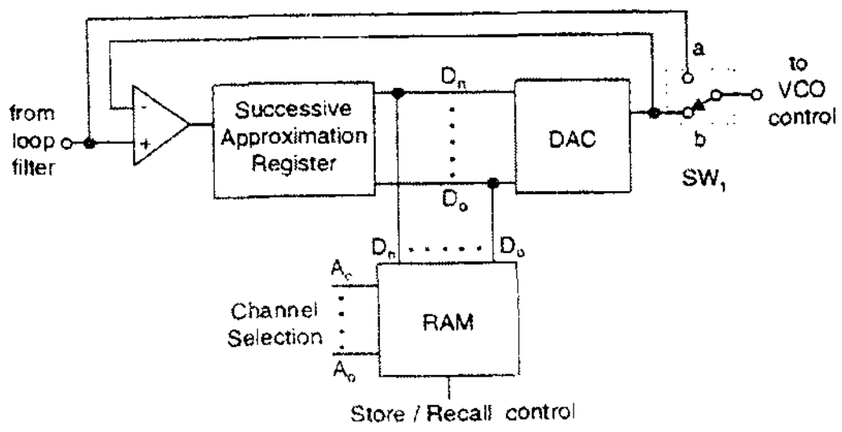



Figure 7. Data conversion and memory access circuit

During the normal mode, the VCO is operating under open loop control. The noise sources of the frequency synthesizer are shown in Figure 9. The output noise spectrum can be expressed as in (1)

$$\eta_s = \varphi_v(s) + K\varphi_{DAC}(s) \quad (1)$$

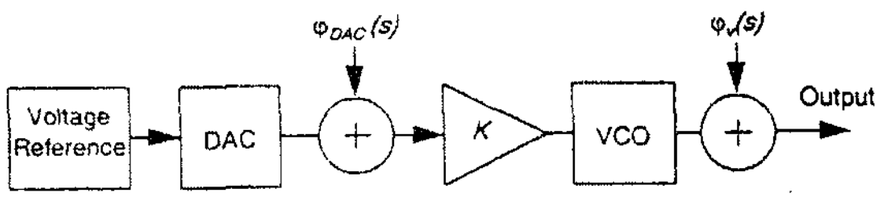
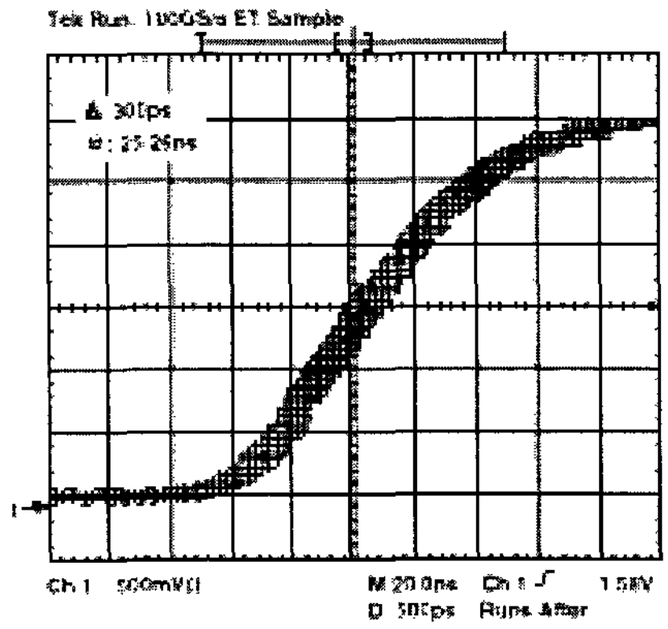
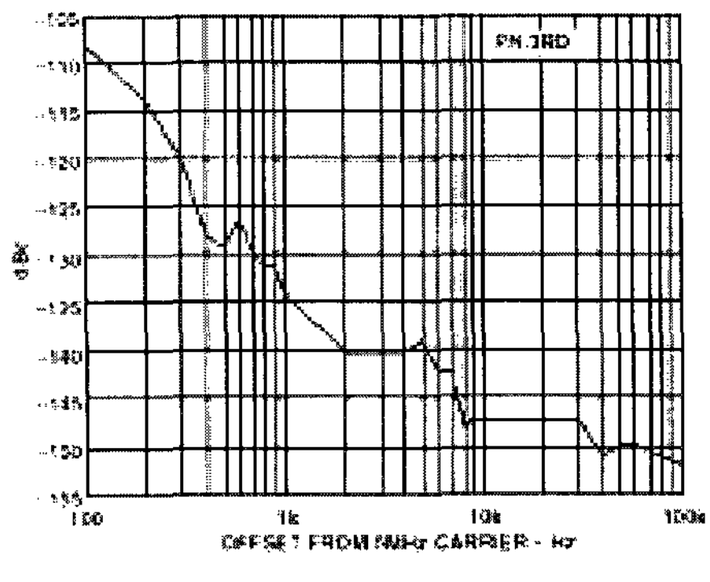



Figure 8. Noise source in Transceiver

To minimize the phase noise of transceiver, the DAC should be operated in low noise condition. Also, high stability reference voltage source and high quality power supply are the critical factors. Since there is no close loop control, the phase noise created by the control loop, such as the reference spur and the phase noise shoulder, is no longer exist. In the prototype, the high side (10 KHz or higher offset from the carrier) phase noise in normal mode is about 3dB lower than that of calibration mode. In the prototype, it can be found that the dominant phase noise is concentrated below 10 KHz. The noise mainly comes from the VCO control voltage, that is, created by the DAC and the voltage buffer. The noise increases the residual FM to around 10 KHz, which is much higher than that if in close loop. To reduce residual FM, low noise DAC and operational amplifiers should be applied. An advantage of applying direct frequency synthesizer in the transceiver is that the modulation bandwidth is larger. Since the VCO is under open loop control, the modulation bandwidth is no longer limited by the PLL bandwidth. As a result, rate can be transmitted without distortion.



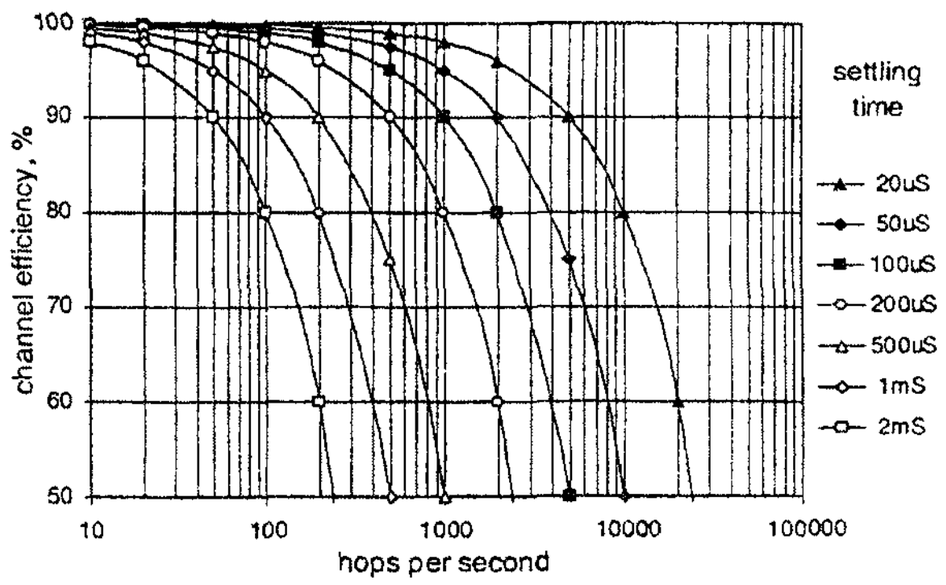
(a) Output Jitter (@$f_{out}$=40MHz)



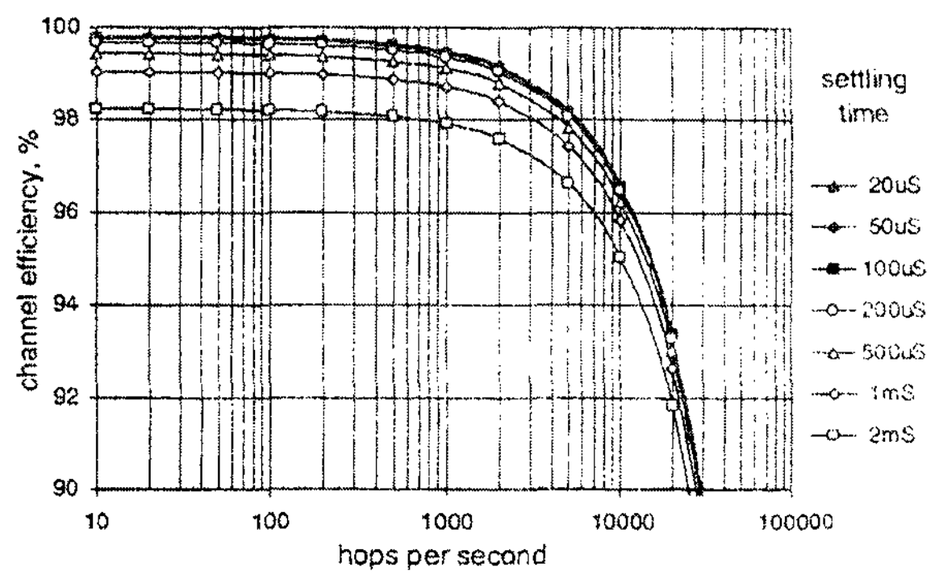
(b) Output Residual Phase Noise(@$f_{out}$=40MHz)

Figure 9. Phase noise of the transceiver

The resolution of the digital-to-analog converter (DAC) is 16 bits. In the application of 80MHz frequency range and 3X tuning window, the 16 bit DAC provides frequency resolution as fine as 5 KHz. The settle time of the DAC is 5 micro second. Together with the response time of the VCO and the access time of the RAM, channel switching in within 10 micro seconds is achievable. At the beginning, the RAM does not have any information about the VCO control voltage of each channel frequency. To learn the control voltage, self-calibration is needed. The successive approximation register (SAR) works incorporate with the DAC to form a successive approximation analog-to-digital converter (ADC). After self-calibration, the frequency synthesizer operates in normal mode. In this mode, the DAC is directly driven by the RAM using parallel address lines[11,12]. In this way, the access time is much shorter than that of the conventional serial control PLL. As a result, channel switching is much faster. More time can be used for data transmission. Channel efficiency is improved as shown in Figure 11.




(a) Conventional serial control PLL




(b) Designed transceiver with DDS

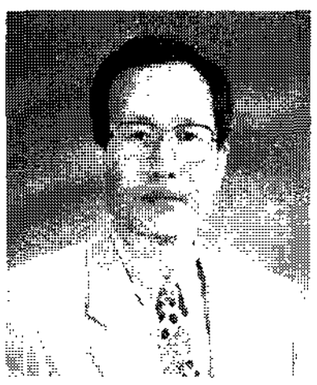
Figure 10. Channel efficiency of frequency synthesizer on different hop rate

## V. CONCLUSIONS

A conventional PLL transceiver needs to undergo thousand cycles of frequency acquisition every second, hence the accumulated channel switching time for channel switching is exceedingly large. In contrast, the proposed transceiver will calibrate the control voltage of each channel only once during the calibration period. When calibration period is longer, the channel efficiency increases. In the example of IEEE802.11 FH-SS specification at 2.4GHz, the proposed transceiver spends total time of 100ms on self-calibration for 80 channels in calibration period of five seconds. The redundancy is only 2%. Although the technique is simple, the successful application reveals vital implication in engineering.

## REFERENCES

[1] Phase-Locked Loop Design Fundamentals, Applications Note An-535, Motorola Inc
[2] F. M. Gardner, Phase Lock Techniques, 2nd Edition, John Wiley, NewYork, 1979.
[3] C. M. Yuen, "One microsecond fast acquisition 2.4GHz low voltage frequency synthesizer for frequency hopping spread spectrum mobile communication," Proceedings of IEEE TENCON'97, pp.501-504, Dec. 1997.
[4] A. Kajiwara, "A new PLL frequency synthesizer with high switching speed," IEEE Trans. Veh. Technol., vol41, pp.407-413, Aug. 1992.
[5] F. A. B. Cercas, M. Tomlinson, A. A. Albuquerque, "Direct digital frequency synthesizer for a FH spread spectrum system: analysis and design," IEEE ITS 90 Record, pp. 19.4.1-19.4.5,1990.
[6] N. M. Filiol, C. P. Plett, T. A. D. Riley, M. A. Copeland, "An interpolated frequency hopping spread spectrum transceiver," IEEE Trans. Veh. Technol., vol45, pp.3-11, Jan. 1998.
[7] Henry T. Nicholas III, Henry Samueli, An Analysis of the Output Spectrum of Direct Digital Frequency Synthesizers in the Presence of Phase-Accumulator Truncation, IEEE 41st Annual Frequency Control Symposium Digest of Papers, 1987, pp.495-502.
[8] K. J. Song, "DC-2.GHz Frequency Synthesizer Based on Frequency Multiplied DDS and Offset Mixing for Low Phase Noise," Doctoral Dissertation, Kwangwoon University, 2005.
[9] Henry T. Nicholas III, Henry Samueli, The Optimization of Direct Digital Frequency Synthesizer Performance in the Presence of Finite Word Length Effects, IEEE 42st Annual Frequency Control Symposium Digest of Papers, 1988, pp.357-363
[10] D.F. Hoeschele, Analog-to-Digital and Digital-to-Analog Conversion Technique, 2nd Edition, John Wiley & Sons, Inc., New York, 1995.
[11] J. A. Connely and K. P. Taylor, "An analysis methodology to identify dominant noise sources in D/A and A/D converter," IEEE Trans. Circuit Syst. Vol38, No. 10, Oct. 1991.
[12] K. M. Daugherty, Analog-to-Digital Conversion, McGraw-Hill, Inc., 1995.



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