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Development of an Ultra-Slim System in Package (SiP)

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Abstract: This paper reviews the current development of an ultra-slim SiP for Radio Frequency (RF) application, in which three flip chips, additional passive components and Surface Acoustic Wave (SAW) filters are integrated side-by-side. A systematic investigation is carried out for the design optimization, process and reliability improvement of the package, which comprises several aspects: a design study based on the 3D thermo-mechanical finite element analysis of the packaging, the determination of stress, warpage distribution, critical failure zones, and the figuration of the effects of material properties, process conditions on the reliability of package. The optimized material sets for manufacturing process were determined which can reduce the number of testing samples from 75 to 2. In addition the molded underfilling (MUF) process is proposed which not only saves one manufacturing process, but also improves the thermo-mechanical performance of the package compared with conventional epoxy underfilling process. In the end, JEDEC's moisture sensitivity test, thermal cycle test and pressure cooker tests have also been carried out for reliability evaluation. The test results show that the optimized ultra-slim SiP has a good reliability performance.

Keywords: RF Module, SiP, Flip chip, Thermo-mechanical simulation, Reliability test

1. Introduction

The demands for higher level integration, lower costs, and smaller size on mobile electronic devices, such as cell phones, digital cameras, and portable audio players, have continued to drive the development of SiP solutions. SiP is an advanced technology to incorporate multiple components into a single package, the products of which are fully functional systems or sub-systems in IC package format. SiP may contain one or more IC chips plus other components that are traditionally found on the system mother board. Compared with the conventional single chip package or System on Chip (SoC) solution, SiP has the following advantages:

- Smaller size
- Reduced time to market
- Higher performance
- Lower system cost
- Better assembly efficiency
- Known good modules

Therefore, the development of SiP has been growing extremely fast in recent years[1-14].

In the current development of an SiP module, a

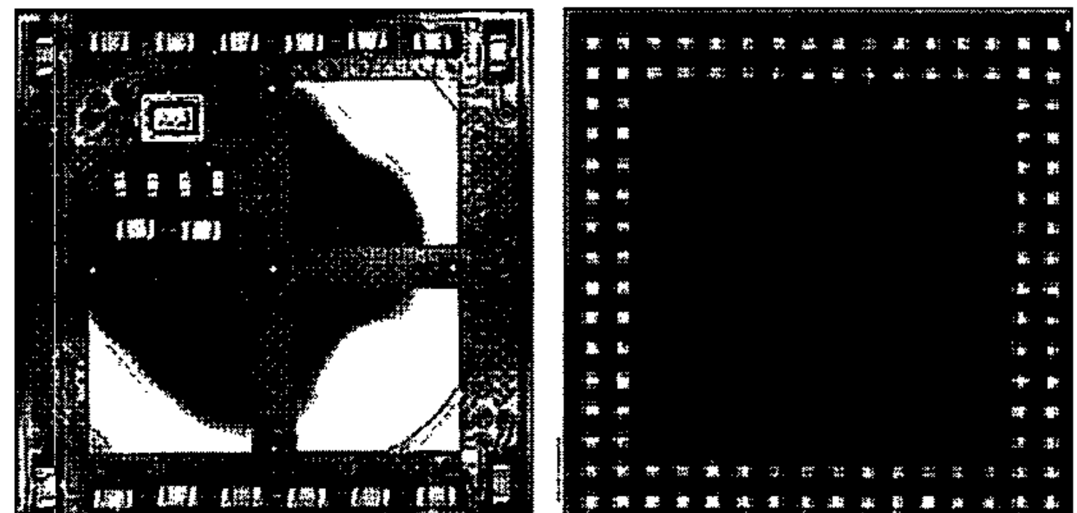

Fig. 1. The developed SiP for RF application

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miniature SiP RF module, which has an ultra-slim structure, is needed to be designed and manufactured. An RF module is a device that takes a baseband input signal and outputs a radio frequency modulated signal. This is often a preliminary step in transmitting signals, either across open air via an antenna or transmission to mobile device. This paper describes the development processes and discusses the crucial consideration required in designing, assembling and testing of such complicated SiP module.

The prototype of the SiP module is shown in Fig. 1. The dimension of the package is 11 mm*11 mm* 1.2 mm, with 112 peripheral I/Os. Inside the module are three flip chip dies with same dimensions of 3.5 mm*3.5 mm*0.15 mm. The functions of these three chips are for power management, memory and Baseband (BB)+RF chips. All the three dies are attached with the flip-chip technique with lead free solder bumps. Many challenges have to be faced in the development of such modules. There is a risk of unacceptably low manufacturing yield since three flip chips are attached on the same substrate. Another big challenge in this development is how to integrate so many package components in such a slim structure with a robust reliability.

2. Manufacturing Processes

The whole manufacturing processes of SiP module are shown in the flow chat (Fig. 2). Wafer is first inspected, bumped, tested, thinned and diced into functional chips before the further packaging

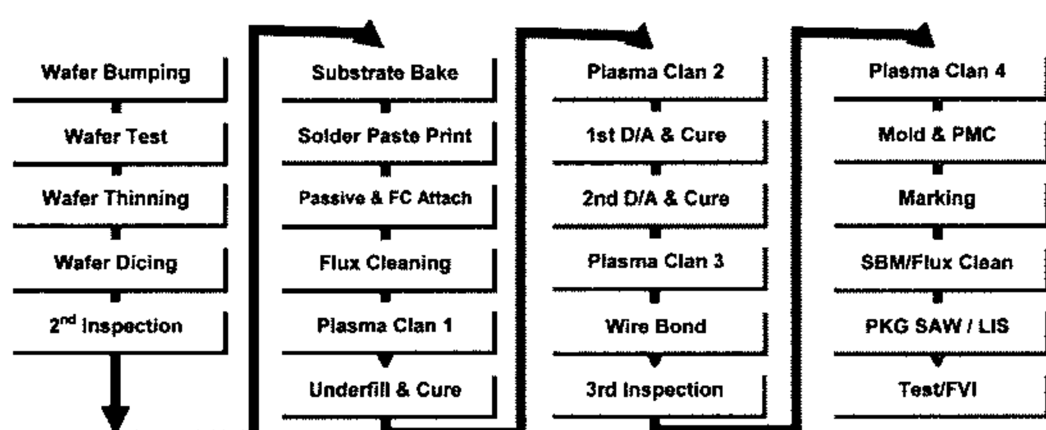


Fig. 2. Flow chat of SiP Manufacturing processes

processes. The next a few steps are Surface Mount Technology (SMT) processes, including substrate preparation, solder paste printing, passive & flip chip attaching and reflowing. After that are the encapsulation processes including underfilling & curing, moulding & Post Mold Curing (PMC) processes. In the end, the package is marked, tested and sawed into pieces.

It should be mentioned that for flip chip package structure Coefficient of Thermal Expansion (CTE) mismatch between the die (2.5 ppm/°C) and substrate (13.5 ppm/°C) can cause significantly localized thermal strain/stress during board level reflow process and ultimately may result in failure of the package, such as die crack and substrate delamination. To prevent this, underfilling process is introduced. The underfill between the die and substrate provides two functions, bonding and encapsulation. The underfill material decreases the stress of solder bumps and thereby increases the reliability performance of the package. Proper selection and evaluation of the underfill materials are important to optimize the assembling process and the reliability performance of SiP.

3. Thermo-mechanical Simulation

As the design of package becomes more compact to meet the development trend for mobile components, thermo-mechanical analysis must be carried out to ensure the reliability of the final products. As a result, although SiP brings numerous advantages in terms of size, performance and cost, in order to achieve good design and speed up time to market, concurrent design in thermo-mechanical aspects must be taken into consideration at initial design stage through accurate and efficient modeling and simulation. Also, co-design in packaging structure, material selection and manufacturing process is required to optimize the performance, size, manufacturability and reliability performance of SiP[15-20].

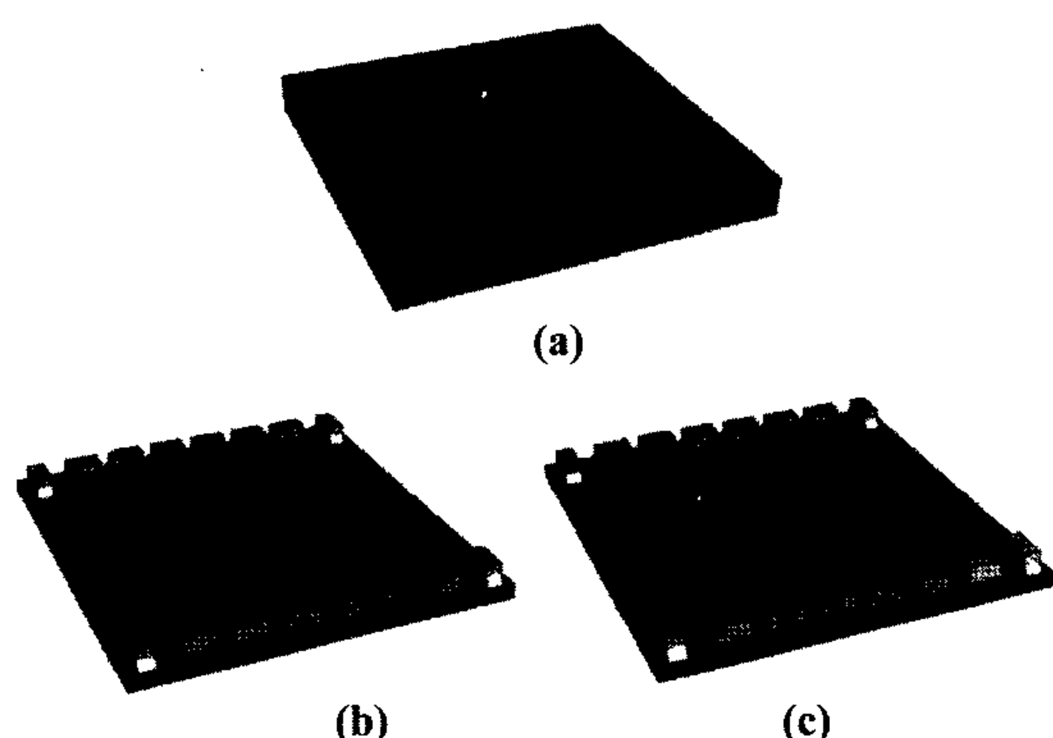


Fig. 3. Geometry structure of SiP: (a) Whole package (b) before encapsulation (c) Without chips

3.1 Finite Element Method (FEM) Model

3D FEM model of SiP module is constructed in Fig. 3, which shows the layout of each package components used in this analysis. There are power management and BB+FR dies each with 56 I/Os and one memory die with 144 I/Os. The passive components, embedded in the package besides a silicon chip, are SAW filters, inductors and capacitors, which are mounted on the substrate with chip side by side. The design and layout of the package are shown with detail in Fig. 3. Organic Printed Circuit Board (PCB) is chosen as the substrate material, SnAgCu (SAC) is the solder material. The gap between die and substrate is filled with underfill material and the package is encapsulated with Epoxy Molding Compound (EMC).

Elastic material properties for the die, EMC, underfill, solder and substrate are considered. The temperature dependent modulus of underfill and EMC materials is used for the simulation. The CTE and Tg values for EMC and underfill materials are measured with TMA and DMA, respectively.

N2 profile is considered for solder reflow process (shown in Fig. 4). The peak temperature is 245°C. The stress-free status of the package is assumed to be at the peak temperature during reflow process. After the reflow, the package is cooled to room

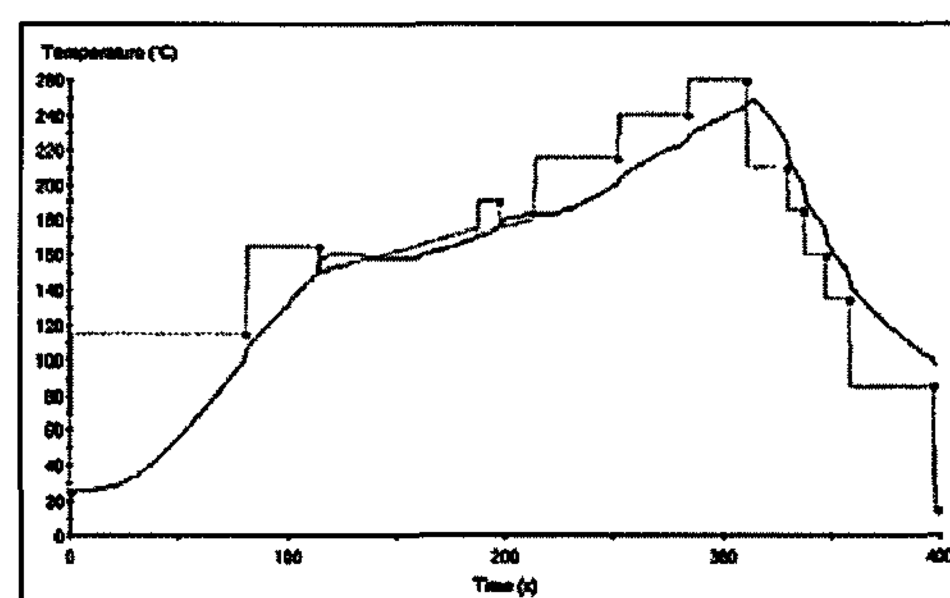


Fig. 4. Temperature profile in reflow process

temperature. This study focuses on the thermo-mechanical behaviors of the package after cooling. Thermo-mechanical FEM analysis is conducted using Abaqus standard v6.6 [21].

3.2. Standard Model Analysis

The benchmark analysis is firstly considered. This analysis is to be used as a reference for the following material and process optimization. The material set is chosen as the initial prototype of the package, in which underfill, EMC, substrate and Sn3.5Ag0.5Cu lead free solder are used. The material properties are given in Table 1. Since the property of underfill material is temperature dependent, only the properties at 25°C are listed in the table.

Fig. 5 shows the warpage distribution of package components after reflow process. Some of the components are taken out from the assembled model

Table 1. Material properties of packaging components

Material	Young's Modulus (GPa)	CTE (ppm/°C)	Poisson's ratio	Tg (°C)
Die	130	2.6	0.27	
EMC	12.6 (<Tg) 1.42 (>Tg)	9 35	0.25	189
Underfill	6.23 (25°C)	29 117	0.33	142
Substrate	26	14	0.17	
Passive	370	7.4	0.22	
Solder	56	20.04	0.35	

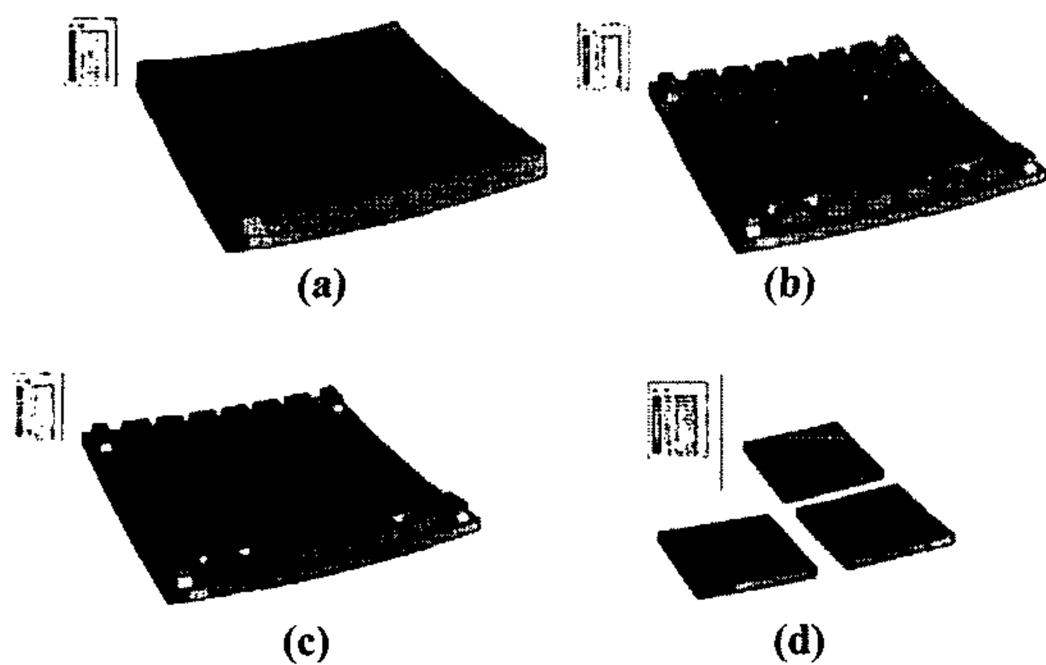


Fig. 5. Warpage distribution of package components after reflow: (a) Whole package, (b) without EMC, (c) Without dies, and (d) pure three dies.

in order to see the deformation inside the package more clearly. It can be seen that the warpage is smile shaped with its value at a relatively high level (140 μm) due to the ultra-slim package design. The maximum warpage occurs at the four corners of the substrate. The warpage decreases when the position is close to the central part of the package. Therefore, the dies should be designed to be located near the central of the package in order to reduce the overall warpage.

Fig. 6 shows the Mises stress distribution of package components after reflow process. It can be seen that there are stress concentration zones for each components of the package. The maximum stresses occur: for solder bumps, at the first and second solder bumps under the BB+RF dies which are close to the corner of the dies; for dies, at the four corners which contact with underfill; and for the passive components, at the four corners which are in contact with molding compound.

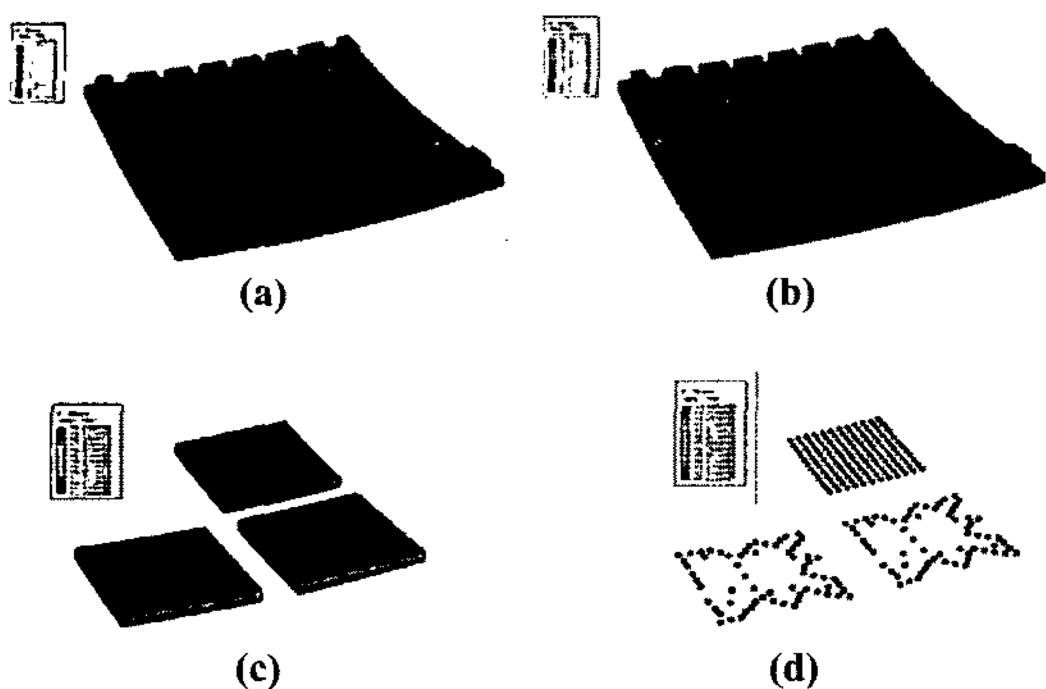


Fig. 6. Mises stress distribution of package after reflow: (a) Without EMC, (b) Without dies, (c) pure dies and (d) Solder bumps

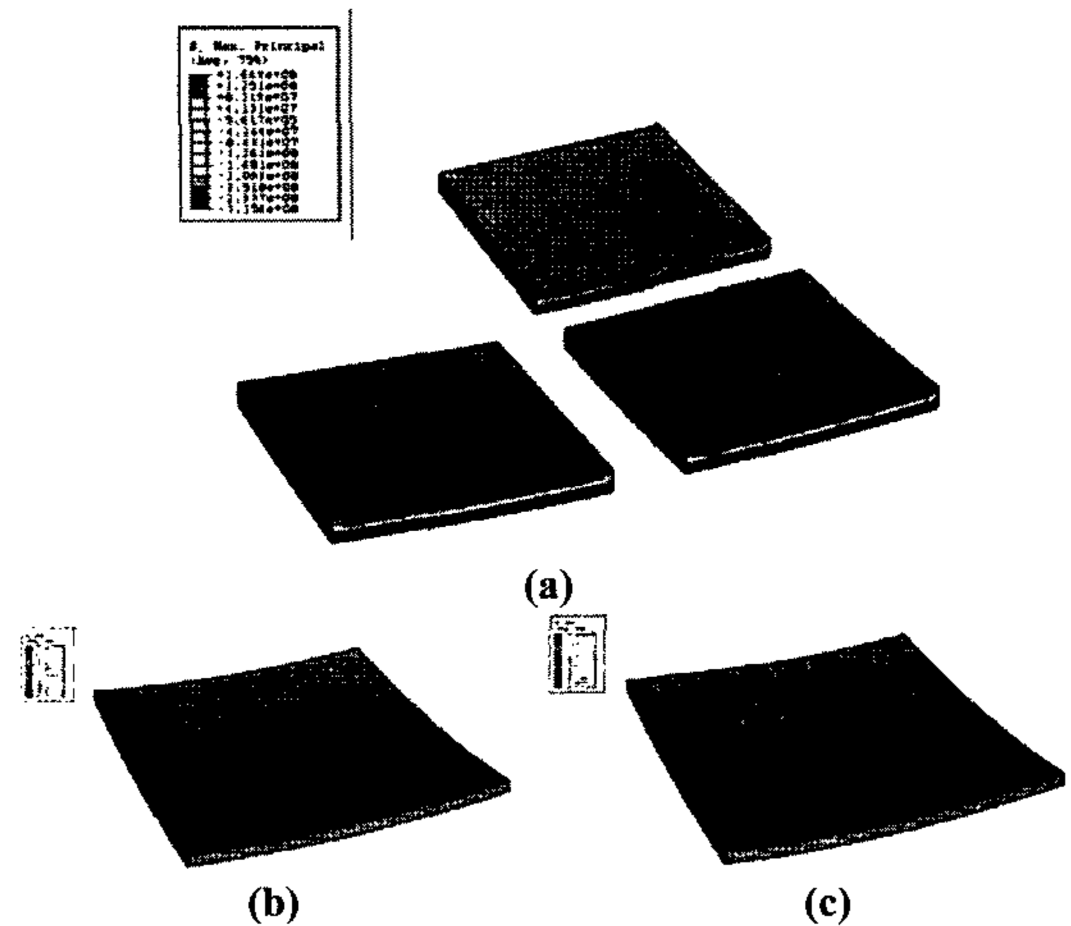


Fig. 7. Stress distribution of package components after reflow: (a) Maximum principle stress of die (b) Shear stress S_{13} (σ_{xz}) of substrate (c) Shear stress S_{23} (σ_{yz}) of substrate

3.3 Material Parametric Study

There are two main failure modes of SiP module, i.e. die broken which is caused by the maximum principle stress and interface delamination which is caused by the maximum shear stress. Fig. 7 shows the principle stress distribution of the die and shear stress distribution on the substrate, respectively. The Maximum Principle Stress (MPS) lies on the bottom of the die where it contacts with the underfill, especially in the central part of die. The Maximum Shear Stress (MSS) on the substrate lies in the area where it contacts with underfill material, especially at the boundary area of the underfill. The absolute values of the two shear stresses S_{13} (σ_{xz}) and S_{23} (σ_{yz}) are almost the same while the directions are perpendicular. The areas where substrate contacts with passive components also show stress concentration although the absolute value of which is not so

high as that of the area contacting with underfill.

3.3 Material Parametric Study

There are many material candidates for manufacturing each component of the SiP module. Conventionally, process engineers have to test each material candidate to find out the optimized material set during development stage of package. However, SiP contains various materials due to its complexity structure, the key materials of which are underfill, EMC and substrate. If there are a few candidates for each material, testing all candidate material set for evaluation may cost too much, take too long time, and in some cases almost impossible. Mechanical simulation, to some extend, can replace the real process for evaluating the performance of each material candidate. The advantage of simulation is that arbitrary packaging structure can be analyzed for any material behaviors and loading conditions fast and efficiently.

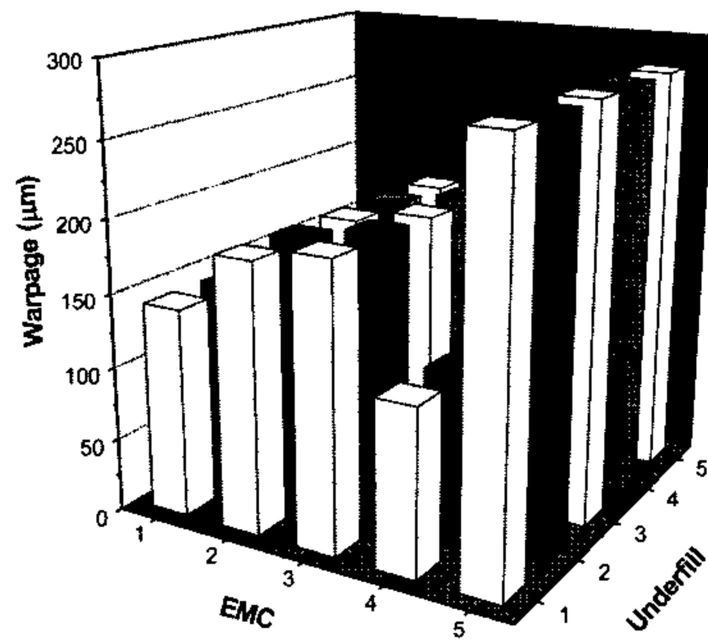
In this study, underfill, EMC and substrate material properties are considered for evaluation. There are 5 underfill materials, 5 EMC materials and 3 substrate materials from various suppliers. Among the three substrate candidates, the first two are organic substrates and the last one is LTCC substrate. The properties of all material candidates are listed in Table 2.

Table 2. Properties of material candidates for Underfill, EMC and Substrate

Material		Young's Modulus (GPa)		CTE (ppm/°C)	Poisson's ratio	Tg (°C)
Underfill	1	6.23 (25°C)	< Tg	29	0.33	142
			> Tg	117		
	2	8.7 (25°C)	< Tg	27	0.33	137
			> Tg	90		
	3	8 (25°C)	< Tg	30	0.33	85
			> Tg	120		
	4	11 (25°C)	< Tg	22	0.33	135
			> Tg	90		
	5	10 (25°C)	< Tg	25	0.33	110
			> Tg	93		
EMC	1	12.6	< Tg	9	0.25	189
		1.42	> Tg	35		
	2	17	< Tg	9	0.25	140
		0.4	> Tg	40		
	3	24	< Tg	9	0.25	145
		0.8	> Tg	43		
	4	27	< Tg	10	0.25	150
		1.8	> Tg	30		
	5	10	< Tg	13	0.25	55
		0.27	> Tg	55		
Substrate	1	26		14	0.17	220
	2	29		11	0.17	260
	3	150		6	0.2	650

Warpage behavior is considered firstly. Fig.8 shows the relationship between warpage of the package and underfill-EMC material with 3 substrate candidates (1), (2) and (3). Only tiny difference can be observed for the 5 underfill candidates. Substrate material has some effect, but not significant effect on the warpage of the package. Warpage is higher for LTCC substrate than that of organic substrate. This is due to the reason that compared with organic substrate CTE of LTCC is much smaller than that of EMC.It is the CTE mismatch which significantly causes the thermal stress and warpage for the package. The higher the CTE difference between the two materials is, the higher the warpage. EMC, however, plays the key role in determining the overall warpage of the package. The EMC No.4, which has smaller CTE and higher Tg value, achieves the smallest warpage value among the 5 EMC candidates. The warpage value of the package can be controlled as small as 100μm by the use of EMC candidate No.4 compared with 300μm for EMC candidate No.5.

The stresses in the die are considered. Fig. 9 shows the relationship between MPS in the die and underfill-EMC material with 3 substrate candidates (1), (2) and (3). Compared with warpage, the effect of materials on MPS is more complicated. The three kinds of packaging materials are coupled together



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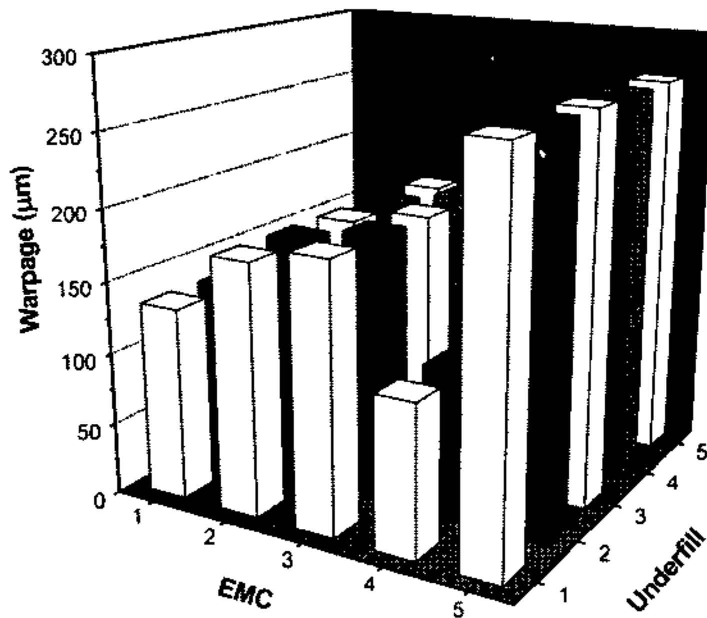

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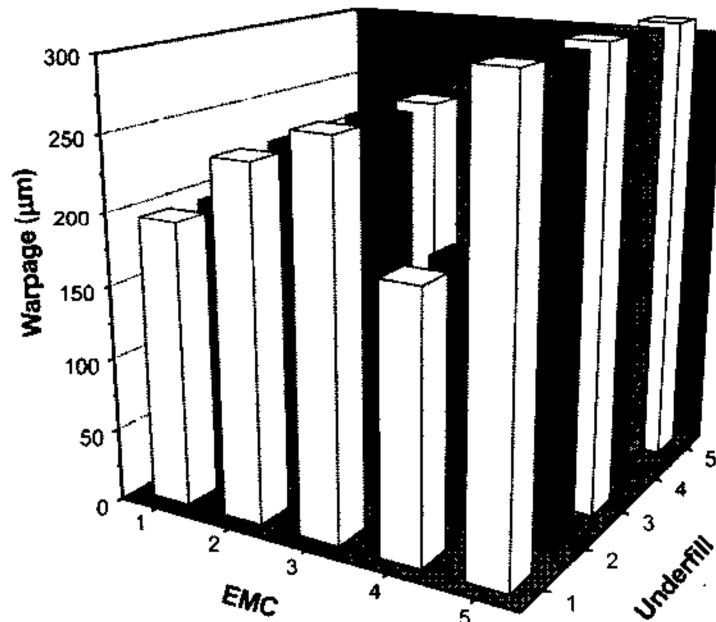

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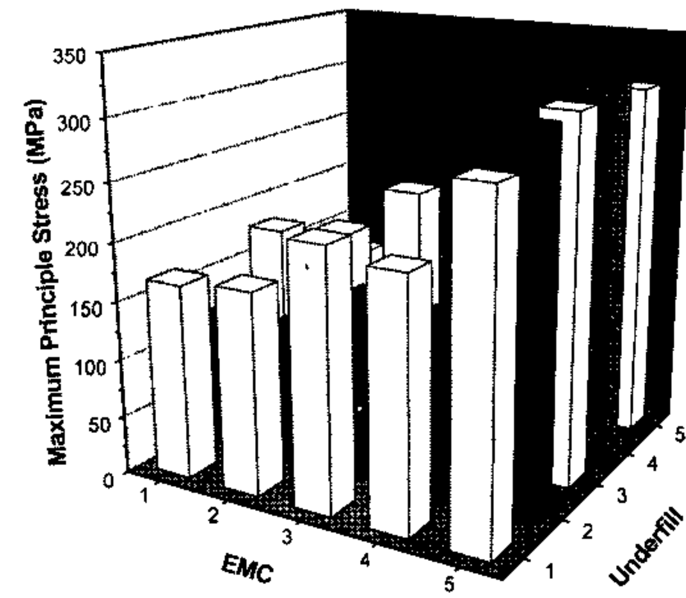
Fig. 8. The relationship between the warpage of the package and underfill-EMC with 3 substrates (1), (2) and (3)



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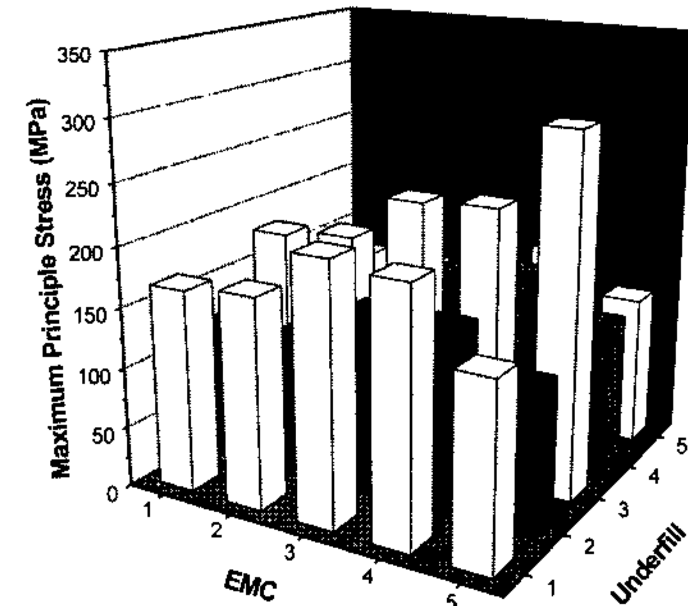

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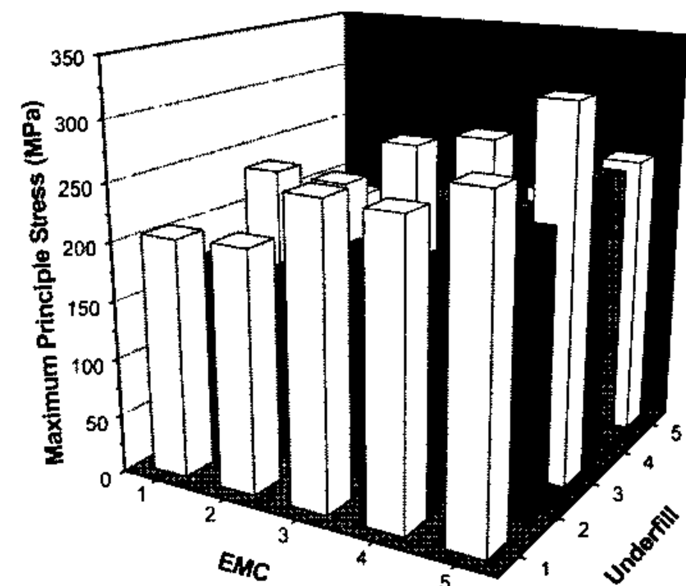
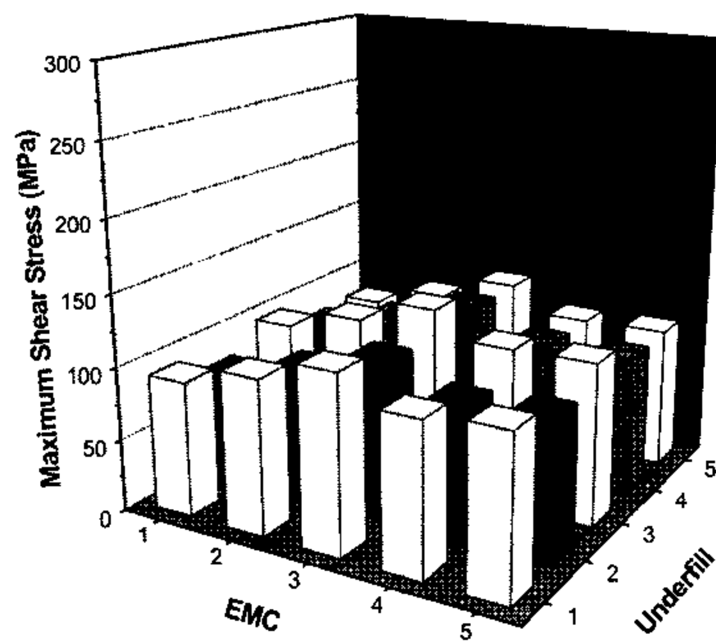


(3)

Fig. 9. The relationship between the maximum principle stress of the die and underfill-EMC with 3 substrates (1), (2) and (3)

and play the same important role in determining the MPS of the die. The EMC candidate No.5 always induces high MPS for substrate No.1 while it does not cause high stress for substrate No.2 except with underfill candidate No.4. For substrate candidate No.2, underfill No.2 and No.5 achieve the smallest MPS of the die. Higher stress can also be observed for LTCC substrate than that of organic ones. In general, substrate No.2 induces smaller MPS than substrate No.1 does.

Shear stresses on the substrate are considered. Fig. 10 shows the relationship between MSS of the substrate and underfill-EMC materials with substrate candidates (1), (2) and (3). Substrate plays the dominating role in determining the MSS among packaging materials. LTCC substrate causes almost double value of MSS than that of the other two substrates. MSSes with underfill No.2 and No.5 are



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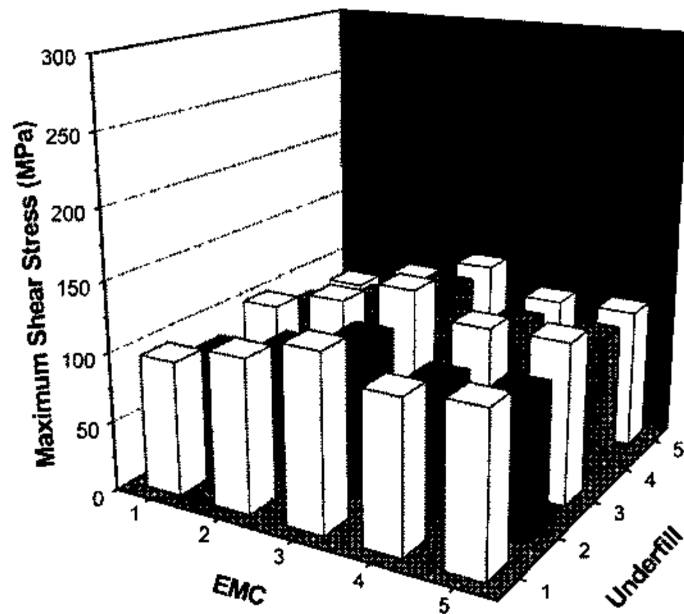

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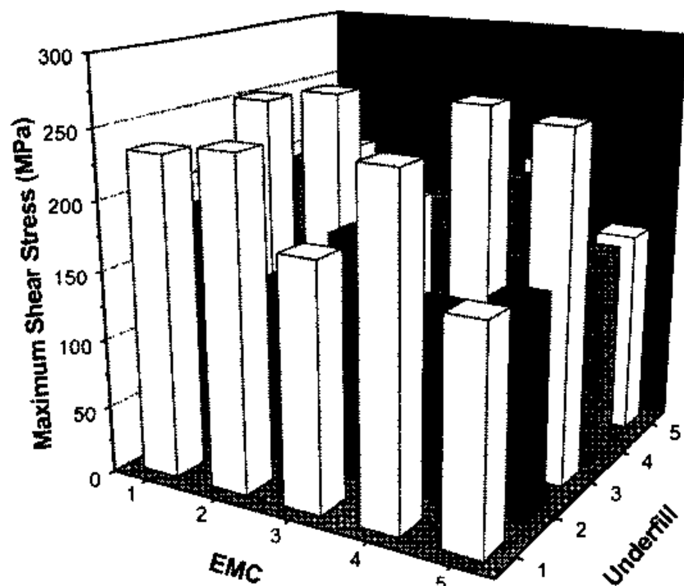

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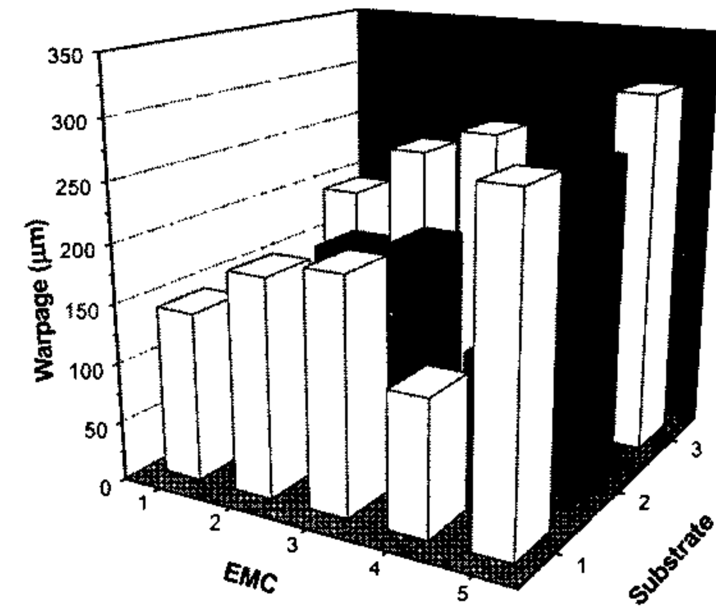
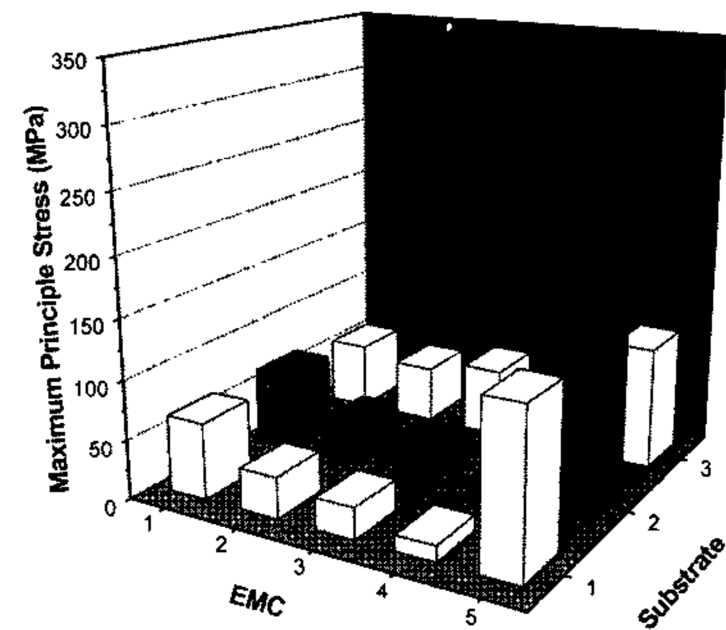
Fig. 10. The relationship between the maximum shear stress of the substrate and underfill-EMC with 3 substrates (1), (2) and (3)



(a)



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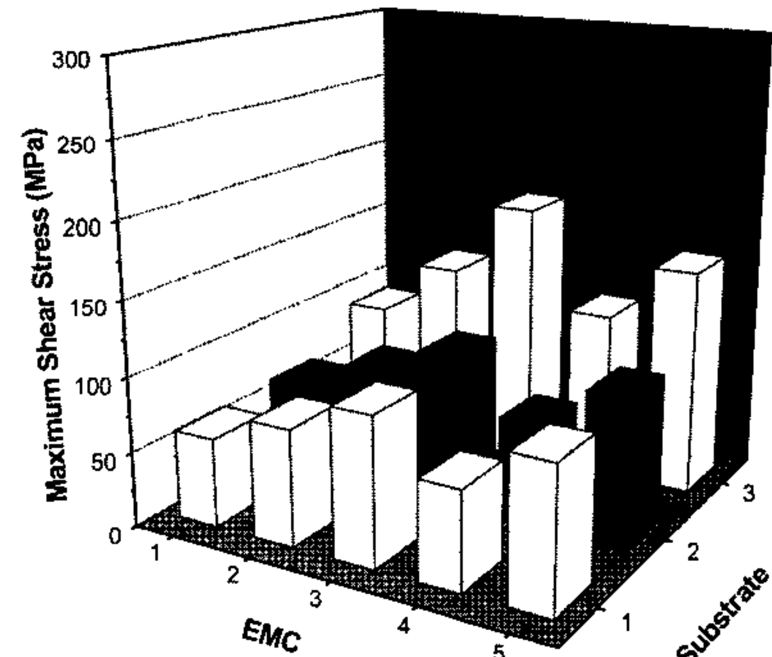

(c)

Fig. 11. Behavior comparison between package with or without underfill: (a) Warpage (b) MPS and (c) MSS

smaller than those of other underfills. It can be also seen that EMC No.3 achieves smaller MSS than the other EMC materials.

Conventionally according to the material candidates listed in Tab. 2, there are altogether 75 material sets of samples needed to be prepared, tested and compared in order to choose the bill of materials (BOM). However, with the help of design study, on considering the warpage of the package, MPS of the die and MSS on the substrate the best material combination for the current package development is underfill No.2 (or No.5), EMC No.4 and substrate No.2. Therefore, the number of testing samples has been reduced to only 2, which saves lot of time as well as cost in the development of the package.

3.4. Molded Underfill Process

Process improvement is also considered in this

study. In the current development of SiP a new manufacturing process, MUF is proposed to be used to compare with the conventional underfill process.

EMCs have been widely used for encapsulation in packaging for a long time. However, since underfilling and molding process all needs long curing time separately, the idea to combine molding and underfilling processes together into one step results in the molded underfill. MUF is applied to a flip chip in package via transfer molding process, during which the molding compound not only fills the gap between the chip and the substrate but also encapsulates the whole package. This process is an extension of the traditional EMC molding process using conventional molding technology. It is also a lower cost solution since it could be possible to use the existing molding equipment. Compared with the conventional underfill which is usually filled with silica at around 50 wt%, molded underfill can afford a much higher filler content, up to 80 wt%, which offers a low CTE close to that of the solder joint and PCB. Also, compared with the conventional molding compound, MUF requires fillers in smaller size, which also contributes to decrease CTE of the material. Higher Tg and lower CTE of EMC leads to low warpage and stresses in the package. Therefore, it provides better reliability. Furthermore, MUF is able to improve the production efficiency for flip chip packaging manufacturing because it is a more automated, simpler, more robust and faster process. It was reported that a four-times production rate increase can be expected using MUF compared with the conventional underfill process[22-27].

Fig. 11 shows the relationship between (a) warpage of the package, (b) maximum principle stress of the die and (c) maximum shear stress on the substrate and EMC-substrate materials. Compared with the underfilled package shown in Fig. 8-10, MUF package has the performance of both lower warpage and lower stresses. With the combination of EMC No.4 and substrate No.1, the MPS in the die is only 20MPa which is almost a neglectable value. The same material set also achieves the lowest MSS, the value of which is only 63MPa. There is no obvious difference in warpage variation between MUF and conventional underfill. This may be due to the smaller volume of underfill compared with EMC. Therefore, its contribution to warpage control is not significant.

4. Reliability Evaluation

In a SiP module, there are multiple dies and passives while substrate structure is relatively more complicated. The overall yield of a SiP is determined by the yield of each die and the substrate. Hence, both Known Good Die (KGD) and substrate are critical to the reliability performance of package[28,29]. In this paper, JEDEC's moisture sensitivity level (MSL) test, pressure cooker test (PCT) and temperature cycle (TC) test are performed for reliability evaluation of SiP.

4.1. Daisy Chain Test Vehicle Design

Test vehicle must be designed to capture all of the thermo-mechanical failures attributed to accelerated reliability tests. To this endeavor, daisy chain design is used. The daisy chain test vehicle is designed to be used for second level interconnect assembly test and continuity verification. Fig. 12 shows the daisy chain test vehicle for the current reliability test of SiP module. Both power management die and

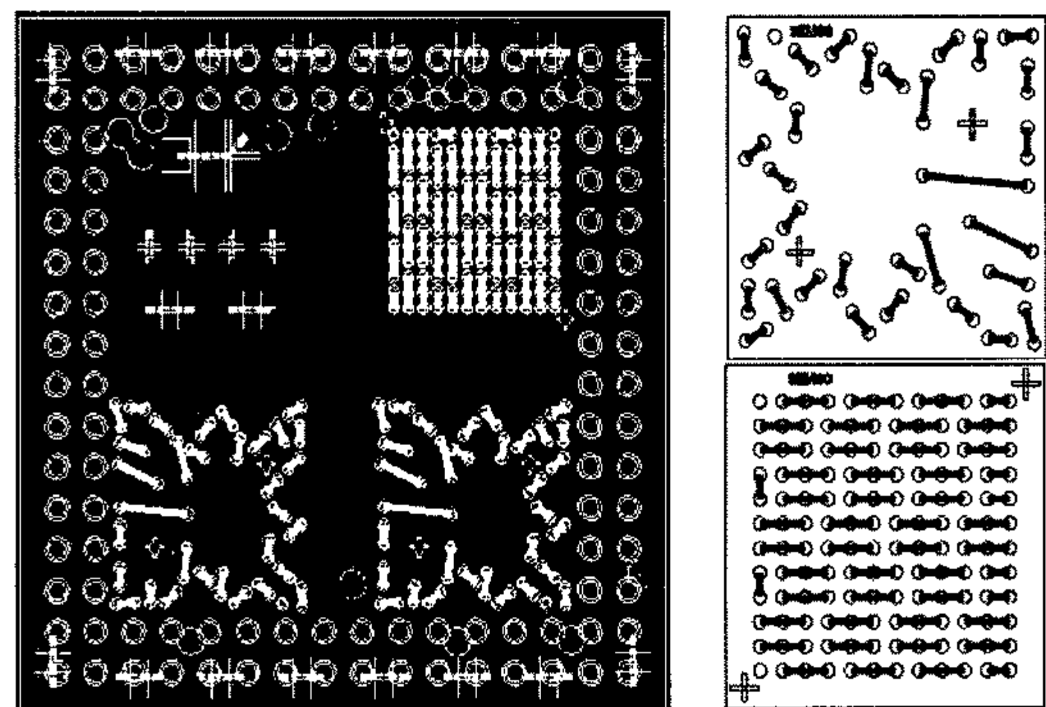

Fig. 12. Daisy chain test vehicle design in the current reliability test

Table 3. Moisture Sensitivity Level (MSL), PCT and TC Reliability test results

Leg	U/F	EMC	Preconditioning Test (MSL)				Reliability test			
			L2		L3		PCT (168hrs)		TC (1000cycles)	
			Elec O/S	Delam	Elec O/S	Delam	Elec.O/S	Delam	Elec.O/S	Delam
1	Sumitomo	Sumitomo	0 / 22	12 / 22	0 / 44	0 / 44	0 / 22	19 / 22	0 / 22	0 / 5
2	Nagase	Sumitomo	0 / 22	19 / 22	0 / 44	0 / 44	0 / 22	22 / 22	0 / 22	0 / 5
3	MUF	Sumitomo	1 / 22	17 / 22	0 / 44	0 / 44	0 / 22	17 / 22	0 / 22	0 / 5
4	MUF	Matsushita	0 / 22	22 / 22	0 / 44	0 / 44	0 / 22	22 / 22	0 / 22	0 / 5

BB+RF die have 65 I/Os and the memory die has 144 I/Os. For the board level interconnection, there are 112 solder balls peripherally distributed (shown in Fig. 12).

4.2. Reliability Test

A series of JEDEC tests have been performed on the SiP module. These tests are designed to accelerate failure in devices, uncovering any design flaws or drawbacks inside the package, the results of which can be used to improve the packages and minimize field failures. The information is useful to help designers establish guidelines for handling, soldering, classifying, and storing the package.

Preconditioning tests are firstly carried out. The moisture sensitivity level (MSL) tests determine the length of time a device can be exposed to humidity. These classification levels are useful in determining the proper storage and handling of the package to prevent thermal and mechanical damage during solder reflow or repair. MSL evaluation under JEDEC MSL3 (60C/60%RH, 40 hours) and MSL 2a ((60C/60%RH, 120 hours) followed by reflow at 245°C are performed. Before the MSL tests, the package needs to be baked out at 125°C for 24 hours.

Pressure cooker tests (PCT) are also carried out. PCT uses a temperature humidity combined environment to accelerate failure caused by metallization corrosion. It is a reliability test performed to assess the ability of the package to withstand severe temperature and humidity conditions. In this study, PCT test conditions are 121°C and 2 atm with no electric bias for 168 hours.

Temperature cycling (TC) tests are performed to determine the electric resistance of package to high and low temperature extremes. This test is designed to simulate the extensive changes in temperature to which the packages may be exposed. Test condition is -55~125°C temperature range with the testing frequency at 1cycle/hour. During the test, daisy chain signals for the package are in-situ monitored. In the most of mobile application, minimum requirement for temperature cycling test is 500 cycles. In this study, 1000 cycles standard is applied to assure the quality of the package.

After these reliability tests, delamination situation inside the package is also checked through scanning acoustic tomography (SAT) and cross-section optical microscopy (OP) or scanning electron microscope (SEM) observation. All the reliability test results and failure analysis are summarized in table 3.

As shown in Table 3, in general the current developed SiP module shows good reliability performance. No electrical open short failure has been found out during all reliability tests except for one case in MSL 2a. The package using Sumitomo EMC shows better reliability than that of Matsushita EMC. It can be also seen that replacing the underfill with UMF could not only save a process, but also improve the reliability performance.

By analyzing the electric open short failure sample, non-wetting electric open is observed which is due to the failure of PCB solder resister development and no flux deposition on the Under Bump

Metal (UBM) during SMT processes. The SiP module could meet JEDEC MSL level 3 requirements for moisture sensitivity. However, serious delamination has been observed after MSL 2a and PCT tests. The delamination occurs at die-underfill, die-EMC, solder-PCB, die-passivation layer, and PCB-SR interfaces. Part of the reason to cause delamination is because the adhesion strength between PCB and underfill-EMC is not enough. During reliability test, the shear stress caused by thermal mismatch of the packaging materials may exceed the shear strength of the interface which leads to the delamination. In addition, voids inside underfill and EMC are observed during underfilling and molding processes, especially in the areas around the solder bumps under the die. These voids will be propagated when the package is subjected to reliability tests at higher temperature. Under the temperature which is much higher than boiling point of water, the humidity trapped inside the underfill or EMC void during manufacturing process or diffused and absorbed during MSL and PCT tests will be changed to vapour, the volume of which is expected to expand significantly. Fig. 13 shows the SAT results on the comparison of the void situation inside the package between level 2a and level 3 MSL reliability tests. The image after L2a tests shows larger voids than that of L3. The pressure caused by the vapor expansion may lead to internal delamination, internal micro-cracks, bond damage, solder lifting, or in some extreme cases, a macro-crack, also known as the "popcorn" effect. Therefore, notable delamination is observed after MSL 2a and PCT test while there is no delamination failure for MSL3 and TC tests.

There are lots of reasons which contribute to underfill void formation during underfill or molding processes. Among them the main factors are, dimension effects such as die size, bump pitch, stand off height of the chip, and substrate design, etc, and physical effects such as material properties, surface tension, and wettability of substrate solder mask, die passivation layer, and the surface tension of bumps on the die and substrate. A comprehensive design of experiment (DOE) investigation needs to be performed to find out the effects of these factors on the reliability of the package, which is however not covered in this study.

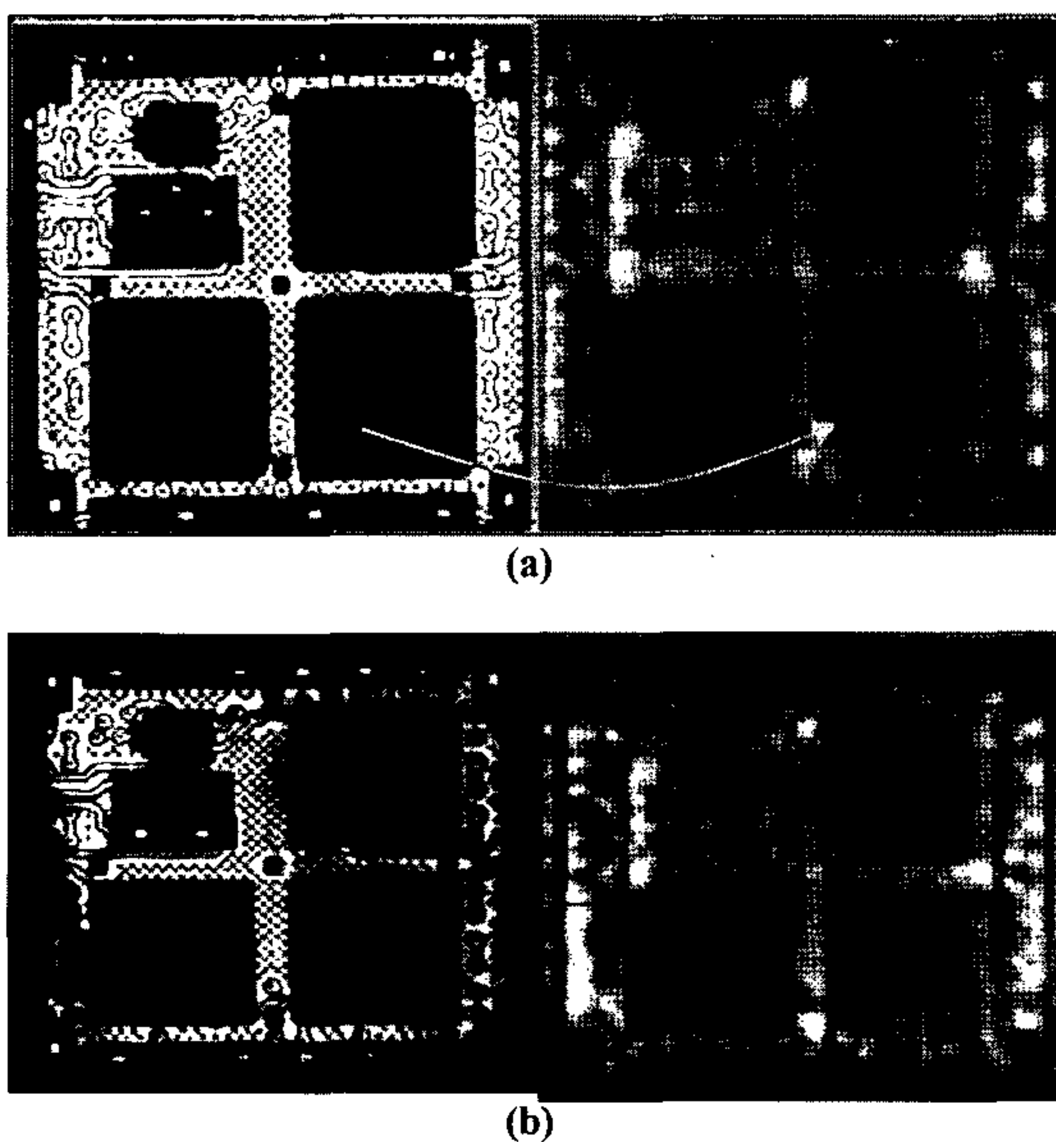

Fig. 13. Comparison of C-SAM image after reliability test: (a) MSL3 test result (b) MSL2a test result

5. Discussion

In this paper, the development of ultra-slim SiP module is reported. The availability of fully tested dies is crucial for the package yield. A single bad die in the package may have a significant impact on the overall cost. The memory and RF parts can be easily combined based on the system design with lower cost. However, the integration of the complex system and the reduction in system volume come at the expenses of difficulty in heat dissipation. Therefore, this package design needs better thermal design approach to tackle the multiple heat sources in the SiP module. Since the heat created by the dies is mainly conducted through the solder bumps, the smaller the bump size and number, the higher the thermal resistance of the package.

6. Conclusion

It is well known that reliability of plastic package on polymeric PCB is better than that of ceramic counterpart. This phenomenon is confirmed through this investigation. Thermal stress and warpage arise in the SiP module when cooling to room temperature after reflow process due to the CTE mismatch between the components of the package. The mechanical simulation on the SiP helps to reduce the testing sample from 75 to 2. The material set with underfill candidate No.2, substrate candidate No.2 and EMC candidate No.5 achieves the smallest warpage and stress of the package and therefore have the best reliability performance. Reliability tests validate the simulation results. SiP module with the proposed material set can pass MSL level3 and TC tests. Although delamination is observed after MSL L2a and PCT tests, no delamination has been found after MSL3 test and no electronic open short occurs during all reliability tests. Furthermore, the proposed process improvement, which uses MUF to replace the conventional underfill, shows more robust reliability behavior.

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