

A Novel Push-Pull Type Charge Pump Based on Voltage Doubler for LCD Drivers

Sung Wook Choi and Kae Dal Kwack

Abstract

A novel push-pull voltage converter structure, using a switched capacitor type voltage doubler, is proposed. The circuit is constructed with a two-stage push-pull voltage doubler that has a stable operation with small output ripple. The two-stage voltage doubler creates the output voltage $4V_{dd}$. The high clock signal is cross-coupled to the input of the second stage with the opposite phase to reduce two switching transistors and capacitors. Simulation results verify that even with a reduced number of transistor and capacitor, there is no circuit performance loss. Adding one capacitor and two switching transistors the circuit can be changed to eight times of V_{dd} maker.

Keywords : push-pull, voltage doubler, switched capacitor, small ripple

1. Introduction

The charge pump DC-DC converter, representative of power supply equipment in an integrated circuit, started with Dickson's charge pump[1]. It has been developed in various applications. The voltage booster using inductors has high power conversion efficiency. Its disadvantages are faulty operation in nearby circuits caused by magnetic elements, volume and weight problems. The charge pump voltage converter is suitable for circuit areas that need a thin composition and light-weight, such as memory and mobile equipment. In particular, switched capacitor (SC) type DC-DC converter is an appropriate circuit, due to its simple structure and high voltage conversion efficiency[2][3].

2. Switched capacitor voltage doubler

With the trend on low-power, low-voltage circuit design, the switched capacitor voltage converters have become mandatory in power management ICs for battery powered portable applications. They have many advantages over inductor-based switch mode power supplies. Fig. 1

shows the most popular SC type voltage converter, voltage doubler, and its operation. The SC type voltage doubler has four switching transistors and two capacitors : a flying capacitor and a load capacitor [2]. This voltage doubler typically has two operational phases. First, in phase 1, switches S1 and S4 are closed and S2 and S3 are open. In this phase, the capacitor C1 is charged by V_{dd} . At the same time, C_{out} is discharged through the output load. In phase 2, S1 and S4 are open and S2 and S3 are closed. In this phase, the voltage on C1 is discharged through C_{out} and the load, compensating the energy lost in C_{out} during the first phase. That is, the two capacitors C1 and C_{out} share charges during the second phase, where the amount of charge lost from C1 is transferred to C_{out} . The final voltage V_{out} across C_{out} can be calculated using the following relation, where V_{out_prev} is the voltage across C_{out} from the previous state.

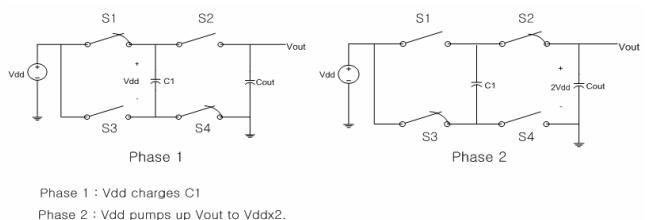


Fig. 1. Typical SC voltage doubler and its operation.

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Corresponding Author : Sung Wook Choi
Division of Electrical and Computer Engineering, Hanyang University,
Hangdang-dong, Sungdong-gu, Seoul 133-791, Korea
E-mail : deadbird@hanyang.ac.kr
Tel : 81-02-2220-0357 **Fax** : 81-02-2291-6399

$$V_{out} = V_{out_prev} + \left(\frac{C_1}{C_1 + C_{out}} \right) (V_{dd} + V_{C1} - V_{out_prev}) \quad [2]$$

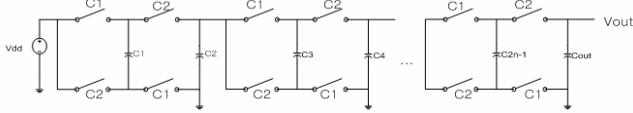


Fig. 2. Simply cascaded voltage doublers.

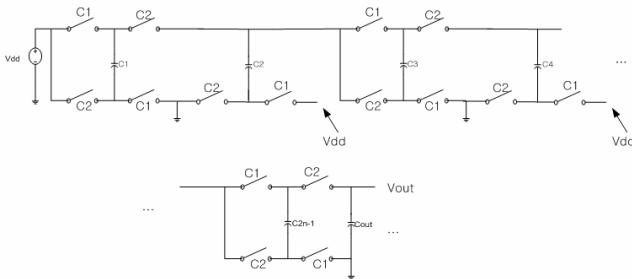


Fig. 3. Input added voltage doubler (IAVD).

To achieve a higher voltage gain, the voltage doubler can be cascaded, as shown Fig. 2. The output voltage of the previous stage becomes the power supply of the next stage. In this case, the ideal voltage gain of the n-states voltage doubler is 2^n . Another effective cascade circuit is Fig. 3. The circuit is almost the same as in Fig. 2, but Vdd is added to the next stage power supply. This n-stages IAVD (Input Added Voltage Doubler) has $(3 \times 2^{n-1}-1)$ times voltage gain (2, 5, 11, 23, ...) [3][4][5].

3. Proposed circuit

Voltage loss and output ripple can be a serious problem in the voltage converter design. Eliminating or reducing these are important issues. The “push-pull” circuit [2] is an effective technique to minimize voltage loss and the output voltage ripple. The “Push-pull” circuit consists of two charge pumps working in parallel and in opposite phases to deliver a charge to support the output voltage. Fig. 4 shows the structure of the push-pull voltage doubler and its operation. In this architecture, one of the pump capacitors is always delivering charge to the output. As a result, the output ripple frequency is at twice the switching frequency. The push-pull circuit is effective, but is critically handicapped requiring so many switching transistors and capacitors. A

new type 4x charge pump is proposed to solve this problem (Fig. 5-(b)). The proposed circuit is based on typical SC voltage doubler. For structural and operational efficiency, it is designed as a 4x charge pump that has the output voltage four times that of Vdd. The second stage capacitor of this circuit is connected to the other phase high clock as a cross-coupled structure. This results in the circuit saving two capacitors and switching transistors, compared to the conventional circuit [5]. Comparison of the structural characteristics with the conventional circuit and IAVD is shown in Table 1[6].

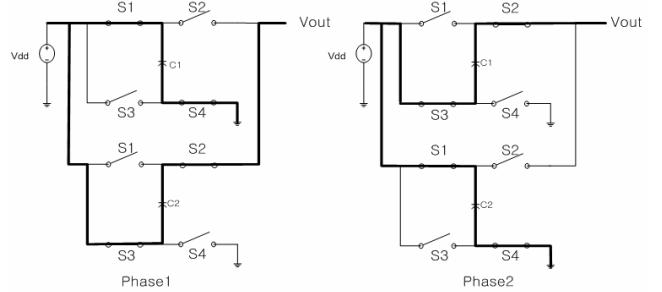
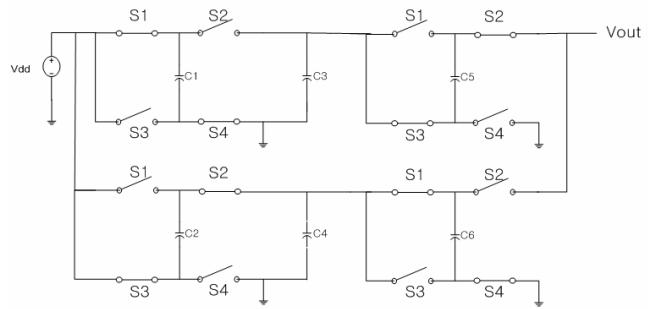
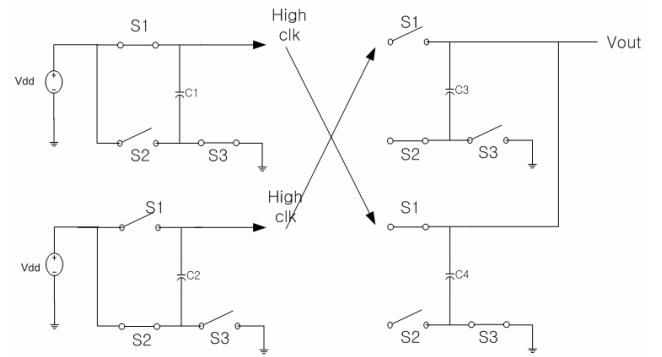


Fig. 4. Push-pull voltage doubler.



(a) Conventional type



(b) Proposed type

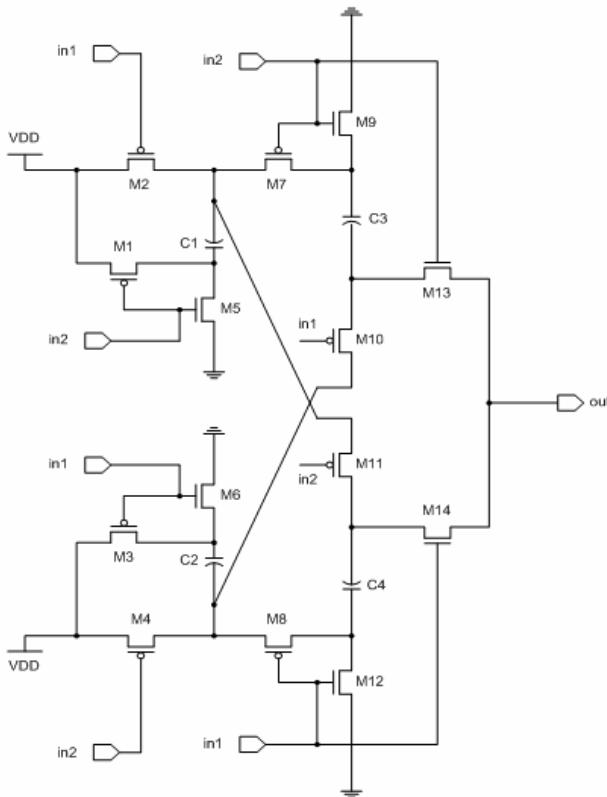
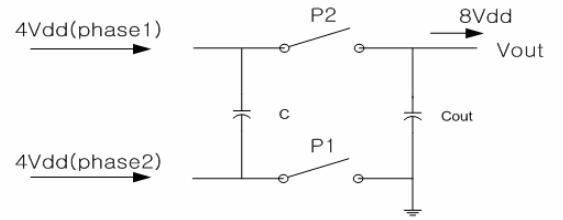
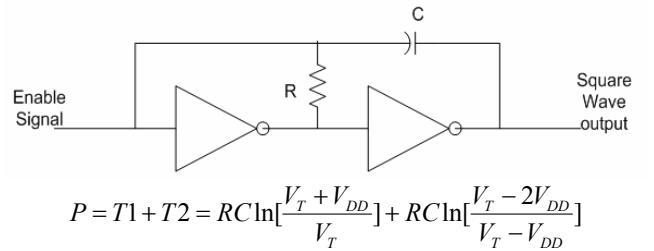
Fig. 5. Push-pull 4x charge pump.

Table 1. Structural characteristics.

	Output Voltage	Switching Tr.	Cap.	Output Ripple
Conventional 4x push-pull	4Vdd	16	6	Good
2 stage IAVD	5Vdd	10	3	Bad
Proposed type	4Vdd	14	4	Good

4. Circuit design

Fig. 6 shows the proposed voltage converter circuit. It consists of 14 switching transistors and 4 flying capacitors. The ideal output voltage is 4Vdd; some modifications can make the output voltage 8Vdd. If two transistors and one capacitor are added to the output stage (Fig. 7), the output voltage can be 8Vdd. If the output stage is designed as an externally controlled circuit, this charge pump circuit is applicable to an 8 times voltage converter, as well as to a push-pull 4x charge pump.

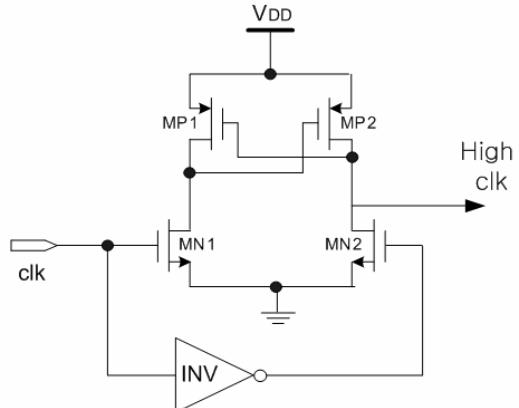
**Fig. 6.** Proposed voltage converter circuit.**Fig. 7.** The output stage modified to 8Vdd maker.

$$P = T1 + T2 = RC \ln\left[\frac{V_T + V_{DD}}{V_T}\right] + RC \ln\left[\frac{V_T - 2V_{DD}}{V_T - V_{DD}}\right]$$

P : Period T1 : High output time T2 : Low output time

V_T : Threshold voltage of the inverter

Typical value of P : 2.2RC or 2.5RC

Fig. 8. RC type oscillator.**Fig. 9.** High voltage level shifter.

The high clock made by C1 passes through the M11 to charge C4 to 2Vdd during the first phase (Fig.6). At the same time, C1 also pushes C3, which has been charged to 2Vdd during previous (second) phase by C2 to 4Vdd. Consequently, the output supply voltage always becomes 4Vdd. Fig. 8 shows the oscillator. The oscillation circuit is a simple RC type, and the oscillation frequency is set to 10kHz. The high clock that can drive the switching transistors is obtained from the output using a high voltage level shifter (Fig. 9). Finally, the output signal of the level shifter should pass through the buffer circuits to drive the large switching transistors.

5. Simulation and results

All simulation results were achieved with a high voltage CMOS process, under the conditions where Vdd was 2.5V and clock frequency was set to 10kHz. First, Fig. 10 shows transient characteristic of proposed circuit and Fig. 11 shows the simulation result, when the circuit is modified to 8Vdd maker. Fig. 12 shows the comparison of three types of DC-DC converter with 1k Ω output load. In these simulations, the transistor sizes of three types of circuits are the same. IAVD and non push-pull type have serious problems in ripple and output voltage dropping to drive the load current (Fig. 12). Fig. 13 is a graph of various characteristics according to the output load resistance variation. Over the total range, the proposed circuit has a relatively steady and stable performance.

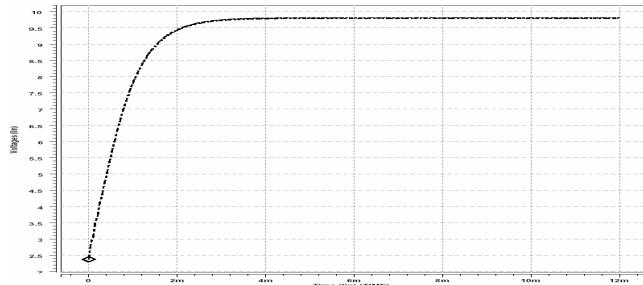


Fig. 10. Transient characteristic.

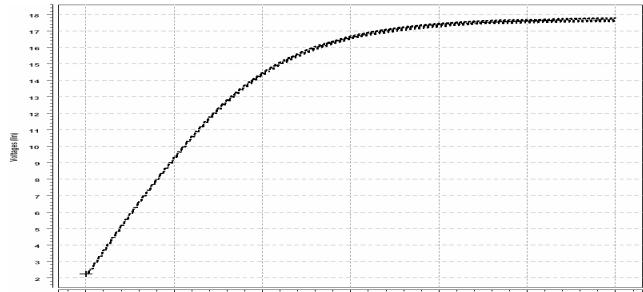


Fig. 11. When modified to Vout=8Vdd circuit.

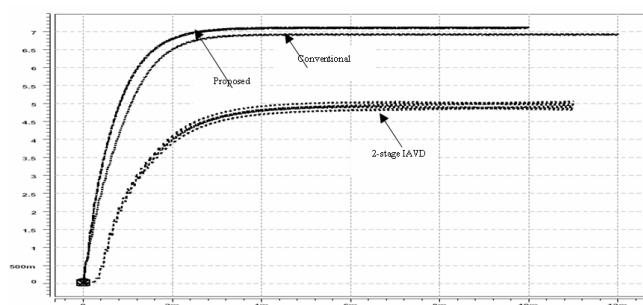
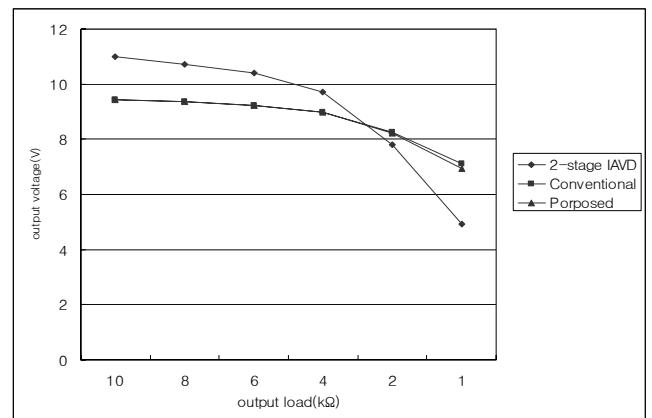
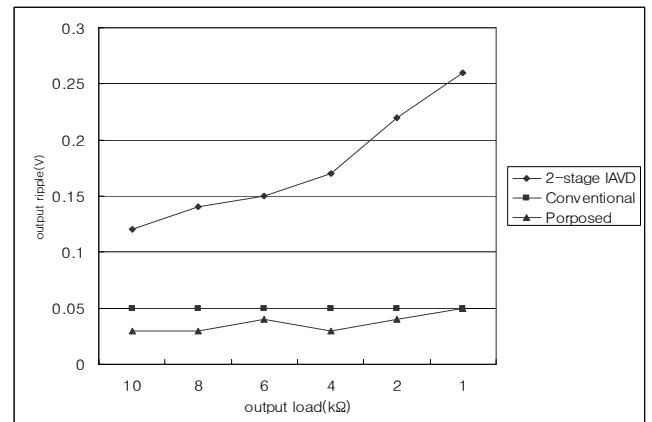


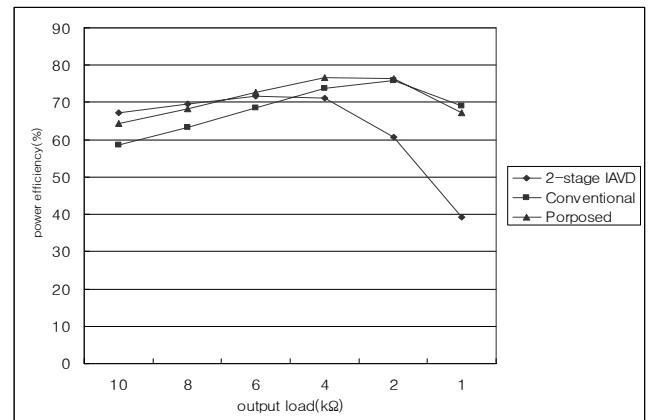
Fig. 12. Output characteristics of 3 type circuits ($R_L=1k\Omega$).



(a) Output voltages



(b) Output ripples



(c) Power efficiency

Fig. 13. Various output characteristics.

6. Conclusion

In this paper, a new type of push-pull voltage converter, based on a voltage doubler for LCD drivers, was proposed. The circuit produces as output four times Vdd. Although the proposed circuit could save two switching transistors and capacitors, the performance would not degenerate, but it would be improved somewhat. The proposed circuit was verified with simulations, using a high voltage CMOS process. This was compared to other conventional type DC-DC converters. The proposed circuit could be simply modified to a DC-DC converter with output voltage 8Vdd.

References

- [1] J.K. Dickson, IEEE J. Solid-State Circuits. **SC-11**, 374 (1976).
- [2] Mentor Graphics Corp. <http://www.mentor.com>
- [3] Starzyk, J.A , Ying-Wei Jan and Fengjing Qiu, Fundamental Theory and Applications, IEEE transactions on. **48**, 350(2001).
- [4] T. Tanzawa and T. Tanaka, T.IEEE. Solid-State Circuits **32**, 1237(1997)
- [5] M. Makowski and D. Maksimovic IEEE PESC, 1215 (1995).
- [6] Kei Eguchi, Toru Tabata, Fumio Ueno, Hongbing Zhu and Takahiro Inoue, IEEJ Trans. EIS. **125**, 37 (2005).