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Electrical Analysis of Bottom Gate TFT with Novel Process Architecture

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Abstract

Bottom gate thin film transistors (TFTs) with microcrystalline and amorphous Si (a-Si) double active layers (DAL) were fabricated. Since the process of DAL TFTs can use that of conventional a-Si TFTs, these DAL TFT process has advantages, such as low cost, large substrate, and mass production capacity. In order to analyze the degradation characteristics in saturation region for driving TFTs of active matrix organic light emitting diode, three different dynamic stresses were applied to DAL TFTs and a-Si TFTs. The threshold voltage shift of DAL TFTs and a-Si TFTs during 10,000 second stress is 0.3V and 2V, respectively. DAL TFTs were more reliable than a-Si TFTs.

Keywords : Dynamic stress, a-Si TFT, Double active layer TFT (DAL TFT), Degradation, State creation

1. Introduction

The active matrix organic light emitting diode (AMOLED) has been widely analyzed. The AMOLED displays have a variety of advantages such as a wide viewing angle, a large color gamut, a fast response time, and low power consumption [1]. Because these displays are current-driven, the backplane TFT should have highly stable electrical performances. Amorphous Si (a-Si) TFTs have been intensively studied for AMOLED applications since the ease and high throughput of the deposition process make them easy to mass produce [1, 2]. However, a-Si TFTs with both low mobility and instability are difficult to apply AMOLED applications [3, 4]. Although polycrystalline Si (poly-Si) based TFTs offer a high-field effective mobility, they have non-uniformity characteristic and their production process is problematic [5]. This paper demonstrates the use of microcrystalline Si (μc-Si) TFTs to avoid these drawbacks [6]. Although μc-Si has a low deposition rate, μc-Si TFTs have a high-field effective mobility and show good stability under DC bias stresses [7].

We investigated the reliability of a-Si/μc-Si double active layers (DAL) in the bottom gate TFT. We specifically focus on the degradation characteristics of both DL TFTs and a-Si TFTs under dynamic electric stresses.

2. Experiments

We propose a bottom gate TFT with a-Si/μc-Si DAL as an active layer. Fig. 1 shows the schematic cross section of a typical DAL TFT. The μc-Si layer was deposited in a 13.56 MHz capacitively coupled RF plasma enhanced chemical vapor deposition (PECVD) chamber. First, a 4000 Å-thick Mo layer was deposited by sputtering, and then the bottom gate was patterned. Four layers consisting of SiN_x (4000 Å), a-Si (1000 Å), μc-Si (1000 Å), and n^+ a-Si (1000 Å) were deposited by PECVD. The a-Si/μc-Si DAL was deposited with mixtures of SiH_4/H_2/inert gas to form the a-Si

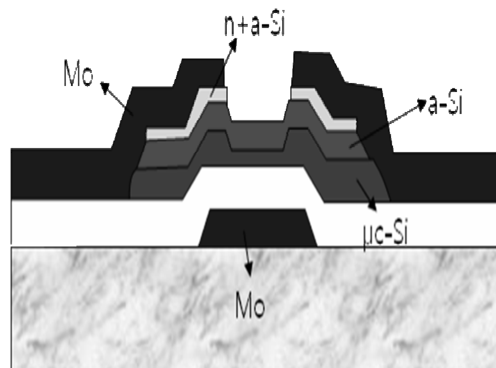

Fig. 1. Schematic cross section of the DAL TFT.

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layer, and SiF_4/H_2 to form the μc-Si layer. The deposition temperature of a-Si and μc-Si is 275°C and 350°C, respectively. After defining the active channel region, a 4000Å-thick Mo layer was deposited by sputtering, and then the source/drain electrode was patterned. Finally, a 2000 Å-thick passivation layer of SiN_x was deposited.

DAL TFTs can be directly applied to the TFT fabrication process for commercial active matrix liquid crystal (AMLCD) without additional process steps or equipment because the fabrication process of DAL TFTs is similar to that of conventional a-Si TFTs. DAL TFTs could be a cost effective way to produce AMOLEDs backplane.

Fig. 2 shows the plane image of the DAL TFT (W/L = 50 μm/8 μm) and its channel area using an optical microscope.

3. Results and discussion

Typical drain current- gate voltage (I_{ds}-V_{gs}) transfer characteristic of the DAL TFTs with W/L = 50 μm/8 μm at V_{ds} = 5.1 V is shown in Fig. 3. The following properties have been measured; a field effect mobility of ~0.44 cm^2/Vs, a threshold voltage of 5V, a subthreshold slope of 1.2V/dec, and on-off ratio of 10^6.

Fig. 2. The plane image of (a) the DAL TFT (W/L = 50μm/8μm) by optical microscope and (b) the channel layer schematic.

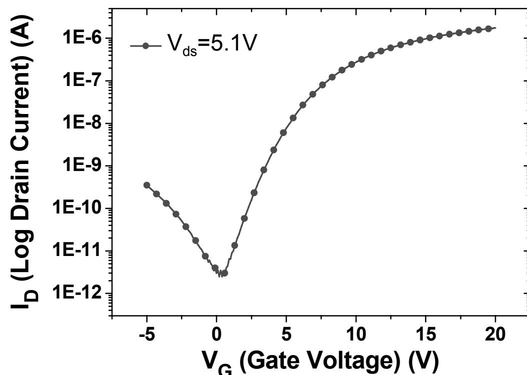

Fig. 3. Typical transfer characteristic of the DAL TFT at V_{ds} = 5.1V (W/L = 50μm/8μm).

Dynamic stresses are more similar to real operating conditions than static stresses [8]. To compare and analyze the reliability of DAL TFTs and a-Si TFTs, dynamic electrical stresses were applied to both transistor types. The dynamic stress conditions are listed in Table 1.

Fig. 4 shows the transfer characteristics of the (a) DAL TFT and (b) a-Si TFT measured at V_{ds} = 5.1 V under dynamic stress condition 1 in table 1. During real operation of the switching TFT in an AMOLED, TFTs are operated at a low frequency (~ 60Hz) and a very low duty ratio (<< 1%). To accelerate degradation, we adopted severe stress conditions with high frequency. After both TFTs were applied to dynamic stresses, DAL TFTs showed little threshold voltage (V_{th}) shift degradation, while the a-Si TFTs suffered a significant positive V_{th} shift. The degradation mechanisms of the a-Si TFT can explain charge trapping in the SiN_x gate insulator, and state creation in the band gap of the a-Si layer [9]. State creation is dominant at low gate bias and charge trapping is dominant at high gate bias. In these experiments of low gate dynamic stress, the transfer characteristics of a-Si TFT are affected to be a considerable positive shift due to state creation. Otherwise, the DAL TFT is not affected the state creation because of μc-Si and a-Si double active layer.

Fig. 5 shows the log-log plot of V_{th} shift versus stress time of a-Si TFTs and DAL TFTs under dynamic stress condition 1 in table 1. This result indicates that log V_{th} shift is linear as a function of stress time. In other words, it shows the power-law time dependence. Otherwise, charge trapping is linear on V_{th} shift, not log. It means that state creation process explains power-law time dependence at low voltage and charge trapping explains logarithmic time dependence at high voltage [10]. Therefore, degradation of a-Si TFTs and DAL TFTs is state creation at our experimental conditions.

Table 1. Dynamic electrical stress conditions.

Conditions	V_{gs} (V)	V_{ds} (V)	Frequency (Hz)	Time (sec)	Duty ratio (%)
1	0/10	10	60K	0, 10, 50, 100, 500, 1000	50
2	0/10	10	60, 600, 6K, 60K	10,000	50
3	0/10	10	60K	10,000	10, 50, 90

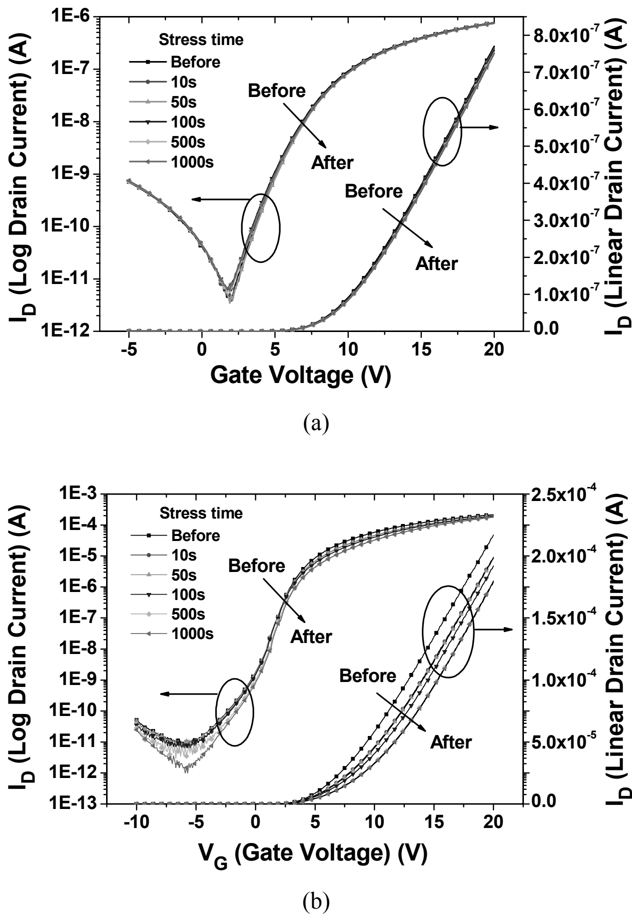

Fig. 4. Transfer characteristics of (a) DAL TFT and (b) a-Si TFT measured at V_{ds} = 5.1 V under dynamic stress condition 1.

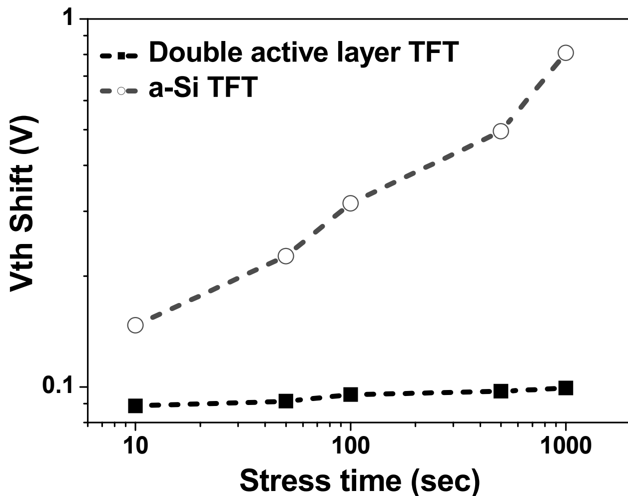

Fig. 5. The log-log plot of V_{th} shift versus stress time of a-Si TFTs and DAL TFTs measured at V_{ds} = 5.1 V under dynamic stress condition 1 in table 1.

Fig. 6 shows the V_{th} shift and mobility variation comparison of the a-Si and the DAL TFT measured at V_{ds} = 5.1 V under dynamic stress condition 2 in table 1. In the a-Si TFT, the V_{th} shift depended on the increase of frequency. However, the DAL TFT showed no variation in V_{th} shift as a function of frequency. In high frequency, gate bias dynamic stresses applied a-Si TFT and DAL TFT generate a larger amount of transition from 0 V to 10 V. It suggests that V_{th} shift increased with transition increment in a-Si TFTs, but DAL TFTs are highly stable in spite of large gate bias transition.

Fig. 7 shows the V_{th} shift and mobility variation plotted against the duty ratio for the two types of transistor under stress condition 3 in table 1, measured at 5.1 V. Fig. 6 and 7 were experimented by five DAL and a-Si TFTs. Although the duty ratio increased, the V_{th} shift was nearly changeless in both the DAL TFTs and the a-Si TFTs. This

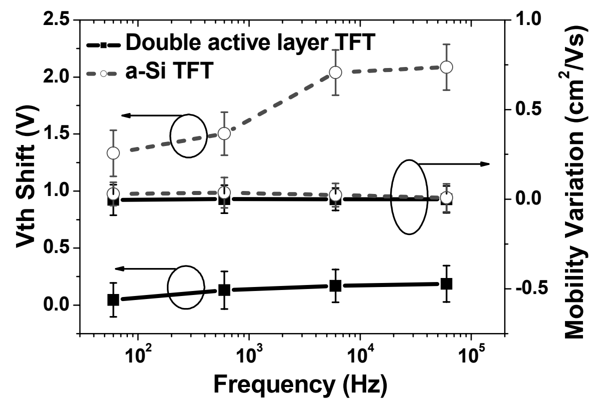

Fig. 6. The V_{th} shift and mobility variation comparison as a function of frequency of DAL TFT and a-Si TFT measured at V_{ds} = 5.1 V under dynamic stress condition 2.

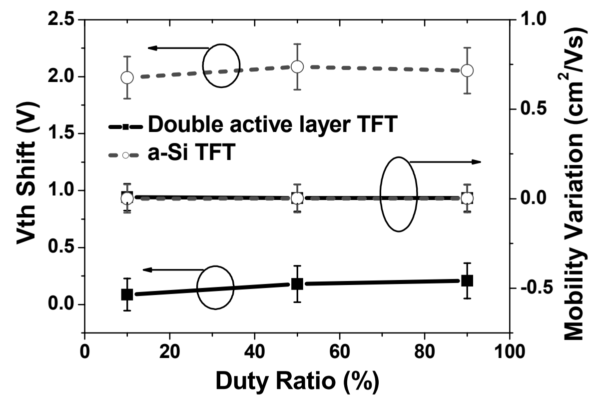

Fig. 7. The V_{th} shift and mobility variation comparison as a function of duty ratio of DAL TFT and a-Si TFT measured at V_{ds} = 5.1 V under dynamic stress condition 3.

result indicates that for an a-Si TFT, a pulsed transition is a greater factor in the transistor's degradation than a dynamic stress applied accumulation time. Although the V_{th} shift in both the DAL TFT and the a-Si TFT was independent on duty ratio, the DAL TFT showed a smaller V_{th} shift of approximately 0.3 V, while the a-Si TFT showed a V_{th} shift of approximately 2 V, as seen in Fig. 6 and 7. Fig. 6 and 7 show that the mobility variation was not affected by dynamic stresses. These results demonstrate that the DAL TFTs are more reliable than the a-Si TFTs under dynamic stresses.

4. Conclusions

DAL TFTs were fabricated and studied for improved stability and production efficiency. These transistors were used with a conventional bottom gate a-Si TFT process. In order to confirm the reliability of the device, dynamic electric stresses were applied to both a DAL TFT and an a-Si TFT. The mobility variations of both transistors under dynamic stresses were negligible. However, a large positive V_{th} shift was shown in the a-Si TFT with the increase of the high frequency. These results indicate that the degradation of the a-Si TFT is caused by state creation in the a-Si active layer. DAL TFT was observed in no V_{th} shift. Because the channel layers of the DAL TFT are made up of double active layers of a-Si and μs-Si, we can conclude that the DAL TFT isn't affected by state creation in the channel layers.

For the a-Si TFT, increasing the frequency produced an increased V_{th} shift, while increasing the duty ratio produced no V_{th} shift variance. From these results, we can demonstrate that the V_{gs} transition from 0 V to 10 V generates more state creation than V_{gs} accumulation stresses time. The V_{th} shift in the DAL TFT was independent of both frequency and duty ratio. In other words, the DAL TFT was reliable under dynamic stress and, therefore, is suitable for AMOLED applications.

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