A MB-OFDM UWB 0.18-μm CMOS RF Front-End Receiver

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Abstract

An RF front-end dual-conversion receiver for 3~5 GHz MB-OFDM UWB systems is implemented in 0.18 μm CMOS technology. The receiver includes a two-stage UWB LNA, an RF mixer, an IF *I/Q* mixer, and a frequency synthesizer. The proposed receiver adopts the dual-conversion architecture to mitigate the burden of design of the frequency synthesizer. Accordingly, the proposed frequency synthesizer generates four LO tones from only one VCO. The receiver front-end achieves power gain of 16.3 to 21 dB, NF of 7 to 7.6 dB over 3~5 GHz, and IIP3 of −21 dBm, while consuming 190 mW from a 1.8 V supply.

Key words : Ultra-Wideband, UWB, CMOS, Low Noise Amplifier, Mixer.

Ⅰ. Introduction

The ultra-wideband(UWB) system has emerged as a major technology for high data rate services in wireless communication systems. The allocated unlicensed UWB frequency range is 3.1~10.6 GHz and the maximum output power level is limited to 41.3 dBm/MHz by the Federal Communications Commission(FCC)[1]. Currently, two UWB system approaches for the Wireless Personal Area Network(WPAN) exist in IEEE 802.15.3a: MB-OFDM(Multi-Band Orthogonal Frequency Division Multiplexing) and DS-CDMA(Direct-Sequence Code Division Multiple Access)[2].

The MB-OFDM approach has inherent robustness against narrow-band interferers and multi-path environments. In addition, the MB-OFDM approach divides the full UWB band into fourteen sub-bands with bandwidth of 528 MHz. The fourteen sub-bands are divided into five groups of frequency bands[2]. In this way, the MB-OFDM approach can use its frequency bands more flexibly and efficiently in aspect of data-rate capability, co-existence with other wireless systems, frequency regulations in each country, and so on. However, in the MB-OFDM system, each sub-band is hopped within 9.5 nsec to define independent pico-nets. Accordingly, the MB-OFDM system needs a fast switching frequency synthesizer for switching between sub-bands. In the proposal[3], among the five groups of frequency bands, the lowest group (3,168~4,752 MHz) is assigned as mandatory mode (Mode 1). Mode 1 has three sub-bands centered at 3,432, 3,960, and 4,488 MHz, respectively, and can support up to 200 Mbps data rate. Other groups of frequency bands are assigned for the optional mode or the future usage as technology improves.

This paper reports a dual-conversion CMOS RF front-end receiver development results for the MB-OFDM UWB system, which supports the lowest group of frequency bands 3,168~4,752-MHz(Mode 1).

Ⅱ. Receiver Architecture and Implementation

Fig. 1 shows the proposed dual-conversion receiver architecture for the MB-OFDM UWB system(Mode 1). As can be seen in Fig. 1, the receiver consists of a two-stage wideband LNA, an RF mixer, an IF *I/Q* mixer, and a frequency synthesizer. In Fig. 1, the incoming three RF sub-bands(centered at 3,432, 3,960, and 4,488 MHz, respectively) are first down-converted to the IF frequency of 1,320 MHz by the RF mixer, and then direct-converted to baseband by the IF *I/Q* mixer. In Fig. 1, the frequency synthesizer provides the fast-switching differential 1st-LO tones(2,112, 2,640, and 3,168

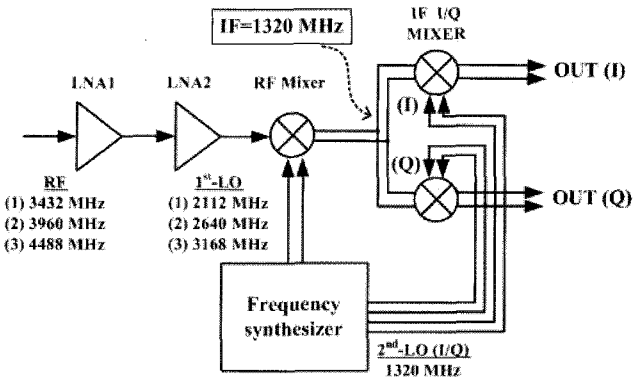

Fig. 1. Proposed receiver architecture.

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MHz, respectively) and one fixed *I/Q* 2nd-LO signal (1,320 MHz).

In the receiver chain, the LNAs can be implemented as a single-ended or differential topology. The differential LNA has high immunity to common-mode noises from the silicon-substrate and bonding-wire inductances, compared to the single-ended topology. However, the differential LNA needs an external or on-chip wideband balun for the differential signal driving. External balun considerably degrades noise performance in the receiver due to its insertion-loss. An on-chip active single-to-differential conversion circuit can dissipate a large dc current and degrade the linearity of receiver[4]. Furthermore, the differential LNA dissipates nearly twice the dc power and degrades noise figure compare to the single-ended LNA topology. In Fig. 1, the proposed receiver adopts a single-ended two-stage LNA, and the single-ended wideband output signal of LNA is converted into a differential signal at the output of the RF mixer. The adoption of a single-to-differential conversion by the RF mixer eliminates the requirement of balun circuit, which reduces dc power consumption in the receiver chain.

The dual-conversion architecture, which has been adopted in many narrow-band wireless systems[5],[6], has a number of advantages when adopted for MB-OFDM UWB system. In Fig. 1, the dual-conversion architecture allows differential(not quadrature) signals for the three fast-hopping LO tones (2,112, 2,640, and 3,168 MHz), which eliminates complex quadrature generation circuits and reduces dc power consumption of the synthesizer. In addition, in Fig. 1, the direct-conversion process occurs stably at a fixed IF frequency of 1,320 MHz, rather than at three different fast-switching LO frequencies(3,432, 3,960, and 4,488-MHz), like case of direct-conversion. Therefore, many of the direct-conversion issues(dc-offset, *I/Q* mismatch, and so on.) in the proposed receiver become the same as those of narrow-band direct-conversion receivers, which can be resolved by the well-known circuit techniques and compensation schemes[7]~[9].

In the proposed receiver(Fig. 1), the 1st- and 2nd-LO frequencies are carefully planed to avoid the image problem and simplify the synthesizer architecture. In Fig. 1, the image frequencies of three 1st-LO tones (2,112, 2,640, and 3,168 MHz) occur at 792, 1,320, and 1,848 MHz, respectively. Therefore, the image frequency bands are located outside of the wanted RF frequency band and can be suppressed by an external BPF. The aforementioned frequency planning allows simpler synthesizer architecture.

Fig. 2 shows the synthesizer architecture for the dual-conversion receiver shown in Fig. 1. As can be seen Fig. 2, the proposed synthesizer can provide four LO frequencies using only one PLL. One of the issues in synthesizer design is to reduce the number of mixer and frequency divider circuit for spectral purity of LO signals. In Fig. 2, the frequency synthesizer consists of the following components; a PLL, an *LC*-VCO, a divide-by-five, two polyphase filters, a single-side band(SSB) mixer, and a switch circuit. The *LC*-VCO resonates at 2,640 MHz, and the divide-by-five circuit and SSB mixer generate other two LO signals(2,112 and 3,168 MHz). The divide-by-five adopts an injection-locked frequency divider(ILFD) based on a ring-oscillator topology for low power and high frequency operation[10]. The switch circuit finally selects one of the three 1st-LO tones by external control signals. The quadrature 2nd-LO of 1,320 MHz comes from the divide-by-two circuit inside the PLL, which comes free and therefore saves the power dissipation and chip size. For higher isolation between four LO signals, the cascode type buffer amplifiers are located at the interface of each functional blocks in spite of additional dc power consumption. At the outputs of the 1st-LO signals, a differential LO buffer with resistive load is added to assure constant voltage gain for three LO frequencies.

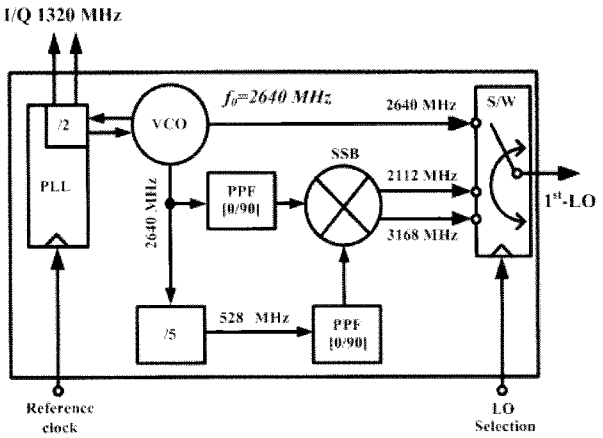

Fig. 2. Block diagram of the proposed frequency synthesizer.

Fig. 3 shows the schematic of a single-ended two-stage wideband LNA. In Fig. 3, each stage uses a cascode type amplifier with shunt-peaking load. To reserve enough bandwidth, the 3 dB bandwidths of LNAs are designed at 5.5 and 6.5 GHz for the 1st- and 2nd-LNA, respectively. The overall 3 dB bandwidth of amplifier is adjusted from 3 to 6.5 GHz. The design focus of the 1st-LNA is mainly wideband 50 ohm input matching and low noise figure. In Fig. 3, the 1st-LNA adopts the shunt-feedback resistor Rf onto a narrow-band cascode amplifier(M_1 and M_2) to achieve wideband input charac-

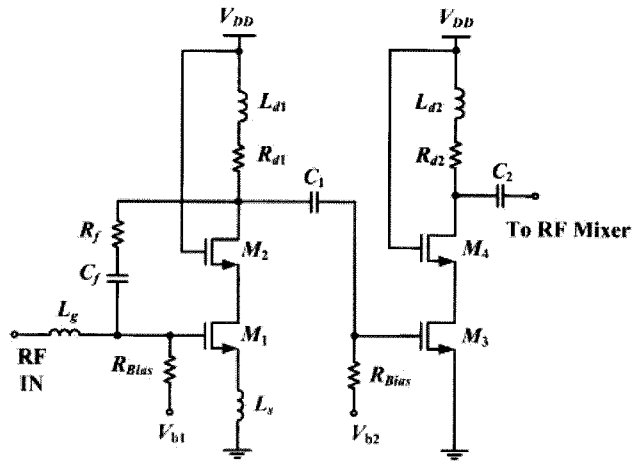

Fig. 3. Two-stage wideband LNA.

teristics[11]. The capacitor C_f is used for ac coupling purpose and L_s is the source-degeneration inductor. In the 1st-LNA, the wideband input matching of over 3.1~5 GHz is obtained by utilizing the feedback resistor R_f as a component to reduce the Q-factor of the input series resonant circuit in the narrow-band amplifier. Since the value of feedback resistor R_f can be high(1 Kohm), it contributes a small amount of noise degradation to the overall amplifier. The feedback resistor R_f also helps to extend the bandwidth of the amplifier and improve gain flatness over pass-band. The shunt-peaking load(L_{d1} and R_{d1}) of 1st-LNA is used to extend the bandwidth at high frequencies[12]. The 2nd-LNA is a cascode amplifier(M_3 and M_4) with shunt-peaked load(L_{d2} and R_{d2}), which is adopted to improve the noise performance of the receiver chain with high linearity. In Fig. 3, the shunt-peaking inductor L_{d2} of the 2nd-LNA compensates the impedance reduction with frequency at the drain node of M_4, due to the parasitic capacitances including the input capacitance C_{GS5} of the following RF mixer(Fig. 4). Accordingly, the RF signals are transferred from the output of the 2nd-LNA to the input of the RF mixer

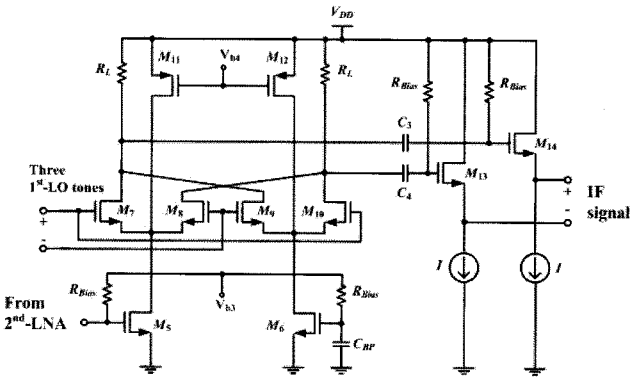

Fig. 4. The proposed single-to-differential RF mixer.

with flat wideband response. The same principle is applied at the interface between 1st- and 2nd-LNA as well. In Fig. 3, C_1 and C_2 are ac-coupling capacitors and R_{Bias} is a RF-blocking bias resistor.

Fig. 4 shows schematic of the proposed RF mixer, which consists of M_5~M_{12} and R_L. In Fig. 4, the RF mixer adopts a Gilbert cell topology, where a tail current source is removed to achieve enough voltage margin in this work. As can be seen in Fig. 4, for a single-to-differential signal conversion, the single-ended output of 2nd-LNA is ac-coupled to only one of the input transistor M_5 of the mixer in this work. The other input transistor M_6 of the mixer is ac-grounded with a bypass capacitor C_{BP}. Therefore, even though the proposed mixer operates like a single-balanced mixer with a conversion gain of $(2/\pi)\cdot(g_{m5}R_L)$, it can suppress the strong LO signal at the output nodes of the mixer by cross-connected switching transistors(M_7~M_{10}). Suppressed LO signal alleviates the linearity degradation of the following IF I/Q mixer circuit. Furthermore, the single-ended wideband RF signals are converted into fully differential IF signals at the output nodes of the mixer. These balanced IF signals are provided to input transistors of the following IF I/Q mixers in Fig. 1. Accordingly, in the proposed receiver, the single-to-differential conversion for RF signals is achieved without requiring any balun circuits. The source-followers(M_{13} and M_{14}) at the RF mixer output are adopted for the wideband flat frequency response near the IF frequency of 1,320 MHz. In Fig. 4, for better conversion gain and linearity, the RF mixer adopts the current-bleeding technique using PMOS transistors(M_{11} and M_{12})[13]. The IF I/Q mixer in Fig. 1 adopts the conventional Gilbert-cell topology, while sharing the common-transconductance stage for better I/Q matching. The resistive loads are adopted in IF I/Q mixer for wideband characteristic and lower $1/f$ noise.

Ⅲ. Measurement Results

The proposed RF front-end receiver is fabricated in 0.18 μm CMOS technology. The evaluations are done as chip-on-board(COB) and two passive LPFs are added on the PCB at the I- and Q-outputs of the receiver.

Fig. 5 shows the measured input return loss(S_{11}) of the receiver input, which shows lower than 8 dB over 3~5 GHz. Fig. 6 shows the measured receiver power gain and noise performance for the three RF sub-bands as a function of the baseband frequency. As can be seen in Fig. 6, the receiver front-end achieves power gain of 18.7~21, 17.5~19.5, and 16.3~18.7 dB for three sub-bands, respectively. The gain flatness for each band is 2.4, 2.0, and 2.3 dB, respectively. In Fig. 6, the receiver shows maximum noise figure of 7.6 dB for all three

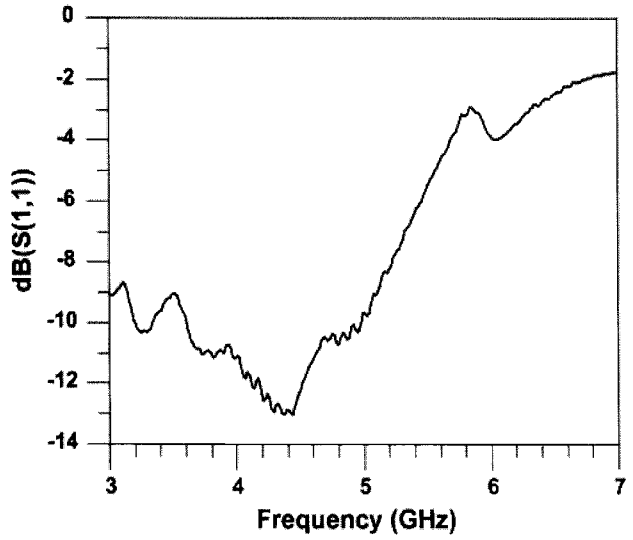

Fig. 5. Measured input return loss(S_{11}).

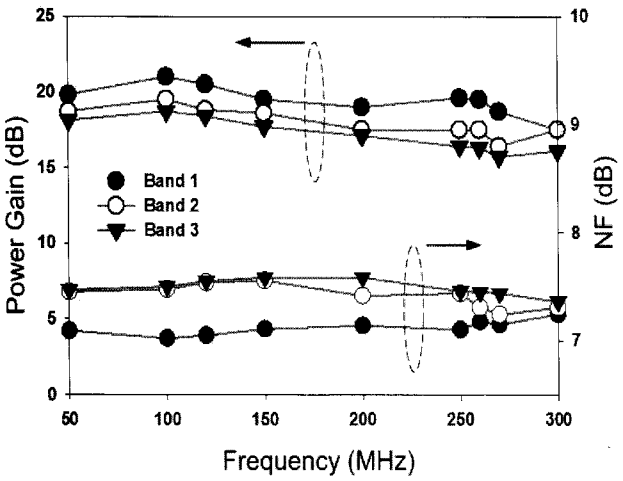

Fig. 6. Measured power gain and noise figure.

bands. The linearity of the receiver is tested by applying two in-band signals at 3,587 and 3,582 MHz. As shown in Fig. 7, the measured input-referred P1 dB and IP3 are -33 and -21 dBm, respectively. The LO-to-RF isolation is better than 50 dB for 1st-LO signals. The evaluation of the frequency synthesizer is also performed. The synthesizer shows clean LO signals with the sideband suppression ratio of 30, 43, and 22 dBc for the 1st-LO tones of 2,112, 2,640, and 3,168 MHz, respectively. In addition, the frequency-offset tolerance is less than 16 ppm and within the requirement of 20 ppm[3]. The phase noise for the 2.6 GHz LO frequency is measured 110 dBc/Hz at 1 MHz frequency offset.

Table 1 summarizes measured reveiver performances. The receiver chain and frequency synthesizer consume 78 mW and 112 mW from a 1.8 V supply, respectively. The Table 2 compares the performance of this work to

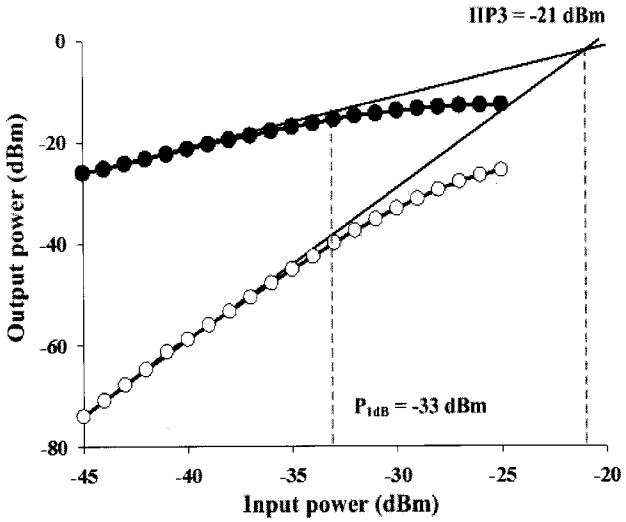

Fig. 7. Measured P1dB and IIP3.

Table 1. Summary of receiver front-end performances.

Parameters		Measured results
Frequency range		3.1~4.9 GHz
S_{11}		>−8 dB
Band 1	Power gain	18.7~21 dB
	Flatness	2.3 dB
	NF	<7.2 dB
Band 2	Power gain	17.5~19.5
	Flatness	2.0 dB
	NF	<7.5 dB
Band 3	Power gain	16.3~18.7
	Flatness	2.4 dB
	NF	<7.6 dB
P1 dB		−33 dBm
IIP3(High mode)		−21 dBm
LO-to RF isolation		>50 dB
VCO Phase Noise ($\triangle f$=1 MHz)		−110 dBc/Hz@2,640 MHz
Frequency synthesizer sideband suppression ratio		32 dBc/Hz for 2,112 MHz
		43 dBc/Hz for 2,640 MHz
		32 dBc/Hz for 3,168 MHz
dc Power (from 1.8 V)	Rx chain	78 mV
	Frequency synthesizer	112 mV

Table 2. Performance comparison.

Parameter	This work*	[14]	[15]	[16]	[17]*
Technology	0.18 um CMOS	0.13um CMOS	0.13um CMOS	0.18 um CMOS	65 nm CMOS
Frequency(GHz)	3.1~5	3.1~5	3.1~5	3.1~5	3.1~8
NF(dB)	7.2~7.6	6~7	6.5~8.4	4~4.7	5
P1 dB(dBm)	−33	n/a	−29.5	−9**	n/a
IIP3(dBm)	−21	−15	n/a	−0.8**	+5**
Dc power	190 mW (105 mA@1.8 V)	150 mW (100 mA@1.5 V)	237 mW (158 mA@1.5 V)	412 mW (229 mA@1.8 V)	137 mW (114 mA@1.2 V)

*w/o baseband blocks(LPF+VGA)
**Rx: low gain mode

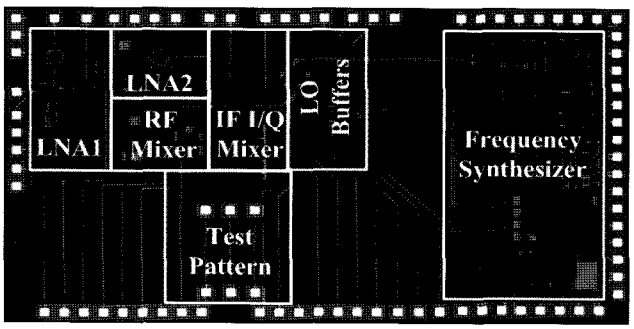

Fig. 8. Chip microphotograph.

recently reported CMOS UWB receivers. The microphotograph of the fabricated chip is shown in Fig. 8. In Fig. 8, the chip size with pads is 1.5×1.2 mm.

Ⅳ. Conclusion

A simple and effective dual-conversion RF front-end receiver is implemented using 0.18 μm CMOS technology, which supports the 3.1~5 GHz MB-OFDM UWB system(Mode 1). The advantages of the proposed architecture are discussed emphasizing the power consumption, chip size, spectral purity, implementation feasibility, etc. The proposed single-ended two-stage wideband LNA adopts the resistive shunt-feedback technique onto the conventional narrow band LNA topology to achieve wideband characteristics. In the receiver chain, the single- to-differential conversion for wideband RF input signals is achieved in the RF mixer without balun circuits. The simple and low power frequency synthesizer provides four LO frequencies from only one VCO. The receiver achieves a power gain of 16.3 to 21 dB, a noise figure of less than 7.6 dB, across three RF sub-bands, and IIP3 of −21 dBm. The frequency synthesizer shows a maximum side-band suppression ratio of 43 dBc and frequency-offset tolerance of less than 16 ppm for the 1st-LO signals. The receiver consumes 190 mW from a 1.8 V supply.

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