A Study on Improvement and Degradation of Si/SiO$_2$ Interface Property for Gate Oxide with TiN Metal Gate

Byung-Hyun Lee[a]
Advanced Technology Development Team 1, Semiconductor R&D Division, Samsung Electronics. Co. Ltd, San #24, Nongseo-dong, Giheung-gu, Yongin-si, Gyeonggi 446-711, Korea
School of Information and Communication Engineering, Sungkyunkwan University, Chunchun-dong, Jangan-gu, Suwon-si, Gyeonggi-do 440-746, Korea

Yong-Il Kim, Bong-Soo Kim, Dong-Soo Woo,
Yong-Jik Park, and Dong-Gun Park
Advanced Technology Development Team 1, Semiconductor R&D Division, Samsung Electronics. Co. Ltd, San #24, Nongseo-dong, Giheung-gu, Yongin-si, Gyeonggi 446-711, Korea

Si-Hyung Lee
Process Development Team, Semiconductor R&D Division, Samsung Electronics. Co. Ltd San #24, Nongseo-dong, Giheung-gu, Yongin-si, Gyeonggi 446-711, Korea

Yonghan Rho
School of Information and Communication Engineering, Sungkyunkwan University, Chunchun-dong, Jangan-gu, Suwon-si, Gyeonggi-do 440-746, Korea

[a]E-mail : byunghyun77.lee@samsung.com

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In this study, we investigated effects of hydrogen annealing (*HA*) and plasma nitridation (*PN*) applied in order to improve Si/SiO$_2$ interface characteristics of TiN metal gate. In result, *HA* and *PN* showed a positive effect decreasing number of interface state (N_{it}) respectively. After *FN* stress for verifying reliability, however, we identified rapid increase of N_{it} for TiN gate with *HA*, which is attributed to hydrogen related to a change of Si/SiO$_2$ interface characteristic. In contrast to *HA*, *PN* showed an improved N_{it} and gate oxide leakage characteristic due to several possible effects, such as blocking of Chlorine (*Cl*) diffusion and prevention of thermal reaction between TiN and SiO$_2$.

Keywords : TiN gate, Hydrogen anneal, Plasma nitridation, Interface state, *FN* stress, Activation energy

1. INTRODUCTION

By scaling down of the effective gate channel length into sub-50 nm region for advanced MOS device applications, metal gate electrodes are required to overcome many side effects originated from conventional poly-silicon gate, such as poly-depletion and high gate resistance[1]. Among several candidates for metal gate electrode, TiN, with a mid-gap work function on SiO$_2$ is regarded as a promising candidate for metal gate with several merits, such as good thermal stability, effectiveness for diffusion barrier, and good step coverage[2,3].

However, employing TiN gate electrodes in a conventional CMOS process poses new challenges which may cause considerable problems degrading device performance. Of the many problems, It is well known that the impurity (chlorine: *Cl*) contained in the CVD-TiN which is used to prevent the physical damage of gate oxide by PVD-TiN[4,5] degrades the gate dielectric reliability[6,7]. Also, it is reported that the TiN deposited above the gate oxide induces the mechanical stress, which result in the degradation of Si/SiO$_2$ interface characteristics and the change of C-V curve[8-10]. In addition to that, after high temperature process, a severe reaction between TiN and gate oxide may cause a change of gate oxide breakdown characteristic.

Of the problems due to an application of metal gate shown above, we focused on the Si/SiO$_2$ interface characteristics. Thus, we investigated Si/SiO$_2$ interface characteristics of TiN gate. And then, we applied hydrogen annealing (*HA*) before gate oxide formation and plasma nitridation (*PN*) after gate oxide formation as processes in order to improve Si/SiO$_2$ interface characteristics of TiN gate. Through that, we investigated the change of Si/SiO$_2$ interface characteristics, and considered about the effects of that processes affecting the Si/SiO$_2$ interface characteristics of TiN gate.

2. EXPERIMENT

The thickness of gate oxide was 40 Å. Poly-silicon was deposited with thickness of 1800 Å after 200 Å thick CVD-TiN had been deposited for TiN gate transistor. The poly-silicon gate transistor had been made with 2000 Å thick poly-silicon layer. The *HA* before gate oxide formation is applied at various time and temperature. For *PN*, in order to prevent degradation of gate oxide reliability due to supplement of hydrogen in SiO$_2$, it is applied to a N$_2$ ambient, not NH$_3$.

As a direct method to identify improvement of Si/SiO$_2$ interface property, the measurement of N_{it} using the charge pumping method was carried out. Gate induced drain leakage (*GIDL*) and sub-threshold slope (*SS*) was measured as an indirect method for identifying improvement of SiO$_2$/Si interface property. The major generation mechanism of *GIDL* is interface trap assisted tunneling and *SS* is degraded when interface capacitance is increased by interface trap charge. So, *GIDL* and *SS* have a close relation to Si/SiO$_2$ interface property[11,12]. For verifying reliability, the *FN* stress is carried out. (For *FN* stress, the same electric field which is calculated from Capacitance Equivalent Thickness (*CET*) through the C-V curve is applied to each sample.) Also, the bake of *FN*-stressed sample is carried out to investigate the difference of activation energy due to variation of N_{it}.

3. RESULT

First of all, we investigated N_{it} of poly-silicon gate and TiN gate for comparison of Si/SiO$_2$ interface characteristics due to the difference of gate material. In result, Fig. 1 shows that the N_{it} of TiN gate is larger than that of poly-silicon gate before and after *FN* stress. As mentioned above, this result is thought to be originated from several problems induced by an application of TiN gate, such as diffusion of *Cl* generated by CVD-TiN and mechanical stress induced by TiN. Through that, it is found that TiN gate has the poor Si/SiO$_2$ interface characteristics compared to poly-silicon gate.

Of the issues of TiN gate mentioned above, in order to verify an effect of *Cl* degrading Si/SiO$_2$ interface characteristics, we investigated N_{it} when *Cl* content for CVD-TiN is changed. In result, Fig. 2 shows that before and after *FN* stress, as *Cl* content for CVD-TiN is increased, the N_{it} of TiN gate is increased. As a result of Fig. 2, it is found that the increase of *Cl* content for CVD-TiN degrades Si/SiO$_2$ interface characteristics of TiN gate as already known.

In order to improve the result shown in Fig. 1, we applied *HA* before gate oxide formation and *PN* after gate oxide formation at TiN gate. It is reported that *HA* is effective for removing surface micro defects and improving surface roughness[13,14]. Thus, through the application of *HA*, we expected the improvement of Si/SiO$_2$ interface characteristic due to a reduction of surface roughness and surface micro defects.

For *PN* after gate oxide formation, it is well known that SiON generated by *PN* is an effective layer for blocking of boron penetration[15-17]. Thus, we expected that SiON formed at TiN/SiO$_2$ interface would block a diffusion of impurities including *Cl* to near the Si/SiO$_2$ interface. In result, before *FN* stress, Fig. 3 shows the decreased N_{it} of TiN gate with *HA* or *PN* compared to that without *HA* or *PN*. Fig. 4 shows that *GIDL* and *SS* also are improved by an application of *HA* and *PN*.

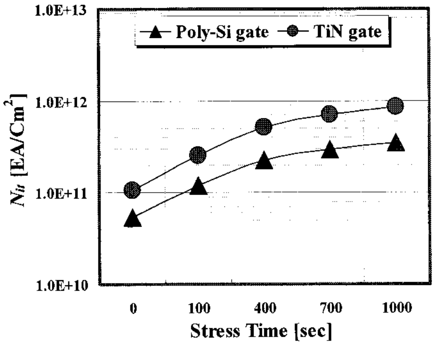

Fig. 1. The variation of N_{it} before and after *FN* stress.

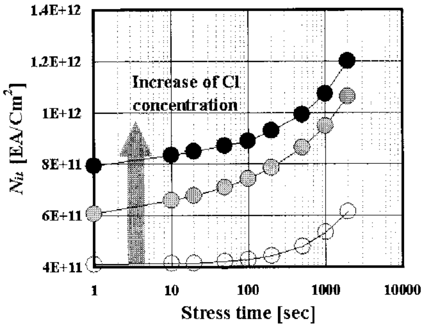

Fig. 2. The variation of N_{it} with *Cl* concentration of TiN gate transistors after *FN* stress.

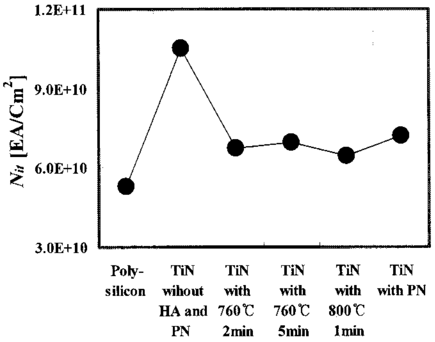

Fig. 3. The variation of N_{it} with application of *HA* and *PN* before *FN* stress.

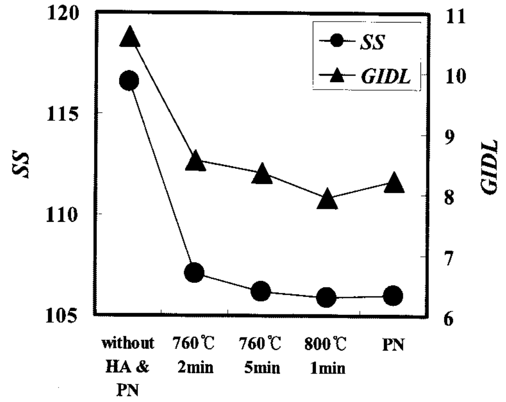

Fig. 4. The variation of *GIDL* and *SS* for TiN gate transistors due to an application of *HA* and *PN* before *FN* stress.

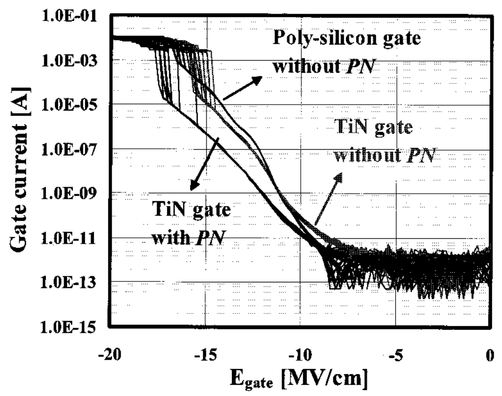

Fig. 6. E_{gate} vs I_{gate} characteristic of several samples.

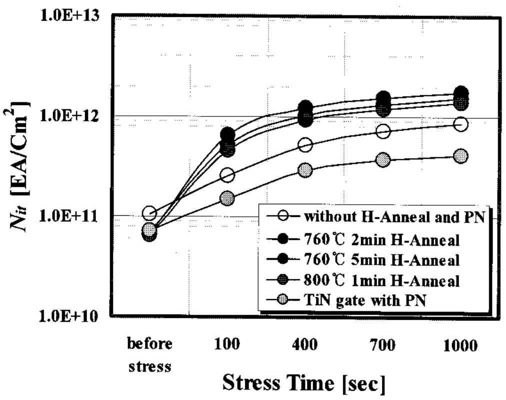

Fig. 5. The variation of N_{it} for TiN gate transistors with application of *HA* and *PN* after *FN* stress.

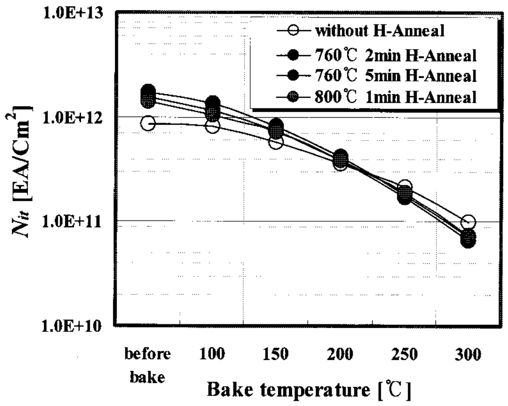

Fig. 7. The variation of N_{it} for *FN* stressd TiN gate transistors with *HA* after bake.

Through the result, it is thought that *HA* and *PN* is an effective process for improving Si/SiO_2 interface characteristics of TiN gate, and *HA* is more effective for improving Si/SiO_2 interface characteristics than *PN* due to improvement level.

After *FN* stress, however, Fig. 5 shows that the N_{it} of TiN gate with *HA* is rapidly increased compared to that without *HA* and *PN*, resulting in sharp variation of increase rate after *FN* stress of initial 100 sec. In contrast to result of TiN gate with *HA*, the N_{it} of TiN gate with *PN* is rather smaller than that without *HA* and *PN* after *FN* stress of 1000 sec, and the increase rate of N_{it} is also smaller than that without *HA* and *PN*. As a result shown in Fig. 5, it is expected that *PN* after gate oxide formation is effective process for improvement of Si/SiO_2 interface characteristic of TiN gate. In case of *HA* before gate oxide formation, however, it is found that an application of the process is not effective for complete improvement of Si/SiO_2 interface characteristics of TiN gate.

In addition to the improvement of N_{it}, an application of *PN* process is effective for improving gate dielectric leakage characteristic. Through the several comparisons between gate oxide of TiN gates with *PN* and that without *PN*, we could identify the effect of *PN* decreasing the physical thinning of gate oxide. As expected, Fig. 6 shows an improvement of gate dielectric leakage characteristic due to an application of *PN* process compared to TiN gate without *PN*, which is also thought as a result originating from the decrease of N_{it} as well as the decrease of physical thinning of gate oxide.

And then, in order to investigate a cause about rapid increase of N_{it} for TiN gate with *HA*, we baked *FN* stressed samples at various temperatures. In result, Fig. 7 shows that the N_{it} for TiN gate with *HA* was rapidly decreased compared to that without *HA*. Especially, after bake of initial 100 °C, the N_{it} for TiN gate without *HA* showed a little variation compared to that with *HA*.

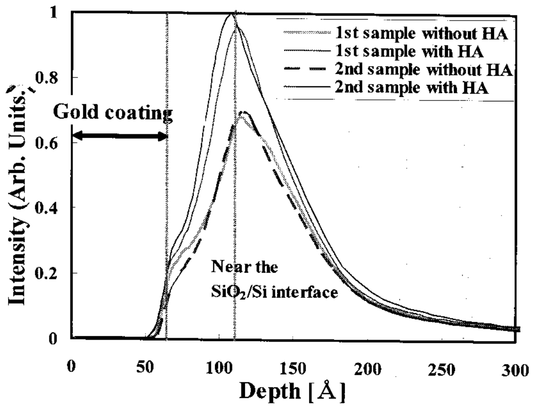

Fig. 8. The intensity of hydrogen using *SIMS* analysis after formation of gate oxide.

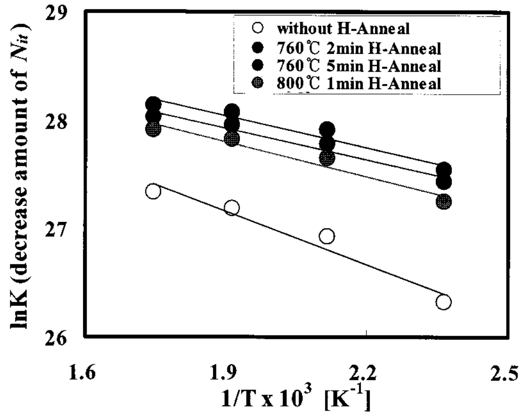

Fig. 9. The Arrhenius chart by bake temperature versus the decrease amount of N_{it}.

Table 1. The activation energy of TiN gate transistors calculated from Arrhenius equation.

Sample	Without *HA*	760 °C 2 min	760 °C 5 min	800 °C 1 min
Activation energy [kj/mol*K]	13.59	8.10	7.99	8.19

4. DISCUSSION

4.1 Hydrogen annealing effect

As shown above, through the rapid increase and decrease of N_{it} for TiN gate with *HA*, we can have any question about H*A* effect which affect Si/SiO$_2$ interface characteristics. It is well known that the gate oxide interface states are an unstable Si bonding such as dangling bond, and hydrogen exists in gate oxide with a various type (H, H$_2$, and H$^+$ et al), resulting in causing reaction for passivation and depassivation of interface state as follows[18,19];

$$D + H \rightarrow SiH, \qquad (1)$$

$$SiH + H \rightarrow D + H_2 \qquad (2)$$

where D is a dangling bond and SiH is a Si-H bond, respectively.

So, initially low N_{it} of TiN gate with *HA* is taught that the passivation reaction of dangling bond is more often with more fluent hydrogen supplied by *HA*, compared to that without *HA*, and the rapid increase of N_{it} for TiN gate with *HA* may be explained that more fluent hydrogen supplied by *HA* would induce the more depassivation reaction of dangling bond, as like reaction (2). After bake, it is also thought that rapid decrease of N_{it} for TiN gate with *HA* is originated from more frequent passivation reaction of interface state due to changed hydrogen intensity.

For verifying that, we investigated hydrogen intensity after gate oxide formation. In result, Fig. 8 shows that hydrogen intensity of TiN gate with *HA* is larger than that without *HA*. And as expected, we could identify the largest hydrogen intensity near the Si/SiO$_2$ interface. Thus, we may conclude that the variation of N_{it} for TiN gate with *HA* is originated from more frequent reaction (1), (2) induced by more fluent hydrogen supplied in silicon through the *HA*, not an effect improving Si/SiO$_2$ interface characteristic through the improvement of surface roughness.

As a result of Fig. 8, we can also infer that the changed concentration and type of hydrogen would cause the change of reaction for passivation and depassivation of interface state, resulting in the difference of activation energy needed for reaction related to passivation and depassivation of interface state. Eventually, it is thought that the decrease and rapid increase of N_{it} for TiN gate with *HA* is attributed to the difference of activation energy needed for reaction related to passivation and depassivation of interface state.

So, we applied the result of Fig. 7 to Arrhenius equation in order to calculate activation energy. As a result of that, Fig. 9 shows the decrease amount of N_{it} with increase of bake temperature, where the gradient x air constant means activation energy. Through the result of Fig. 9, Table 1 shows activation energy calculated from Arrhenius equation. As expected through the rapid change of N_{it} for TiN gate with *HA*, we could identify that the TiN gate with *HA* is needed a lower activation energy for the change of interface state than that without *HA*.

4.2 Plasma nitridation effect

PN is an effective process for blocking boron penetration causing a variation of device operation performance including a shift of threshold voltage, and it is already verified that *PN* changes the Si/SiO_2 interface hardness due to nitrogen introduced in gate oxide by nitridation[20,21]. Therefore, it is thought that before *FN* stress, the improvement of N_{it} for TiN gate with *PN* is originated from proper blocking of *Cl* or other impurities which diffuse in gate oxide or to near the Si/SiO_2 interface. Also, one possible explanation regarding improvement of N_{it} is that thin SiON layer formed between TiN and SiO_2 may decrease the mechanical stress of SiO_2 caused by TiN metal gate.

In addition, as shown in Fig. 5, an increase rate of N_{it} for TiN gate with *PN* is decreased with further stress time compared to that without *PN*, which is thought as a result that the formation of strong Si-N bond by nitrogen, in place of weak Si-H bond, reduces a possibility of interface trap generation under the *FN* stress.

Another positive effect by an application of *PN* process is an improvement of gate dielectric leakage characteristic, as shown in Fig. 6. In case of gate oxide with TiN gate not applied *PN*, it is well known that a severe reaction between TiN and the thermally grown SiO_2 gate dielectric decreases the insulator thickness by formation of a TiN_xO_y interfacial layer, resulting in increase of gate dielectric leakage current[22].

Figure 10 shows a formation of SiON layer due to an application of *PN*. As mentioned above, we could identify the effect of *PN* decreasing the physical thinning of gate oxide. Thus, it is expected that thin SiON layer between TiN and SiO_2 decreased thermal reaction between TiN and SiO_2, which is thought that an application of *PN* plays a positive role to improve thermal instability due to a use of TiN as a metal gate electrode.

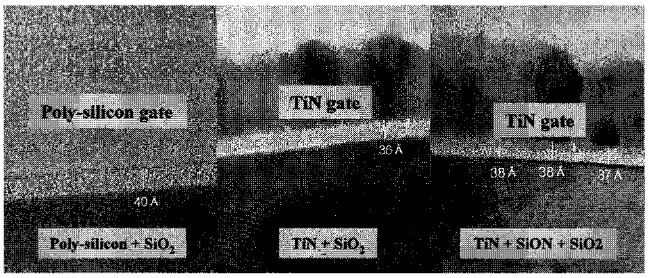

Fig. 10. The TEM of TiN gate with and without *PN*, and conventional poly-silicon gate.

5. CONCLUSION

In this study, we investigated the effect of *HA* and *PN* applied to improve unstable Si/SiO_2 interface characteristics due to an application of TiN metal gate electrode. In result, we could identify that the *HA* before gate oxide formation is not effective process for complete improvement of Si/SiO_2 interface characteristics, resulting in rapid degradation of Si/SiO_2 interface characteristics after *FN* stress for verifying reliability. It is resulted from role of hydrogen related to passivation and depassivation of Si/SiO_2 interface state, not effect due to a change of surface roughness. Whereas the *PN* process applied in N_2 ambient showed a positive effect for improving Si/SiO_2 interface characteristics as well as improvement of gate oxide leakage characteristic, which is thought as a result due to several positive effect effects of *PN*, such as effectiveness for blocking of impurity diffusion and increase of thermal stability through the prevention of reaction between TiN and SiO_2. Thus, we suggest that *PN* is an effective process for successful integration of TiN metal gate.

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