A New Scaling Theory for the Effective Conducting Path Effect of Dual Material Surrounding Gate Nanoscale MOSFETs

N. B. Balamurugan*, K. Sankaranarayanan, and M. Suguna***

Abstract—**In this Paper, we present a scaling theory for dual material surrounding gate (DMSGTs) MOSFETs, which gives a guidance for the device design and maintaining a precise subthreshold factor for given device parameters. By studying the subthreshold conducting phenomenon of DMSGTs, the effective conductive path effect (ECPE) is employed to acquire the natural length to guide the design. With ECPE, the minimum channel potential is used to monitor the subthreshold behavior. The effect of ECPE on scaling factor significantly improves the subthreshold swing compared to conventional scaling rule. This proposed model offers the basic designing guidance for dual material surrounding gate MOSFETs.**

Index Terms—**Dual material surrounding gate (DMSG) MOSFETs, drain induced barrier lowering (DIBL), scaling theory, short channel effects (SCEs), two-dimensional (2-D) modeling.**

I. INTRODUCTION

Scaling of MOSFETs to smaller dimensions has been a key driving force in the IC industry. As the channel length of MOSFETs enter the nanometer regime, short channel effects [1] become increasing significant and challenge the continuous improvement of MOSFET performance. Yan et al [2] proposed a unique scaling theory for single gate MOSFETs which gives a degraded subthreshold swing but they have not shown whether the same scaling factor with various device parameters gives the same factor. Suzuki et al [3] proposed a scaling rule for double-gate MOSFETs by assuming that the maximum potential at the SOI center is more sensitive to gate length than that at the surface and that the punch through current flows at the SOI center. But it is limited in offering a general guideline due to ignoring the high doping effect of the silicon film. With the same assumption as the central conduction mode for the low doped substrate, Auth et al [4] reported another scaling theory for SGT MOSFETs provided that the punch through current flows along the central conduction mode. Therefore, the models developed by Yan et al, Suzuki et al and Auth et al, cannot be used to predict sub-threshold by only considering the central channel conduction case. It is deficient in offering substrate effect. In this paper, we propose a novel scaling theory for dual material surrounding gate MOSFET which combines the advantages of both SG and DMG structure. The depth of the effective conducting path (d_{eff}) presents the location where the punch through current mainly occurs at subthreshold conduction with ECPE conducting mode. It is found that in addition to the device parameters such as thickness of oxide, channel length, and the scaling factor are also influenced by the depth of the effecting conducting path (d_{eff}). It is based on the new scaling theory α_4 associated with effective conducting path

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effect (ECPE). With ECPE, our model provides general guidelines for fully depleted SOI Dual material surrounding gate MOSFET.

II. SCALING THEORY

A schematic view of the DMSG Nanoscale MOSFET is shown in fig. 1 with gate consists of two materials M_1 & M_2 with gate lengths L_1 and L_2 and two different work functions V_{b1} and V_{b2}. The coordinate system consists of a radial direction r , a vertical direction z , and an angular component θ in the plane of the radial direction. The Poisson's equation for potential ϕ (r, z) in fully-depleted DMSG MOSFETs is

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\phi(r,z)}{\partial r}\right)+\frac{\partial^2\phi(r,z)}{\partial^2 z}=\frac{qN_a}{\varepsilon_{si}} \quad (1)$$

Where N_a is the channel doping concentration, $\phi(r,z)$ is the potential distribution in the silicon film, q is the electron charge, and ε_{si} is the permittivity of the silicon. Using the similar manner to Young's [5], we assume that the parabolic potential profile in the vertical direction of the channel is

$$\phi(r,z)=s_1(z)+s_2(z)r+s_3(z)r^2 \quad (2)$$

The boundary conditions required for the solution are given as follows [2]

(i) The central potential is a function of z only.

$$\phi(0,z)=s_1(z)=\phi_c(z) \quad (3)$$

(ii) The electric field in the center of the silicon pillar is zero by symmetry. Hence

$$\left.\frac{\partial\phi(r,z)}{\partial r}\right|_{r=R}=\frac{\varepsilon_{ox}}{R}\left(\frac{V_{GS}-\phi_s(z)-V_{FB}}{\ln\left(\frac{1+t_{ox}}{R}\right)}\right) \quad (4)$$

(iii) The electric field at r=R is continuous. Hence

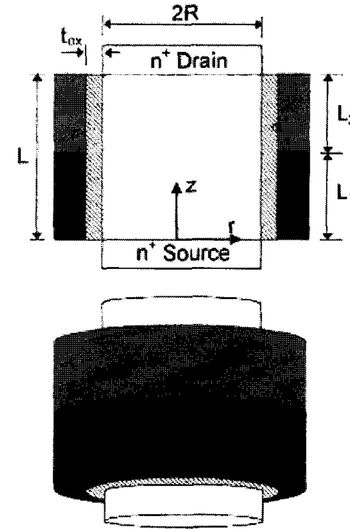

Fig. 1. Schematic view of dual material surrounding gate MOSFETs

$$\left.\frac{\partial}{\partial r}\phi(r,z)\right|_{r=0}=0 \quad (5)$$

(iv) The potential at the source end is

$$\phi(0,0)=\phi_s(0)=V_{bi} \quad (6)$$

(v) The potential at the drain end is

$$\phi(L_1+L_2,0)=\phi_s(L)=V_{bi}+V_{ds} \quad (7)$$

Where , V_{FB} is the flat band voltage, V_{GS} is the gate-source voltage, $\phi_S(z)$ is the surface potential along the channel, $2R$ is the diameter of the silicon pillar, t_{ox} is the silicon –oxide thickness, V_{bi} is the built in potential between the source and the body, V_{ds} is the drain-source voltage, and ε_{ox} is the permittivity of the oxide layer.

The constants $s_1(z)$, $s_2(z)$ and $s_3(z)$ in (2) can be found from above boundary conditions 1 to 3. Substituting (4) and (5) in (2) we get the value of $s_2(z)$ and $s_3(z)$ as,

$$s_2(z)=0 \quad (8)$$

$$s_3(z)=\frac{\varepsilon_{ox}}{2R\varepsilon_{si}}\frac{V_{GS}-\phi_s(z)-V_{FB}}{\ln\left(1+\frac{t_{ox}}{R}\right)} \quad (9)$$

Since $s_1(z), s_2(2)$ and $s_3(z)$ are known, the 2D potential $\phi(r,z)$ in (9) is expressed as,

$$\phi(r,z)=\phi_c(z)+\left[\frac{\varepsilon_{ox}}{2R\varepsilon_{si}}\frac{V_{GS}-V_{FB}-\phi_s(z)}{\ln\left(1+\frac{t_{ox}}{R}\right)}\right]r^2 \quad (10)$$

When the channel doping is increased, the electron potential at surface is greater than that at the center of channel. This will pull back the electron from the center of the channel to the surface and cause the punch through current to flow at the surface. On contrary, for the undoped SOI of $N_a=1.0\times10^{14}cm^{-3}$, the high center potential makes the electron retreat from surfaces into the depth and hence causes the electron flow near the center of channel. For the moderately doped substrate, the overall conduction is reasonably somewhere in between surfaces and channel center due to the relatively even spreading of free electrons. Therefore, to derive the unified scaling theory at subthreshold, the effective conducting path should be needed. . The depth of the effective conducting path (d_{eff}) presents the location where the punch through current mainly occurs at subthreshold conduction with ECPE conducting mode. It is found that in addition to the device parameters such as thickness of oxide, channel length, and the scaling factor are also influenced by the depth of the effecting conducting path (d_{eff}). In (10), accounting for ECPE, where the most leakage path $r=d_{eff}$ is at the position between surface of $r=R$ and body center of $r=0$, the potential in the effective conducting path is obtained as,

$$\phi_{d_{eff}}(z)=\phi_c(z)+\left[\frac{\varepsilon_{ox}}{2R\varepsilon_{si}}\frac{V_{GS}-V_{FB}-\phi_s(z)}{\ln\left(1+\frac{t_{ox}}{R}\right)}\right]d_{eff}^2 \quad (11)$$

From (10) and (11), the values of $\phi_s(z),\phi_c(z)$ are obtained as,

$$\phi_s(z)=\frac{\phi_{deff}(z)-A(V_{GS}-V_{FB})}{1-A} \quad (12)$$

and

$$\phi_c(z)=\frac{\phi_{deff}(z)-A(V_{GS}-V_{FB})}{1-A}(1+B)-B(V_{GS}-V_{FB}) \quad (13)$$

Where,

$$A=(d_{eff})^2\frac{\varepsilon_{ox}}{2R^2\varepsilon_{si}\ln\left(1+\frac{t_{ox}}{R}\right)}-\frac{\varepsilon_{ox}}{2\varepsilon_{si}\ln\left(1+\frac{t_{ox}}{R}\right)} \quad (14)$$

and

$$B=\frac{\varepsilon_{ox}}{2\varepsilon_{si}\ln\left(1+\frac{t_{ox}}{R}\right)} \quad (15)$$

Using (10), (11) and (12), we transform $\phi(r,z)$ to the following expression in which the function $\phi_{deff}(z)$ to be solved.

$$\phi(r,z)=\phi_{deff}(z)\left(\frac{1+B-Cr^2}{1-A}\right)+(V_{GS}-V_{FB})\left[Cr^2+\frac{ACr^2}{1-A}-\frac{A(1+B)}{1-A}\right]-B(V_{GS}-V_{FB}) \quad (16)$$

Where,

$$C=\frac{\varepsilon_{ox}}{2R^2\varepsilon_{si}\ln\left(1+\frac{t_{ox}}{R}\right)} \quad (17)$$

A simple scaling equation is obtained by substituting (16) into (1) and setting $r=d_{eff}$

$$\frac{d^2\phi_{deff}(z)}{dz^2}+\frac{V_{GS}-V_{FB}-\phi_{deff}(z)}{\frac{1+B-Cd_{eff}^2}{4C}}=\frac{qN_a}{\varepsilon_{si}}\frac{1-A}{1+B-Cd_{eff}^2} \quad (18)$$

It should be noted that for $R>>t_{ox}$ then, $\left(\ln\left(1+\frac{t_{ox}}{R}\right)\approx\frac{t_{ox}}{R}\right)$. The natural length may be obtained as,

$$\lambda_4 = \sqrt{\frac{2R}{8}\left(1 - \frac{2d_{eff}^2}{2R} + \frac{\varepsilon_{si} t_{ox}}{2\varepsilon_{ox}}\right)} \tag{19}$$

This natural Length is an easy guide for choosing device parameters, and has simple physical meaning that a small natural length corresponds to superb short channel effect immunity. Eq.(19) is simply a second – order 1D differential equation and can be uniquely solved by specifying the boundary conditions from (6) and (7), and the solution of (18) may be obtained as

$$\phi_{deff}(z) = \frac{1}{\sinh(\frac{L_{eff}}{\lambda_4})}\left[\begin{array}{l} K\sinh\left(\frac{L_{eff} - z}{\lambda_4}\right) + \\ N\sinh\left(\frac{z}{\lambda_4}\right)\end{array}\right] - J \tag{20}$$

Where,

$$J = \frac{qN_a}{\varepsilon_{si}}\frac{1-A}{4C} - V_{gs} + V_{fb} \tag{21}$$

$$K = V_{bi} + J \tag{22}$$

$$N = V_{bi} + V_{ds} + J \tag{23}$$

In a conventional SGT MOSFET, the gate is made of only one material, but in the DM-SGT structure, we have two gates with different work functions and doping density under them. Applying (20) to this device, we have

$$\phi_{d_{eff1}}(z) = \frac{1}{\sinh(\frac{L_{eff}}{\lambda_4})}\left[K\sinh\left(\frac{L_{eff} - z}{\lambda_4}\right) + N\sinh\left(\frac{z}{\lambda_4}\right)\right] - J$$

for $0 \le z \le L_1$, Under bottom gate M_1 (24)

$$\phi_{d_{eff2}}(z) = \frac{1}{\sinh(\frac{L_{eff}}{\lambda_4})}\left[\begin{array}{l} M\sinh\left(\frac{L_{eff} - z}{\lambda_4}\right) + \\ N\sinh\left(\frac{z - L_{eff}}{\lambda_4}\right)\end{array}\right] - J$$

for $L_1 \le z \le L_1 + L_2$, Under top gate M_2 (25)

The subthreshold conduction can be described by the minimum potential in effective conducting path. The minimum of the potential will occur at $z_{\min}$ by setting

$$\left.\frac{d\phi_{eff1}(z)}{dz}\right|_{z=z\min} = 0 \tag{26}$$

Substituting (24) in (26), we get

$$Z_{\min} = \frac{1}{2}\lambda_4 \ln\left[\frac{K - N\exp\left(\frac{L_{eff}}{\lambda_4}\right)}{N\exp\left(\frac{-L_{eff}}{\lambda_4}\right) - K}\right] \tag{27}$$

From (26) and (27), the minimum potential of $\phi_{d_{eff,\min}}$ can be solved. However, the solution is too complex to be used in deriving the explicit form of scaling factor. In terms of $\frac{L_{eff}}{\lambda_4} \ge 1$, the minimum potential with ECPE is given by,

$$\phi_{d_{eff,\min}} \approx \sqrt{NK}\exp\left(\frac{-L_{eff}}{2\lambda_4}\right) - J \tag{28}$$

And the minimum channel position becomes

$$z_{\min} = \frac{L_{eff}}{2} + \frac{\lambda_4}{2}\ln\left(\frac{K}{N}\right) \tag{29}$$

Since the punch through current at subthreshold primarily depends on the minimum channel potential of $\phi_{deff,\min}$ induced by effective conductive path; hence, with respect to the exponential term of (28), the scaling factor with ECPE is obtained as,

$$\alpha_4 = \frac{L_{eff}}{2\lambda_4} \tag{30}$$

As shown in (28), the novel scaling factor accounting for ECPE is derived. Once α_4 is determined, the relationship between device parameter of t_{ox} and R may be expressed by,

$$t_{ox} = \frac{\varepsilon_{ox} L_{eff}^2}{\alpha_4^2 \varepsilon_{si} 2R} - \frac{\varepsilon_{ox} 2R}{4\varepsilon_{si}} + \frac{d_{eff}^2 \varepsilon_{ox}}{\varepsilon_{si} 2R} \tag{31}$$

Eq. (31) is the key equation to adjust the device parameters for allowable scaling factor α_4. We can design the proper device parameters such as t_{si} and t_{ox} for certain effective conducting path d_{eff} to meet the required scaling factor α_4 at a given channel length L.

III. RESULTS AND DISCUSSIONS

Fig.2 shows the dependence of the channel length on the silicon oxide with different conducting models. The accuracy of the results obtained by our model is compared to the surface conducting model proposed by Yan at al [2] and to the central conducting model proposed by Suzuki et al [3]. It is obviously seen that central conducting model overestimates S-factor because of impractical assumption. The Surface S model underestimates the S-factor due to the unrealistic assumption. ECPE causes the electron to spread more close to the surface without considering the carrier confinement. So the proposed ECPE model demonstrates the improved subthreshold swing.

Fig.3 shows the dependence of the scaling capability on device parameters for central conducting model and ECPE conducting model with scaling factor of α_4=3. The result suggests that the central conducting model underrates the scaling capability when in comparison to ECPE conducting model. As shown in Fig. 3, when t_{si} increases, the allowable design space for t_{ox} and L_{eff} will become narrow. For the thickest silicon case, the effective gate length L_{eff} and the oxide thickness should be designed to less than 100nm and 4nm to reach the desirable scaling factor of 3 with less short channel effect. To obtain a good scalability factor with less short-channel effect, a thinnest silicon thickness of t_{si} =20nm which has the largest span of the design space for t_{ox} and L is preferred.

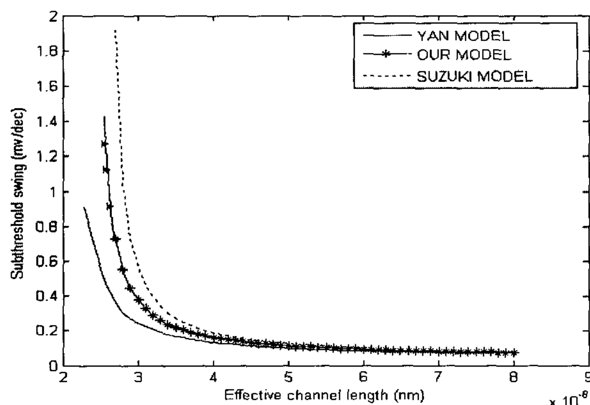

Fig. 2. The dependence of the subthreshold swing on the Gate length for various theoretical models

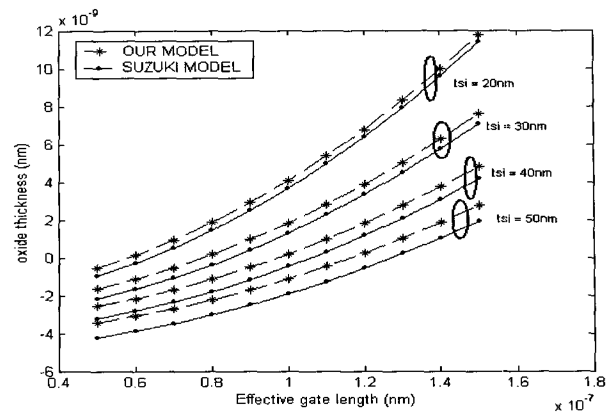

Fig. 3. Design contour for both double gate MOSFETs and dual material surrounding gate MOSFETs with different silicon thickness.

IV. CONCLUSIONS

We derived a scaling theory for dual metal surrounding gate MOSFETs based on the new scaling factor associated with ECPE. The device parameters are designed according to the scaling factor to obtain the proper subthreshold swing. It is seen that the small scaling factor cannot alleviate the short channel effects efficiently. The accuracy of the results obtained using our analytical model is compared with the other conventional scaling rule. The model provides a basic designing guidelines for dual metal surrounding gate MOSFETs.

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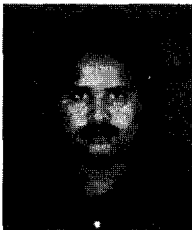

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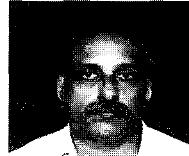

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