Overview of the Current Status of Technical Development for a Highly Scalable, High-Speed, Non-Volatile Phase-Change Memory

Suyoun Lee, Jeung-hyun Jeong, and Byung-ki Cheong

Abstract—**The present status of technical development of a highly scalable, high-speed non-volatile PCM is overviewed. Major technical challenges are described along with solutions that are being pursued in terms of innovative device structures and fabrication technologies, new phase change materials, and new memory schemes.**

Index Terms—**Non-volatile, phase-change memory, phase-change material, scalability, device speed**

I. INTRODUCTION

Since its revival from a 30-year-old relic (i.e., the original 256-bit prototype) as a 4-Mb prototype in 2002 [1], the non-volatile phase-change memory (PCM) has been under rapid development. In particular, a 512-Mb prototype was delivered in 2006 [2], and the first commercial product will most probably appear this year, positioning itself as the leading candidate for the next generation of non-volatile memories. By use of CMOS-compatible state-of-the-art fabrication technologies combined with a reliable memory material, the latest PCRAM prototypes provide superior writing endurance and speed than flash memory.

On one hand, these remarkable advances have substantiated the potential of PCM technology, but on the other hand, they have presented major challenges that must be overcome to open the pathway to a highly scalable, high-speed non-volatile memory technology. As for a high scalability, reduction of the current for a RESET operation will continue to be a cardinal issue because it is a key factor in the shrinkage of a memory cell, more specifically, a cell transistor. For that matter, fabrication of highly downscaled devices with proper functionalities poses a tough technical challenge by itself. In addition, multi-level storage capability will have to be implemented in the coming years to boost memory capacity. These tasks are compounded by another one, namely, improving the writing/sensing speed of a memory device (which appears to be a growing concern for higher-density PCM devices). Briefly stated, these challenges must be overcome with new device structures, fabrication techniques, memory materials, and so on, and major research and development activities are being actively exercised thereon.

The objective of this report is to present an overview of the latest technological developments for state-of-the-art PCM prototypes and beyond. In the first part, major components of state-of-the-art PCM devices are described. The second part is a review of the technologies under development for future PCM devices based on present memory material, i.e., $Ge_2Sb_2Te_5$ (GST). Lastly, problems concerning GST material are explained, and a review of research activities on alternative memory materials is presented.

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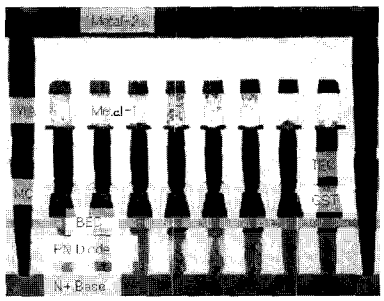
II. LATEST PCM PROTOTYPES AND TECHNOLOGICAL COMPONENTS

At present, a major hurdle to the commercialization of a PCM is its high RESET current (I_{RESET}). So far, the reduction of I_{RESET} has been mainly achieved by diminishing the programmed volume of the phase change material by reducing the contact area between the phase change material and the bottom electrode. As the contact area gets smaller, however, it becomes all the more difficult to control its distribution as well as its size. Other strategies have therefore been required, for example, devising a novel structure with a small contact size and thermal surroundings that efficiently confine heat or material engineering of phase-change material. In conjunction, use has been made of a cell switch with a large current supply for the required I_{RESET}.

1. 512 Mb Prototype by Samsung

Development of a commercial PCM is being led by research groups of many device manufacturers, such as Samsung Electronics, STMicroelectronics, and Intel. In making a high-density PCM, Samsung Electronics has been leading the race and announced the development of 512-Mb prototype at the 2006 International Electron Device Meeting (IEDM) [2]. Fig. 1(a) shows a cross-section view of a cell array of the 512-Mb prototype, featuring a 5.8 F^2 cell size and low-standby-power 90-nm CMOS technology. Such a high-density PCM was achieved by the following technical advancements. Firstly, a vertical pn-diode was adopted as a cell switch, for the first time, in place of a CMOS transistor, complemented with a self-alignment process for the bottom-electrode contact (SABEC) with a size of several tens of nanometers. In this way, a small cell with a cell switch of large current capacity was obtained. Secondly, a novel device structure with so called ring-type bottom-electrode contact (BEC) was employed. To fabricate the structure, the following process was developed: formation of a contact hole, deposition of a very thin metal-electrode layer, deposition of a core insulating layer in the hole, and chemical-mechanical polishing (CMP) [3]. Because of the ability to control the thickness of a thin metal layer much more accurately than a



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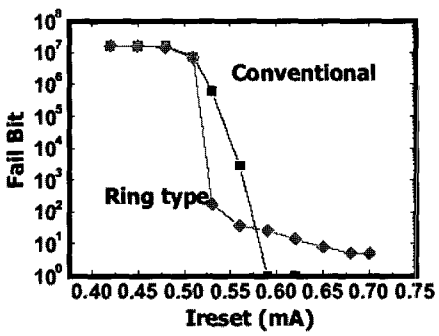


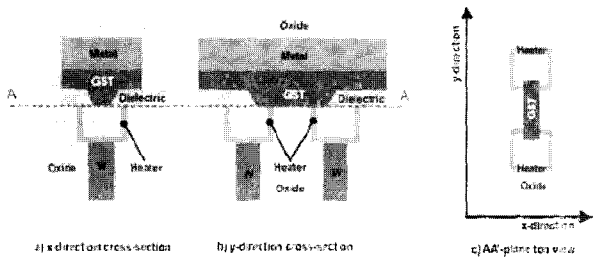
(b)

Fig. 1. (a) Cross-section view of a cell array in a 512 Mb prototype developed by Samsung Electronics, (b) Fail bit distribution of 16 Mb sample cell array for conventional and ring-type contact schemes.

lithographic feature size, a much smaller contact was obtained with much less scatter in size. Moreover, a line-type layout was used for the GST layer in order to prevent it from etching damage. Using these technologies with nitrogen-doped GST, I_{RESET} of about 0.6 mA, in conjunction with an improved distribution of fail-bits over programming current compared to the case of the conventional T-plug BEC scheme (see Fig. 1(b)), was obtained.

2. Prototypes by STMicroelectronics

Meanwhile, STMicroelectronics is leading the way in developing technology for reducing I_{RESET}, notably with an intelligent device structure called a "μTrench cell", featuring a small contact area as well as efficient heat confinement [4]. In the μTrench structure, as in the aforementioned ring-type contact, the contact area is determined by the thickness of an electrode layer. Unlike in the ring-type contact, however, it should be noticed that only a part of the larger cross-section of the electrode is used as a contact area (see Fig. 2(a)). In



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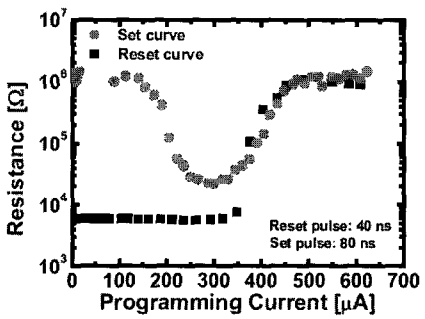
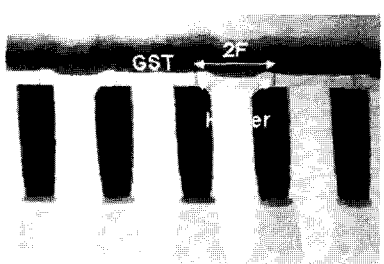


(b)

Fig. 2. (a) Schematic cross-sections and top-view, (b) programming curve of the μ-trench structure of a PCM developed by STMicroelectronics.



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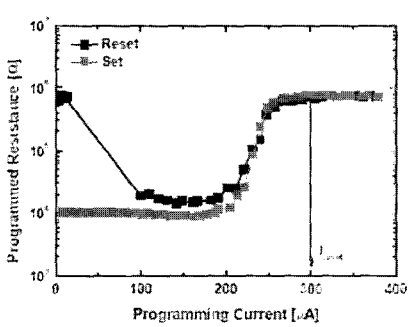


(b)

Fig. 3. (a) TEM cross-section (along y-direction) of the SA μTrench array, showing a large distance between two adjacent heaters that allows use of a non-critical mask for their definition (b) programming curve of a SA μTrench cell, showing that a full amorphization of the cell is achieved with a programming current of 0.3 mA.

addition, the μTrench structure adopts a confined-cell scheme that is advantageous over the conventional T-plug cell scheme in that the programmable volume is confined in a trench so that it has more thermally-resistive surrounding, thereby making more efficient use of joule heat. For a 4-Mb PCM test chip employing the μTrench structure, I_{RESET} of 0.45 mA was reported, as shown in Fig. 2(b) (2004 European Solid-State Device Research Conference). In 2007, a 128-Mb PCM based on 90-nm technology [5] that adopts an advanced version of the μTrench cell structure (called "self-aligned (SA)" μ-trench cell) (Fig. 3(a)) was successfully demonstrated. The self-aligning technique for forming heaters which eliminates the need for a critical lithographic patterning of the heater elements in the standard μTrench process, was developed. For the 128-Mb PCM, I_{RESET} of 300 μA was reported. This value, to our knowledge, is the lowest value at the megabit-density cell-array level.

III. TECHNOLOGICAL DEVELOPMENTS TOWARDS A HIGHER-DENSITY PCM

Research aimed at achieving a higher-density PCM is divided into three categories: further reduction of I_{RESET}, development of scalable devices utilizing GST nanowires, and development of device structures and programming methods for multi-level cell (MLC) operation.

1. Further Reduction of RESET Current

To obtain a lower I_{RESET}, new phase-change materials and thermally efficient cell structures are being sought. Recent efforts to develop these materials will be described in the following section. As for cell structure, realizing a confined structure (see the schematic illustration in Fig. 4(a)) is becoming a major fabrication issue. It was shown that a confined structure may lead to about 50% lower I_{RESET} than that of a T-plug structure [6]. For implementing this structure in a PCM device, a conformal-deposition technique that can fill the pores with a size of several tens of nanometers with a phase-change material is required. For this purpose, research to develop new deposition techniques for GST material (such as atomic-layer deposition (ALD), chemical-vapor

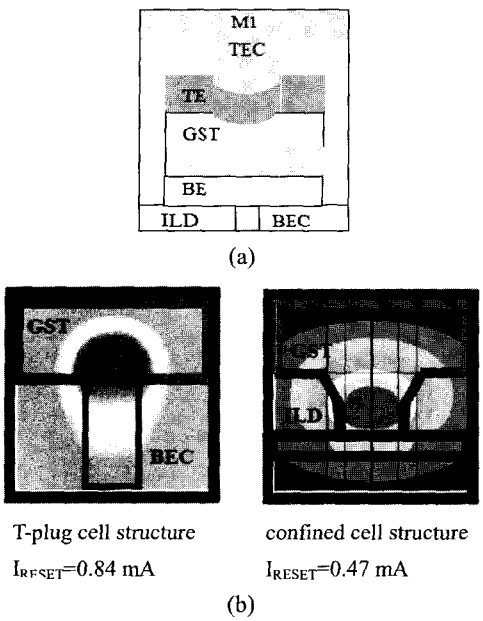


Fig. 4. A schematic illustration of (a) off-axis confined structure and (b) on-axis confined structure of a PCM.

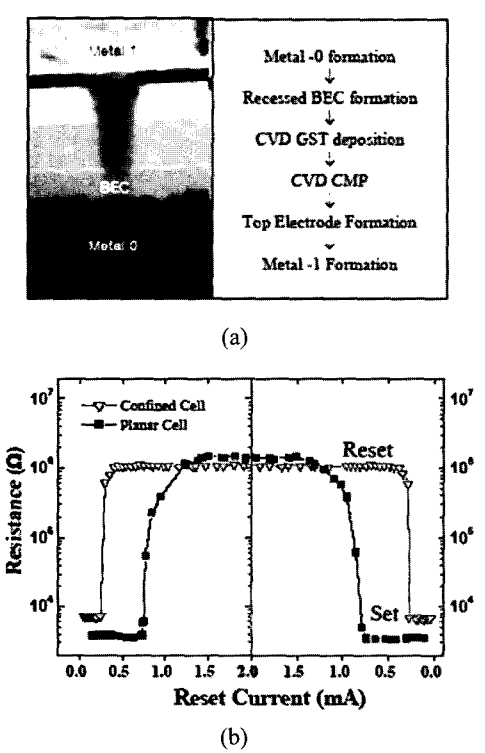


Fig. 5. (a) A cross-section view and the process flow, (b) programming curve of the fully confined cell structure developed by Samsung Electronics.

deposition (CVD), and advanced sputtering) is in progress.

Recently, researchers at Samsung Electronics produced a confined structure, where GST is fully

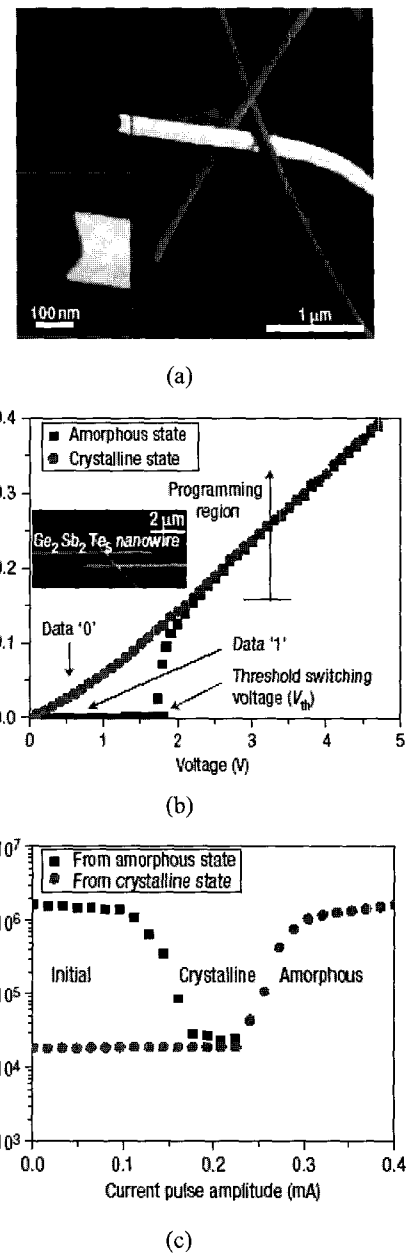


Fig. 6. (a) An SEM image of as-grown $Ge_2Sb_2Te_5$ nanowires with a faceted structure, (b) Current–voltage (I –V) characteristics of a 60-nm nanowire device (inset: SEM image) in amorphous(squares), and crystalline (circles) states, (c) Resistance change as a function of writing pulses with different current amplitudes (amorphization: 100 ns; recrystallization: 300 ns) obtained for initially amorphous (blue squares) and crystalline (red circles) phases.

confined inside a pore, as shown in Fig. 5, in a test device [7]. Such a fully confined structure maximizes the effect of physical confinement, as well as thermal confinement, of a programmable volume. CVD for highly conformal GST deposition and CMP for GST

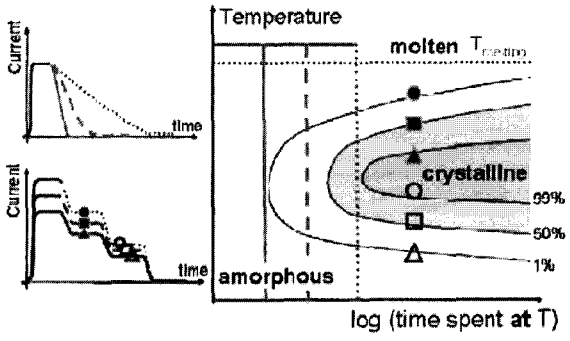
planarization were developed. I_{RESET} was reported to be 0.26 mA for a device with a pore with an aspect ratio higher than 3, that is, more than 150 nm deep and 50 nm wide. In addition, SET resistance (R_{SET}), another important device characteristic of a PCM regarding its scalability, was reported to be 6.7 kΩ, strongly suggesting that the fully confined structure combined with a CVD GST may be utilized as a promising technological ingredient for the development of a high-density PCM.

2. PCM using GST Nanowires

In pursuit of continuing scalability for a higher density PCM, a dilemma will be encountered; that is, the functionality of a phase-change material (as well as fabrication of a reliable device via top-down processing technology) will become questionable. With regard to this issue, a research group at the University of Pennsylvania recently reported a successful synthesis of GST nanowires, along with the characteristics of a PCM device made thereof, as shown in Fig. 6 [8]. According to their report, the devices made of GST nanowires of diameters down to 30 nm showed successful transitions between amorphous and crystalline states, suggesting that the GST material retains the required bi-stability and can be used for data storage down to the scale examined. It was also shown that I_{RESET} of the nanowire devices decreases as the diameter of the nanowire decreases. These results are certainly promising, but there remains much to be done before the demonstrated techniques can be applied to fabricate a reliable PCM device.

3. Multi-level Storage

The capability of multi-level storage is becoming an industrial standard for a high-density non-volatile memory. Based on its very high on/off resistance ratio (about 10^3), a PCM has been regarded as having a high potential for multi-level storage since the early stage of its development [9]. However, there have been few reports convincingly demonstrating the potential. This is due to the difficulty of reliable control over forming intermediate phase states, hence resistance states, in a reproducible manner. For this reason, other approaches to accomplish multi-level storage in a PCM have been



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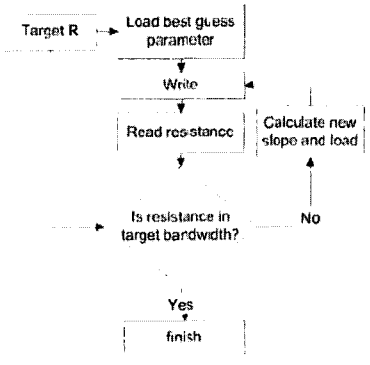


(b)

Fig. 7. (a) Staircase pulse scheme and schematic plot of time-temperature-transformation chart, (b) Programming algorithm using a verification step for controlling the resistance in the targeted range.

taken, for example, adopting multi-layer phase-change material for multiple programming volumes [10]. Recently, interesting studies were made on new programming methods with promising results, as described below.

Researchers at IBM made a systematic study of the controllability of the resistance of a PCM device at an intermediate state and proposed a new method for programming it. [11] The new method features a staircase-cooling scheme at the end of a writing pulse sufficient to melt a large region, and a verification step for controlling the device resistance in the targeted range (see Fig. 7). The authors successfully demonstrated four-level writing operations and showed that the resulting multi-level states were not degraded by repetitive reading operations for up to 10^3 seconds (corresponding to 1E9 cycles).

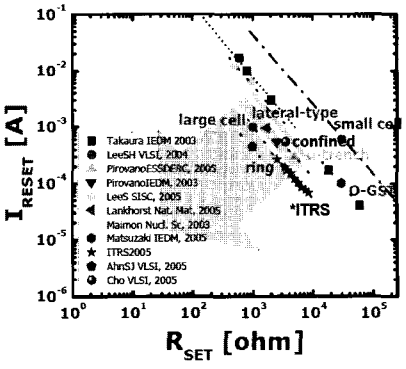
Another programming method was also recently proposed [12]. The authors studied the bias-dependence of the programming characteristics of a PCM device

with the pore-type structure to show that reverse biasing (top electrode: ground; bottom electrode: positive) leads to higher R_{RESET} and R_{SET} with increased I_{RESET}, I_{SET}, and extended t_{SET}. The observed bias-dependence was accounted for by the difference in the interface trap states between the bottom electrode/phase-change layer (PCL) interface and the top-electrode/PCL interface. We demonstrated that direct transitions from one state to another were highly reproducible, suggesting that the programming method is promising for reliable multi-level operation.

IV. Phase-Change Materials for High-Performance PCM

The current commercial developments of phase-change memory are based on the use of $Ge_2Sb_2Te_5$ (GST) as the memory material. For higher performance, GST-based PCMs must resolve two critical issues, namely, reduction of I_{RESET} and enhancement of SET speed. As for reduction of I_{RESET}, some successful improvements have been made by, for example, reducing contact area, cell-structure optimization, and nitrogen- or oxygen-doping into the GST; [13-15] however, most of these measures lead to an increase in SET resistance, as summarized in Fig. 8(a). Since the increase in SET resistance deteriorates the sensing margin and speed of a PCM, it must be avoided. Regarding the second issue, GST does not appear to have good prospects, in view of a latest report showing that a SET time of at least 300 ns is required for a high-density PCM prototype based on GST (see Fig. 8(b)). [16]

For these reasons, a new memory material for a higher density and higher speed with such features as lower I_{RESET}, higher SET and sensing speed, good sensing margin, and good data retention, may be in need. Material properties required for these device characteristics are summarized in Fig. 9. To deal effectively with the I_{RESET} issue, including that of thermal crosstalk, a material must have a lower melting temperature (T_m) and higher crystallization temperature (T_x), along with higher electrical resistivity (ρ) and lower thermal conductivity. For higher SET speed, it must have higher nucleation rate or growth speed, for higher crystallization speed. For better sensing characteristics,



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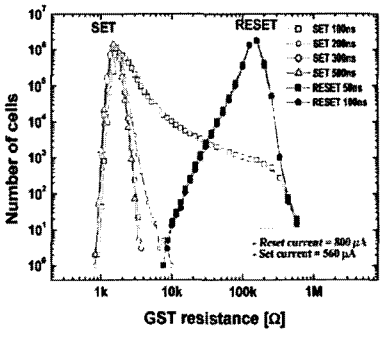

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Fig. 8. (a) Relationship between RESET current and SET resistance due to various approaches of lowering RESET current and (b) cell distribution in terms of SET and RESET resistance in an SEC 512 Mb prototype.

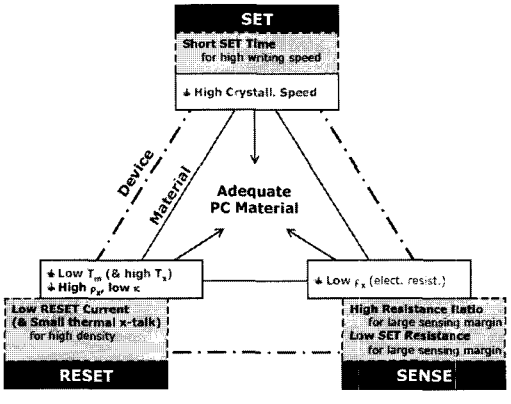

Fig. 9. Requirements for a high performance memory device and material.

the resistivity of a crystalline phase should be as low as possible, but this is in conflict with the requirement for a low I_{RESET}. Reasonably, it needs to be optimized through a judicious choice of a material system viz. a low-resistive base material doped with additives to increase resistivity.

A base material meeting the above requirements is desired to have a composition for eutectic melting or congruent melting, because the melting temperature is not only the lowest therein but also the thermodynamic driving force for crystallization is at minimum. There are several material candidates belonging to such material group: Ge-doped SbTe (called doped SbTe for short) [17,18] based on an Sb:Te composition belonging to the δ phase field of the Sb-Te binary phase diagram, GeSb [19], and Se-Sb-Te [20] of eutectic compositions. Melting temperatures of these materials are, respectively, 544.5°C ($Sb_{72.3}Te_{27.7}$), 592°C ($Ge_{14.5}Sb_{85.5}$), and 422°C ($Sb_{7.4}Te_{92.6}$) according to the respective binary phase diagram.

1. Doped SbTe

Doped SbTe materials are well known for their successful use in high-speed phase-change optical recording media, including Blu-ray® DVD discs. [21,22] A few important characteristics of a doped SbTe material are summarized and compared with those of GST in Figs. 10(a) and 10(b). Firstly, the doped SbTe crystallizes in a growth-dominated mode in contrast with the nucleation-dominated crystallization mode of GST. Secondly, the doped SbTe has a higher crystallization temperature and lower electrical resistivity in both amorphous and crystalline states. In regards to the difference in crystallization mode between the two materials, a discontinuous and complete transition of sheet resistance in the case of doped SbTe, as compared with a gradual transition in the case of GST, is also noticeable. As for a growth-dominated PCM material, it may reasonably be deduced from these characteristics that crystallization of an amorphous programmed region in a PCM device initiates from the amorphous/crystalline (α/x) phase boundary and progresses towards the center of the programmed region. As such, the device tends to have a very fast SET speed if the size of the programmed amorphous region is small enough and if the material has a sufficiently high growth speed (which is indeed the case with the doped SbTe material).

A PCM device based on doped SbTe was first demonstrated by Phillips, using a novel planar device called phase-change line memory. [17] It was shown that SET time could be reduced to below 50 ns and I_{RESET} to

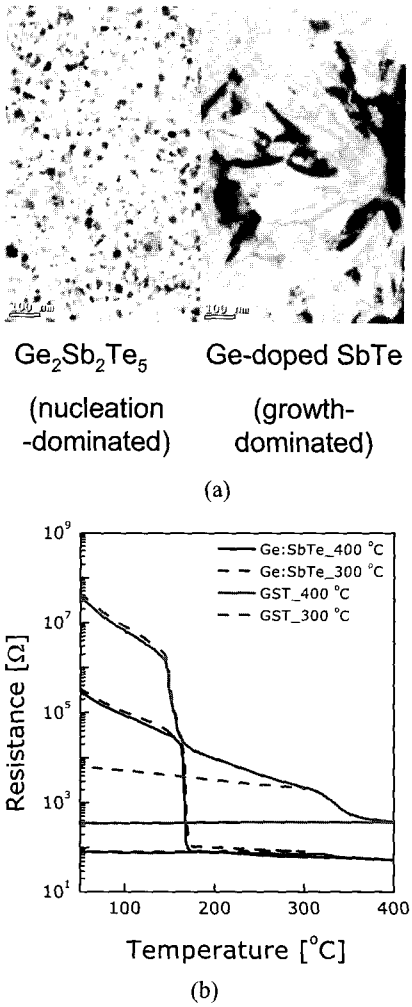

Fig. 10. (a) TEM microstructures of crystallized GST and Ge-doped SbTe and (b) resistance vs. temperature plots of the two materials.

below 200 μA. The focus of their work was mostly on the effectiveness of a new cell design (with a cross-section for current flow that is adjustable by changing film thickness of the PCM material line), and the device characteristics of doped SbTe were not systematically compared with that of GST. Recently, we examined Ge-doped SbTe (Ge-ST) with a conventional pore cell structure [18], and showed that SET time could be down to 20 ns, thereby confirming the usefulness of Ge-ST as a high-speed PCM material. The fast SET was attributed to the fast motion of the α/x phase boundary, as mentioned above. With respect to data retention characteristic, doped SbTe was found to be comparable to GST; that is, a device with doped SbTe was estimated to retain a RESET state for 10 years at 100°C as compared with 105°C for a GST-based device. [23]

With respect to I_{RESET}, it is not clear whether or not doped SbTe is more favorable than GST. In Phillips' work, I_{RESET} for doped SbTe seems to be comparable to the estimated value for GST for a similar cross-section, but the comparison is not valid because of the difference in the memory cell structures of these two materials. In the authors' work [18], I_{RESET} of Ge-ST was higher, most likely due to Ge-ST's lower electrical resistivity (see Fig. 10(b)) and higher thermal conductivity (which would lead to less joule heating and more heat dissipation, thereby overruling a gain from a lower melting temperature). Nitrogen was added into Ge-ST to increase the electrical and thermal resistivity of the crystalline Ge-ST. As a result, I_{RESET} was reduced with increasing nitrogen concentration with little increase in SET time. [18]

2. GeSb

GeSb has material characteristics similar to those of doped SbTe. It has an eutectic melting at an Ge:Sb ratio of 14.5:85.5 (T_m = 592°C), and higher crystallization temperature (T_x is even higher by about 100°C than doped SbTe) but lower crystalline resistance than GST. It also shows growth-dominated crystallization. The feasibility of GeSb as a PCM material was first reported by IBM in 2006—in another novel planar device called a "phase-change bridge memory" [19], in which doped GeSb with an unspecified doping element was used instead of GeSb. The basic design concept of the device, i.e. minimizing the cross-sectional area for current flow, is essentially the same as in the case of the phase-change line memory developed by Phillips, except that the distance between lateral electrodes is also minimized by controlling the thickness of the interlaying SiO_2 layer.

As for SET speed, pertinent device data was not presented, but it was shown by pulsed-laser experiment that doped GeSb could be crystallized faster than GST. With respect to I_{RESET}, the IBM report showed that it could be reduced to 90 μA at a cross-sectional area of 60 nm^2, a world record. However, this remarkably small I_{RESET} is not a material attribute but is a device attribute due to its extremely small cross-section. Data retention of doped GeSb seems to be sufficient, considering its high crystallization temperature (about 260°C). No assessment of the temperature for a 10-year lifetime was made, but it was reported that a RESET state was maintained for several minutes at around 175°C.

3. Se-Sb-Te

In the Sb-Te binary phase diagram, another eutectic composition is found in the Te-rich region (T_m = 422°C at Sb:Te=7.4:92.6). As compared with the melting temperature of GST, that of Sb-Te is more than 200°C lower, suggesting that the RESET current could be reduced significantly for a device made thereof. Se-Sb-Te and As-Sb-Te having Se or As in the Te-rich Sb-Te were suggested as phase-change materials with low melting temperatures of below 400°C. [20,24] With respect to crystallization, Se-Sb-Te appears to be crystallized in a growth-dominated mode. [25] Unlike doped SbTe and doped GeSb, its crystallization speed is fairly low, however.

Se-Sb-Te and As-Sb-Te were tested by Nakayama et al. [20,24] with respect to device characteristics. For both materials, RESET current was found to be one fourth of the value for GST. Nevertheless, SET speed does not look promising. In the case of As-Sb-Te, SET time was high, reaching typically 100 μs. Se-Sb-Te led to better SET time, i.e., less than 500 ns, but that is not still comparable to a typical SET time of a GST-based device, i.e., less than 100 ns.

V. CONCLUSIONS

The present status of technical development of a highly scalable, high-speed non-volatile PCM was overviewed. From a scalability perspective, the primary challenge has been reducing RESET current. To meet that challenge, the latest PCM prototypes carry various technological innovations, namely, cell structures with a small contact size (such as a cell structure with a ring-type BEC or a μTrench cell structure), use of nitrogen-doped GST, and use of a cell switch capable of a high current supply (such as p-n diode or bipolar junction transistor). For a higher-performance PCM surpassing the present prototypes, the challenge gets tougher and furthermore compounded with the added challenge of increasing device speed. Solutions are being pursued in terms of innovative device structures and fabrication technologies, new phase change materials, and new memory schemes such as multi-bit cell technology.

Briefly phrased then, PCM has come a long way of technology development to the first commercial product at near sight, yet to go another long way of exciting technological challenges in the years ahead.

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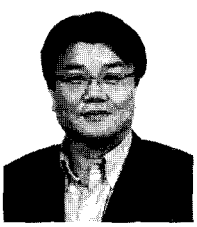

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