# The Study of the Cycle Time Improvement by Work-In-Process Statistical Process Control Method for IC Foundry Manufacturing

**Yu-Cheng Lin[1], Chih-Hung Tsai[2†], Rong-Kwei Li[1], Ching-Piao Chen[2] and Hsien-Ching Chen[3]**

[1]Department of Industrial Engineering and Management
National Chiao-Tung University, Hsin-Chu, Taiwan, ROC.

[2]Department of Industrial Engineering and Management
Ta-Hwa Institute of Technology
1 Ta-Hwa Road, Chung-Lin
Hsin-Chu, Taiwan, ROC.
Tel: +886-3-5927700~2953
E-mail: ietch@thit.edu.tw

[3]Center for General Education, Chung-Hua University
No.707, Sec.2, WuFu Rd., Hsin-Chu, Taiwan 300, R.O.C

## Abstract

The definition of cycle time is the time from the wafer start to the wafer output. It usually takes one or two months to get the product since customer decides to produce it. The cycle time is a critical factor for customer satisfaction because it represents the response time to the market. Long cycle time reflects the ineffective investment for the capital. The cycle time is very important for foundry because long cycle time will cause customer unsatisfied and the order loss. Consequently, all of the foundries put lots of human source in the cycle time improvement. Usually, we make decisions based on the experience in the cycle time management. We have no mechanism or theory for cycle time management. We do work-in-process (WIP) management based on turn rate and standard WIP (STD WIP) set by experiences. But the experience didn't mean the optimal solution, when the situation changed, the cycle time or the standard WIP will also be changed. The experience will not always be applicable. If we only have the experience and no mechanism, management will not be work out. After interview several foundry fab managers, all of the fab can't reflect the situation. That is, all of them will have an impact period after product mix or utilization varied. In this study, we want to develop a formula for standard WIP and use statistical process control (SPC) concept to set WIP upper/lower limit level. When WIP exceed the limit level, it will trigger action plans to compensate WIP Profile. If WIP Profile balances,

† Corresponding Author

we don't need too much WIP. So WIP level could be reduced and cycle time also could be reduced.

**Key Words**: Foundry, Manufacturing Cycle Time, Delivery, Dispatch, Work-in-Process Management

# 1. Introduction

This study adopted a semiconductor foundry in Taiwan's Hsinchu Science Park for case study. This company transformed from a DRAM manufacturer to a specialized foundry, and it has set up good reputation and customer base gradually in this industry after several years of exploration and learning. However, it is still behind the leading foundries in the industry. The gaps are analyzed based on three principal indexes most concerned by the clients, which are quality, cost and due date. Because the company has focused on high voltage products and centralized the resources, clients are very satisfied with the product quality. As for the cost, most machines of the company have exceeded the period of depreciation (the maximum factor in manufacturing cost of semiconductor), the depreciation is kept at a very low level, so the cost has great competitive power. Clients' complaints are mainly concentrated on product due date and cycle time, according to the production data, the product cycle time of the company is obviously longer than those of others in the same industry. Therefore, the due date and cycle time should be improved if the company wants to promote its competitive power and customer satisfaction. The management of the company also knows this issue, but there has been no obvious improvement so far. The countermeasure of the foundry is just performing machine control and regular reviews afterwards, but it is short of prior programs and systematic improving methods. Therefore, the machine always crashes when we need it, here the reviews cannot retrieve the lost production. The production control department of the company adopts uniform loading, namely considers the yield rate according to the output plan of each month, and divided by the number of days of that month to figure out the wafer input plan, this cannot reflect the production status of foundry. On the other hand, the manufacturing department is always disputing about standard work-in-process (STD WIP), and it often argues about which machines having how many work-in-process could be regarded as normal, presently the STD WIP stipulated is based on empiric value and lacks support of theoretical basis. Additionally, the foundry management and dispatching are lack of feedback management system, so that it can hardly increase the production efficiency effectively. So building an effective work-in-process management system is the most urgent issue to the company at present.

This study hopes to provide a good manufacturing management system to improve the

most urgent issue at present, such as unsatisfactory due date and cycle time, and to promote company's competitive power and customer satisfaction. Besides, it hopes to provide a channel for communications between production management personnel and manufacturing site staff, to avoid the communication mode by which there are only mutual rebukes but no concrete proposals and action projects. Firstly, this study will discuss relevant literatures to work-in-process management and bottleneck management, and collect previous studies and improvement methods of due date and cycle time, and collect available data, practical observations and analyses to find out matters influencing the due date and the cycle time. When the matters are found out, a model and method which can improve current issues would be constructed, namely a concept of WIP statistical process control is led, the problems would be improved by systematic methods. Finally, the improvement effect of WIP SPC model would be demonstrated by real data. The range and limit of the study is: (1) this study takes pure-play foundries as the study object; (2) the form of production is make-to-order; (3) the system constraint is machine capacity without manpower factors; (4) assuming the limit is the production capacity of foundry.

## 2. Literature Review

In the literatures relative to release and dispatching, numerous theories have made prominent contributions to discussions about the cycle time (Akcah and Uzsoy, 2001; Uzsoy *et al.*, 1992/1994; Malmstrom, 1997; Levitt and Abraham, 1990; Lou and Kager, 1989; Hung and Leachman, 1996; Huang, 1998; Lu, 2004; Chen, 2006; Hsu, 2007), described as follows:

### 2.1 Release Rules

In some previous studies relating to semiconductor manufacturing management, scholars use emulations to demonstrate the impact of release on due date and cycle time is greater than that on field scheduling and dispatching in foundries (Tu, 1998; Lu, 2004; Chen, 2006; Hsu, 2007; Glassey and Resende, 1988a/b; Wein 1988; Miller, 1990; Leachman and Hodges, 1996; Lawton, 1990). The release rule can be probably divided into two types: open-loop and close-loop. The open-loop means putting in fixed quantity in fixed time intervals, namely carrying out wafer input without respect of field status, for example, the uniform loading. While the close-loop release considers the field work-in-process or machine load as the basis of release. Generally, the close-loop release rule would adjust the release according to the dynamic changes in manufacturing field, and its production performance is better than that of open-loop release rule. A brief introduction of close-loop release rule is given as follows:

(1) Fixed-WIP (FW) release rule: Under the concept of output rate being equivalent to re-

lease rate, when a system yields a product, a part must be put in the system to maintain WIP fixed, this rule determines release time point based on output rate.

(2) Constant WIP (CONWIP) release rule: It adopts billboard concept for release, and it is a production control type between JIT and push system (Spearman *et al*., 1990). There is only one kind of billboard in the same production line, when a part is sent to the production line, the billboard would be attached to the part till the part leaves the production line, and then the empty billboard would be sent back to the first step, but the priority of ingoing part needs to be scheduled in advance.

(3) Starvation Avoidance (SA) release rule: SA release rule was put forward by Glassey and Resende (1988a/b), aiming at semiconductor manufactories which take machine crash and repair as main random source of variation, its main target is to increase the usage of bottleneck machines (B/N), and shorten the cycle time and improve the due date at the same time. Its central concept is reducing WIP, but timely release is required in order to avoid B/N Movement Loss. Its release is controlled by setting a key value which is the product of operation time (L) and safety factor ($\alpha$, $\alpha > 0$) of releasing to B/N. When the WIP of bottleneck is lower than the set value, release shall be carried out. When the productive capacity approaches full load, SA's performance on due date has a quite positive difference from that of other release methods such as Uniform/Fixed WIP.

(4) Workload Regulating (WR) release rule: Workload Regulating (WR) release rule was put forward by Wein (1988), it takes current overall working load of constraint resource workstation in the system (or substantial inventory; W) as the basis of release decision. Release shall be carried out when the rest process time of bottleneck is lower than the set working load value, this rule is different from SA that it brings parts which have entered the system into calculation as long as further process needs to use constraint resource, it can exactly reflect future machine load and realize maximum machine utilization.

(5) Drum-buffer-rope (DBR): The plan and control of DBR production management system developed from theory of constraints are carried mainly through concepts of drum, buffer and rope (Wu and Li, 2003). DBR emphasizes making the most of capacity of bottleneck resource, so it stipulates a detail scheduling aiming at the bottleneck resource, it is called "Drum." Drum is obtained by using Backward Scheduling and based on order's due date, time buffer and control rod, and reduce corresponding temporary storage area for resource according to the time of commencement of each work order on Drum, then the release schedule is deduced, this is called "Rope", detailed procedure is as follows:

Step 1: Identify the system constraint [resource constraint for maximal load or insufficient

capacity, market demand constraint].

Step 2: Exploit the system constraint [products limited by capacity should make maximum use of that machine with capacity constraint, so Drum is the scheduling of that machine, and products limited by market should make use of the market demand constraint, so Drum is the delivery rhythm of these products].

Step 3: The system fully subordinates the policy of Step 2 [non-constraint resources, protection and buffer of unstable system's state and subordination of release rhythm].

Step 4: Elevate the system constraint.

Step 5: If the constraint is broken in Step 4, then return to Step 1, don't let inertia become the system constraint.

### 2.2 Dispatching Rules

Dispatching rules reduce the impact of unpredictable events in manufacturing field on batch production cycle time through changing the batch processing sequence. A good release policy cannot exert its efficiency completely without proper dispatching rule. A brief introduction of dispatching rules is given as follows:

(1) First in First Out (FIFO): the processing order is determined by the order of arriving at workstation, the earlier the part arrived, the higher priority it would have.

(2) Earliest Due date (EDD): Parts of later Due date would have higher processing priority, it is a dispatching rule based on due date guiding.

(3) Critical Ratio (CR): Divide the remaining available time of each part prior to due date by the remaining process time, the resulted value is called critical ratio, higher processing priority would be provided for those have lower CR value, such a dispatching rule is called Critical Ratio, it is a dispatching rule guided by due date.

(4) Minimum Slack Time (MST): Reduce remaining required process time from the remaining available process time of each part prior to due date, the resulted value is called slack time, the shorter slack time the part has, the higher priority it would have, it is a dispatching rule guided by due date.

(5) Short Remaining Processing Time (SRPT): The shorter the remaining overall process time is, the part would have higher processing priority. It is a dispatching rule based on process time guiding.

## 3. Case Study

### 3.1 Existing Circumstance of Individual Case

The individual case of this study is a semiconductor wafer manufactory (W Company) lo-

cated in Taiwan's Hsinchu Science Park, which mainly carries on foundry orders entrusted by IC design corporations, the products include generic logic components, mixed mode components and high voltage components, it is applied to consumptive electronic products, displays, cell phones, digital cameras and relative peripheral products to computers. Its market characteristic only needs a big quantity and quick replacement, so clients always face the pressure of time-to-market, however, they don't want to set up huge stocks, so when good business conditions come, the clients need to make quick delivery because of this fast change of market, and they need to meet the fast demand of market, therefore the cycle time is paid much attention to. However, for the company operating, the use rate of machine should be increased if the profit needs to be increased, the production line shall be fully used to increase the quantity of output, so the release shall be increased frequently for increase of WIP, and reduce the probability of machine's idle for material, and increase the use rate of machines, the movement/output of foundry would increase accordingly, but the cycle time is extended.

The demands of company and clients are conflicting with each other, the electronic product market changes rapidly, the cycle time of company is relatively long, and sometimes on-time delivery cannot be made, so clients always place orders in advance in order to get goods on time, when the demand declines, clients asked for delayed delivery, so that the capacity of company is wasted on the products not to be delivered immediately, and stocks piled up as well as decline of turnover. But when the good business conditions rise, it would be too late to make deliveries that delay the business opportunities, clients' complaints become more and more, even some clients turn orders to other foundries that provide prompt deliveries though have higher prices. Therefore, W company is always thinking about how to shorten the cycle time and improve order deliveries while keeping the output and movement at a certain level. Comparing the production performance of W Company before improvement with that of fellow traders, the cycle time of other manufactories under high utilization is still better than that of the company. The cycle time of company under low utilization is not too bad, but when the utilization rate of productive capacity is increased, the quantity of output would be increased, and the WIP is increased rapidly as well as the cycle time is increased, so the order delivery would decline. The reason is that when the orders increase, excessive WIP would be inputted in order to increase the output, the excessive WIP makes the company be short of flexibility to cope with sudden demands of clients, even fail in meeting the due date, which results in the strong dissatisfaction of clients. Therefore, we know the bad due date is resulted from excessive WIP, reducing the level of WIP is the essential solution, but the insufficiency of WIP is liable to increase the idleness probability of machines, namely increase the probability of capacity idle/loss, and then the output would decline.

### 3.2 Analysis on Improvement Method for Cycle Time

We shall be aware of the factors influence the cycle time before improving the cycle time, there are two kinds of cycle time, Actual Cycle Time and Dynamic Cycle Time. The computing mode is as follows:

(1) Output time reduces wafer input time equals actual cycle time.
(2) Dynamic cycle time is the leading indicator of actual cycle time, its formulation is [WIP ÷ Movement].

The principle of improving cycle time is to reduce WIP and increase movement, but the movement and WIP are interdependent. Reducing the WIP level would increase the probability of capacity idle because B/N lacks WIP, thus the movement declines, and the output is decreased though the cycle time is improved, this is not what we want. On the other hand, to increase the movement, the most straightforward method is to increase the WIP level, so that the probability of capacity idle resulted from B/N's lack of WIP would be diminished, but the increase of WIP level makes the cycle time increase. Therefore, following two principles should be followed in order to improve the cycle time: (1) find out how to reduce WIP without reducing Movement; (2) increase Movement without increasing WIP. This study emphasizes the management of WIP, so the key would be how to reduce the WIP without reducing the movement.

### 3.3 Description of WIP SPC Method

Work-in-process is for avoiding some factors of manufactory which can hardly be handled, such as crash of computers, parameter setup and rework, they would influence the output of B/N, among which, the crash is the principal factor. The WIP level has a close relation with the variation of machine, the bigger variation is, the more WIP is required for protecting the bottleneck. However, the management of dispatching can reduce the impact of variation on the bottleneck, so that the WIP level can be reduced. The impact of dispatching management is very flexible, how big the impact would be depends on the management tool and efforts, it is hard to give an exact number. DBR dispatching of TOC proved effective to cycle time in many studies, however, the concept of TOP is assuming the manufactory has only one bottleneck, due to costly equipments, and considering the cost competition, current semiconductor manufactories purchase machines for each station just enough for setting up the capacity. Furthermore, the semiconductor process is complicated, and it has a lot of stations, usually there are almost one hundred stations. Take W Company, October 2007 as an example, as Table 1, although the genuine bottleneck is Thin Oxide/HTOX, the secondary B/N (if the use rate is greater than 90%, it would be regarded as secondary B/N) would have 14 stations, because the difference between the use rate of secondary B/N and that of

**Table 1.** High use rate equipment group

| No | Equipment | Jul-06 | | Aug-06 | | Sep-06 | | Oct-06 | | Nov-06 | | Dec-06 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Util. | Tools | Util. | Tools | Util. | Tools | Util. | Tools | Util. | Tools | Util. | Tools |
| **1** | **PECVD-SiH4** | **118.7%** | 7.2 | **104.9%** | 8.7 | **104.4%** | 9.2 | 98.8% | 9.2 | **103.7%** | 9.2 | **103.4%** | 9.2 |
| 2 | Lam4500/4520(SOGEB) | **105.2%** | 2.0 | **104.3%** | 2.0 | **102.5%** | 2.0 | 98.4% | 2.0 | **109.3%** | 2.0 | **103.0%** | 2.0 |
| 3 | Thin Oxide/HTOX | 97.1% | 35.0 | **100.7%** | 35.0 | **102.4%** | 35.0 | **105.3%** | 35.0 | **102.6%** | 35.0 | 99.3% | 35.0 |
| 4 | Oxide CMP(EBARA) | 100.0% | 1.0 | 100.0% | 1.0 | 100.0% | 1.0 | 100.0% | 1.0 | 100.0% | 1.0 | 100.0% | 1.0 |
| 5 | Metal Ctcher-Hitachi 308 | 100.0% | 3.0 | 100.0% | 3.0 | 100.0% | 3.0 | 100.0% | 3.0 | 100.0% | 3.0 | 100.0% | 3.0 |
| 6 | Metal Etcher-Hitachi 501 | 100.0% | 2.0 | 100.0% | 2.0 | 100.0% | 2.0 | 100.0% | 2.0 | 100.0% | 2.0 | 100.0% | 2.0 |
| 7 | Gate Oxide | 97.1% | 10.5 | 96.7% | 11.0 | 100.0% | 11.0 | **100.8%** | 11.0 | 98.4% | 11.0 | 96.5% | 11.0 |
| 8 | UTC | 91.6% | 7.0 | 95.5% | 7.0 | 98.8% | 7.0 | 99.7% | 7.0 | 96.8% | 7.0 | 94.6% | 7.0 |
| 9 | Mid Current Implanter | 89.9% | 9.5 | 94.7% | 9.5 | 98.6% | 9.5 | **100.2%** | 9.5 | 98.2% | 9.5 | 98.7% | 9.5 |
| 10 | Metal Etcher-W Plug EB | 100.0% | 8.0 | 89.9% | 8.5 | 97.9% | 9.0 | 99.3% | 9.0 | 99.6% | 9.0 | 98.8% | 9.0 |
| 11 | PECVD-SIN | 92.6% | 4.2 | 91.8% | 4.2 | 96.4% | 4.2 | 96.5% | 4.2 | 97.5% | 4.2 | 97.3% | 4.2 |
| 12 | Sputter | 88.9% | 13.0 | 85.1% | 13.0 | 94.2% | 13.0 | 97.1% | 13.0 | 97.3% | 13.0 | 96.3% | 13.0 |
| 13 | PECVD-SiH4&SiON&SiN | 99.2% | 17.0 | 92.5% | 18.5 | 94.0% | 19.0 | 90.3% | 19.0 | 95.1% | 19.0 | 96.7% | 19.0 |
| 14 | SAUSG | 85.6% | 10.0 | 86.8% | 10.0 | 93.6% | 10.0 | 95.9% | 10.0 | 97.4% | 10.0 | 95.6% | 10.0 |
| 15 | PRS | 87.1% | 11.0 | 88.9% | 11.0 | 89.6% | 11.0 | 91.7% | 11.0 | 93.7% | 11.0 | 91.4% | 11.0 |
| 16 | HDPCVD(PS) | 92.1% | 1.7 | 84.9% | 2.0 | 88.7% | 2.0 | 86.8% | 2.0 | 99.2% | 2.0 | 91.2% | 2.3 |
| 17 | TEL 858 | 93.1% | 21.0 | 85.8% | 21.0 | 88.1% | 21.0 | 90.4% | 21.0 | 85.9% | 21.0 | 89.1% | 21.0 |
| 18 | HDPCVD(STI) | 88.8% | 1.0 | 82.1% | 1.0 | 87.7% | 1.0 | 91.3% | 1.0 | 98.2% | 1.0 | 99.2% | 1.0 |
| 19 | High Current Implanter | 79.2% | 10.0 | 82.5% | 10.0 | 87.7% | 10.0 | 86.9% | 10.0 | 87.1% | 10.0 | 88.7% | 10.0 |
| 20 | NS | 81.5% | 3.0 | 82.7% | 3.0 | 87.1% | 3.0 | 91.1% | 3.0 | 92.8% | 3.0 | 96.2% | 3.0 |
| 21 | Asher | 82.7% | 23.6 | 86.7% | 23.6 | 85.5% | 23.6 | 89.1% | 23.6 | 94.7% | 23.6 | 90.4% | 23.6 |
| 22 | TEL DRM | 85.8% | 9.0 | 72.5% | 9.0 | 84.3% | 9.0 | 85.9% | 9.0 | 92.6% | 9.0 | 94.3% | 9.0 |
| 23 | BPSG Flow | 79.7% | 5.0 | 77.5% | 5.0 | 83.3% | 5.0 | 84.9% | 5.0 | 86.6% | 5.0 | 85.6% | 5.0 |
| 24 | Vacuum/SOG Baking | 81.5% | 11.0 | 79.8% | 11.0 | 82.9% | 11.0 | 83.4% | 11.0 | 86.5% | 11.0 | 85.5% | 11.0 |
| 25 | Mtal Etcher-DDPSM | 81.0% | 9.0 | 80.2% | 9.0 | 81.9% | 9.5 | 79.3% | 10.0 | 84.0% | 10.0 | 85.2% | 10.0 |
| 26 | RTP-Metal | 81.4% | 8.0 | 80.5% | 8.0 | 81.1% | 8.0 | 84.6% | 8.0 | 90.8% | 8.0 | 88.9% | 8.0 |
| 27 | Oxide CMP(Mirra Mesa) | 72.7% | 9.0 | 72.3% | 9.0 | 80.3% | 9.0 | 83.1% | 9.0 | 85.0% | 9.0 | 87.0% | 9.0 |
| 28 | Laser Mark | 74.0% | 3.0 | 76.0% | 3.0 | 78.2% | 3.0 | 80.1% | 3.0 | 78.9% | 3.0 | 79.5% | 3.0 |
| 29 | PETEOS | 68.8% | 11.0 | 76.8% | 11.0 | 77.5% | 11.0 | 81.8% | 11.0 | 86.2% | 11.0 | 81.6% | 11.0 |
| 30 | SOG Coater | 77.2% | 8.0 | 75.6% | 8.0 | 77.0% | 8.0 | 75.5% | 8.0 | 81.2% | 8.0 | 77.9% | 8.0 |
| 31 | OPRS(EKC) | 73.3% | 4.0 | 71.7% | 4.0 | 76.9% | 4.0 | 79.1% | 4.0 | 81.7% | 4.0 | 82.7% | 4.0 |
| 32 | W CMP | 77.8% | 8.0 | 78.9% | 8.0 | 76.6% | 8.0 | 77.5% | 8.0 | 87.1% | 8.0 | 90.6% | 8.0 |
| 33 | RE | 74.7% | 4.0 | 77.5% | 4.0 | 76.4% | 4.0 | 80.5% | 4.0 | 84.2% | 4.0 | 80.3% | 4.0 |
| 34 | OZ3000 | 85.1% | 6.0 | 79.7% | 6.0 | 76.3% | 6.0 | 69.3% | 6.0 | 67.8% | 6.0 | 68.5% | 6.0 |
| 35 | Alloy | 74.3% | 5.0 | 71.5% | 5.0 | 75.4% | 5.0 | 76.6% | 5.0 | 79.3% | 5.0 | 79.4% | 5.0 |
| 36 | WCVD | 73.3% | 12.0 | 71.7% | 12.0 | 75.4% | 12.0 | 76.8% | 12.0 | 79.0% | 12.0 | 79.4% | 12.0 |
| 37 | Wafer Scrubber | 72.0% | 21.0 | 74.1% | 21.0 | 73.9% | 21.0 | 77.9% | 21.0 | 82.8% | 21.0 | 80.0% | 21.0 |
| 38 | WCMP-Buffing | 74.8% | 7.0 | 76.1% | 7.0 | 73.8% | 7.0 | 74.7% | 7.0 | 83.9% | 7.0 | 87.1% | 7.0 |
| 39 | MOCVD | 72.5% | 5.0 | 74.3% | 5.0 | 72.3% | 5.0 | 73.0% | 5.0 | 81.4% | 5.0 | 83.9% | 5.0 |
| 40 | LamTCP9400/Alliancecha mber | 68.2% | 14.0 | 73.8% | 14.0 | 71.9% | 14.0 | 75.2% | 14.0 | 85.1% | 14.0 | 82.3% | 14.0 |

genuine bottleneck is less than 10%, the secondary B/N may become primary bottleneck as long as the variation of it is greater than 10%, so these 14 stations shall be brought under management.

This study suggests adopting a kind of progressive bottleneck and WIP management, it can be divided into 5 steps, the description is as follows: (1) Firstly, estimate reasonable WIP level based on present cycle time level; (2) Distribute WIP level to each machine group according to machine characteristics and utilization rate of productive capacity, and set standard WIP; (3) Set WIP control line based on SPC concept, carry out automated processing of WIP Balance behavior by computers; (4) Set monitoring mechanism, handle machine's variation, estimate and monitor the status of WIP, take remedial actions in time; (5) When the line balance is under control and B/N has no capacity loss, reduce the WIP level gradually, and repeat Step 1~5.

**Step 1: Determine primary WIP level**

According to Little's Law (average cycle time = average work-in-process ÷ output rate), presently the cycle time level is given, output is also determined, then WIP Level = (Cycle Time × Output).

**Step 2: Determine proper WIP Profile**

Rational WIP gross is determined, but if the WIP is at wrong place, that would only increase the cycle time. But how to determine proper distribution of WIP? Presently all semiconductor manufactories make decisions based on experience, for example, a manufactory's monthly output is 60,000 pcs, the average stage of products is 120, then STD Movement = 60,000 × 120/30days = 240,000. Whereas according to experience, different machine group has different output rate, provided that all products Gate Oxide Furnace have only one process step, and the output rate of Gate Oxide Furnace is 1.2, then Gate Oxide Furnace STD WIP = (STD Movement ÷ STD turn) = (60,000 × 1/30) ÷ 1.2 = 1,667 pcs, But presently the output rate 1.2 of Gate Oxide Furnace does not mean Table 1.2 is standard value, so STD WIP thereof is no more than empirical value, when manufactory's product mix changed, or production conditions changed, STD WIP studied out by this means would have sizable error, so comparatively objective STD WIP should be made.

To resolve this issue, we should start on the function of WIP, the function of WIP can be divided into two types, one of which is Running WIP, assuming there is a kind of ideal Fab, the machine definitely has no variation, so called no variation means the machine still needs PM, it would crash as usual, but PM and crash occur only when there is no need for running goods, once there is a need for running goods, the machine can provide capacity again, so that there would be no more redundant WIP piled in front of the B/N, which is to say Running WIP intends to reach the necessary minimal WIP level for output. The other one is

Waiting WIP which is for protecting the bottleneck, realistic manufactories always have variation, machines often crash or have PM when capacity is needed, so extra WIP is required for such status, and avoid bottleneck capacity loss resulted from machine's variation.

**(1) How to determine Running WIP?**

Running WIP means work-in-process being produced in machines. Assuming there is an ideal manufactory, machines definitely have no variation, and production can be carried out before products reach the machine, so there is no need for extra WIP to cope with variation, so Running WIP is in relation to Process Time. For example, batch type machine furnace needs 6 hours for one run, etching machine needs only 1 hour, the probability of WIP at Furnace is 6 times of at etching machine, and the proportion of Running WIP is 6 times, too. The proportion of Running to overall WIP is in relation to X-ratio, take current X-ratio 3.8 as an example, Running WIP accounts for about 40% of overall WIP.

Assume that the quantity of machine group is $r$, then the Run $WIP_i$ of $i$th machine group is:

$$\text{Run WIP}_i = (\text{Run WIP Level} \times \text{Process Time}_i) \div \text{Theoretical Cycle Time}.$$

**(2) How to determine Waiting WIP?**

Waiting WIP means WIP to be produced in front of machine, it is for protecting the bottleneck, and avoiding bottleneck capacity loss resulted from machine's variation, but when non-B/N has severe crash, temporary bottleneck may occur. If the utilization of non-B/N is very low, temporary bottleneck hasn't occur yet though some machines crashed, so remaining capacity (non-bottleneck capacity reduces bottleneck capacity) also has the function of protecting bottleneck. Therefore, STD Waiting WIP in front of the machine can be measured by machine's remaining capacity viewpoint. The impact of machine crash on downstream bottleneck = (probability × incidence). Assume that the foundry has $r$ machine groups, and each machine group has $n$ machines, then STD Wait $WIP_i$ of $i$th machine group is:

$$[\text{Wait WIP Level} \times \sum_{j=1}^{n} C_j^n (1-Avail)^j \times Avauk^{(n-j)} \times Max(0, \frac{n \times Util}{n-j} - 1) \times Group\ Cacity_t] \div$$
$$[\sum_{i=4}^{r} (\sum_{j=1}^{n} C_j^n (1-Avail^{(n-j)} \times Max(0, \frac{n \times Util}{n-j} - 1) \times Group\ \ Capacity_i)]$$

When STD Running $WIP_i$ and STD Waiting $WIP_i$ of $i$th machine group are determined, STD $WIP_i$ of $i$th machine group = STD Running $WIP_i$ + STD Waiting $WIP_i$.

**Example:** Assume that there are only two machine groups in the foundry, Gate Oxide furnace tube and I-line Stepper, the whole process step only has once Gate oxide

and twice I-line, total three steps. The process time of Gate oxide is 6 hours, while the process time of I-line is 44 minutes. In September 2007, the overall WIP 5,000 pcs, there into Running WIP 2,000, Waiting WIP 3,000. There were 11 Gate Oxide furnace tube machines, the utilization rate of machines was 80%, Avail was 88%, group capacity was 10,000 pcs; there were totally 10 I-line stepper machines, the utilization rate of machines was 99%, Avail was 92%, the group capacity was 12,000 pcs.

Running WIP is calculated as follows:

Running WIP of Gate oxide machine is: $(2{,}000 \times 6) \div (6 + (44/60) \times 2) = 1{,}607$;

Running WIP of I-line machine is: $2{,}000 \times ((44/60) \times 2) \div (6 + (44/60) \times 2) = 393$.

Waiting WIP is calculated as follows:

Gate Oxide EQP variability impact is:

$$(C_1^{11} * (1-0.88)^1 * 0.88^{(11-1)} * (11 * 80\%/(11-1) - 100\%) + \cdots + C_{11}^{11} * (1-0.88)^{11} * 0.88^{(11-11)} * (11 * 80\%/(11-11) - 100\%)) * 10{,}000 = 2.1 * 10{,}000 = 21{,}000$$

I-line Stepper EQP variability impact is:

$$(C_1^{10} * (1-0.92)^1 * 0.92^{(10-1)} * (10 * 99\%/(10-1) - 100\%) + \cdots + C_{10}^{10} * (1-0.92)^{10} * 0.92^{(10-10)} * (10 * 99\%/(10-10) - 100\%)) * 12{,}000 = 9.1 * 12{,}000 = 109{,}200$$

STD Waiting WIP of Gate Oxide machine = $3{,}000 \times 21{,}000 \div (21{,}000 + 109{,}200) = 484$;

STD Waiting WIP of I-line Stepper machine = $3{,}000 \times 109{,}200 \div (21{,}000 + 109{,}200) = 2{,}516$.

The STD WIP of each machine group is calculated as follows:

STD WIP of Gate Oxide machine = STD Running WIP + STD Waiting WIP
= (1,607 + 484) = 2,091;

STD WIP of I-line machine = STD Running WIP + STD Waiting WIP
= (393 + 2,516) = 2,909.

The STD WIP of each machine group is determined, but STD WIP of machine group only indicates which place shall have how many WIP, it is not applicable for production control due to the process reflux of semiconductor. A machine group, for example, exposure machine I-line, it may be used for initial step, also may be used for rear center section of process, so we know I-line STD WIP is insufficient, but we don't know which section in

the process lacks I-line WIP. As mentioned above, we need to make STD WIP Profile based on process viewpoint in order to adjust foundry's production sequence and speed.

Generally speaking, the work flow of manufactories mainly uses flow chart of process viewpoint, so-called flow chart of process viewpoint refers to giving priority to products and describing the process sequence. In wafer manufactories, due to long manufacturing procedure, there always be 300~500 steps, it would be very complicated in case analyzing every process step, the Theory of Constraints (TOC) (Goldratt, 1990a/b; Goldratt *et al*., 2000; Goldratt, 2006) also emphasize that only loss of B/N or machine capacity can influence the gross output, so the analysis paper of wafer manufactories combine several steps into one step, which is called Stage. For example, KSR (Key Stage Report) is one of the most important production reports in foundries, so-called Stage usually means a small module of process, so mostly only one step needs to be processed on so-called constraint machine in one Stage, other steps are not important like measurement. But usually the quantity of stage of one product is about 100~150, and different products name Stage in different ways, for example, the position of Stage of DPSN in Generic Logic is different from that in HV, furthermore, it is hard to find out the focal point through more than a hundred stages under control, so the stage must be reintegrated. We divide all product process into 10 sectors, S1~S10 represents 10 sectors of stage respectively, thus there would be no homonymy and confusions, and it is easy to see the distribution of WIP, so for WIP Profile, we decide that using Sector as the unit is suitable for the study of mode. Other than using Sector as the unit, this study made following hypotheses: (1) Form of production is order production; (2) System constraint is machine capacity, there is no manpower factor and lack of material; (3) Assume that the constraint is the production capacity of foundry, there are adequate orders, the constraint is not the market; (4) Except crash, machine would not stop because of other factors; (5) overall WIP of foundry is given.

We want to construct an ideal WIP Profile distribution taking process as viewpoint, assume that the foundry has *i* types of product, each type is divided into *j* sectors. Then according to Little's Law: WIP = (CT × Output).

The *j*th sector of *i*th type product STD $WIP_{ij}$ = $CT_{ij}$ × $Output_{ij}$ = X-$ratio_{ij}$ × Theoretical $CT_{ij}$ × $Output_{ij}$ among which, X-$ratio_{ij}$ = (Full Process CT ÷ Theoretical CT) of Part *i*.

Adjust STD X-ratio of each sector according to waiting theory, and keep $\sum_{j=1}^{n} X_{ij} \times TCT_{ij} = CT\ Target_i$;

$$\text{The } j\text{th sector STD } WIP_j = \sum_{i=10}^{n} Output_i \times X_{ij} \times TCT_{ij}$$

Wait Time = [WIP ÷ Capacity × Process Time];

(Wait Time ÷ Process Time) = X-Ratio = (WIP ÷ Capacity) = WIP ÷ (Tool Qty × Batch Size);

e.g.: [GateOx 11 set WIP 2,000pcs, X-Ratio] = 2,000 ÷ (11 × 150) = 1.21 (as Table 2).

**Table 2.** STD WIP and Target T/R

| Sector | STD WIP | | | | | | Target T/R | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **TTL** | % | D | P | E | T | **Avg.** | D | P | E | T |
| S1 | 6,210 | 8% | 4,967 | 1,146 | 97 | | 2.0 | 1.7 | 4.4 | 6.0 | - |
| S2 | 13,868 | 18% | 10,529 | 2,018 | 1,073 | 248 | 2.3 | 1.9 | 3.7 | 5.3 | 5.2 |
| S3 | 7,757 | 10% | 4,685 | 1,212 | 1,339 | 521 | 2.3 | 1.7 | 3.5 | 4.6 | 3.3 |
| S4 | 18,987 | 25% | 7,160 | 4,105 | 2,650 | 5,072 | 3.0 | 2.5 | 3.7 | 5.4 | 2.5 |
| S5 | 8,968 | 12% | | 1,214 | 2,309 | 5,445 | 3.5 | - | 3.3 | 3.9 | 3.4 |
| S6 | 8,623 | 11% | | 1,217 | 2,253 | 5,154 | 3.0 | - | 2.8 | 3.2 | 3.0 |
| S7 | 3,546 | 5% | | 806 | 363 | 2,377 | 3.8 | - | 2.3 | 5.8 | 3.9 |
| S8 | 2,707 | 4% | | 417 | 912 | 1,378 | 4.1 | - | 2.4 | 4.0 | 4.5 |
| S9 | 3,756 | 5% | | 526 | 1,195 | 2,035 | 3.3 | - | 4.3 | 4.0 | 2.8 |
| S10 | 1,571 | 2% | | | 1,571 | | 1.8 | - | - | 1.8 | - |
| **TTL** | **75,993** | **100%** | 27,343 | 12,659 | 13,761 | 22,231 | **2.8** | **2.0** | **3.5** | **4.1** | **3.2** |

**Step 3: Set up control chart, field dispatching control release avoid bottleneck and Profile deviation**

When the formulation of STD WIP is determined, we divide the product process into 10

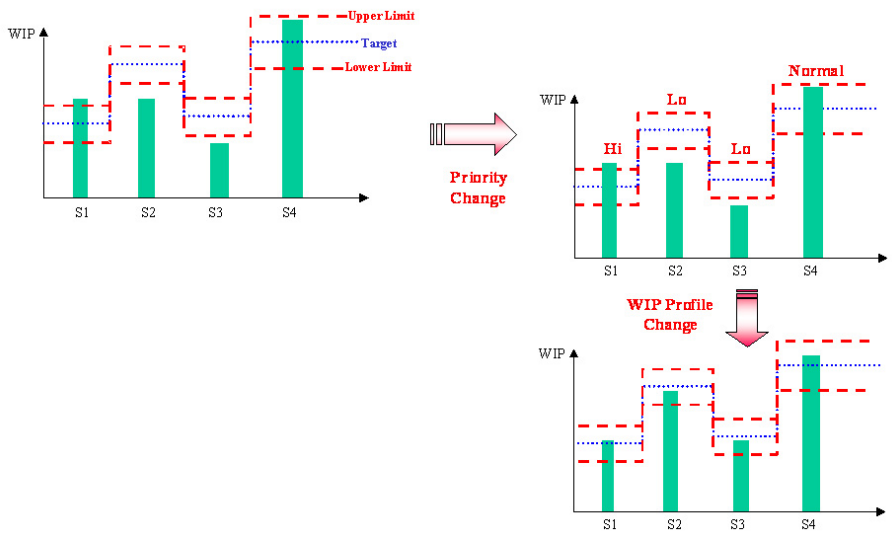



**Figure 1.** STD WIP SPC Conceptual graph

sectors, STD WIP of each sector can be derived from formula, and STD WIP of each machine group in each sector can be worked out, then we can use the control chart principle to determine the control limit of WIP for each sector, if the WIP exceeds the control limit, start up remedial measures (as Table 3).

**Table 3.** STD WIP distribution and STD WIP Upper/Lower Limit

| Sector | STD WIP | | | | | | Target T/R | | | | | Low Limit | | Upper Limit | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **TTL** | % | D | P | E | T | **Avg.** | D | P | E | T | | | | |
| S1 | 6,210 | 8% | 4,967 | 1,146 | 97 | | 2.0 | 1.7 | 4.4 | 6.0 | - | 5,589 | -10% | 6,831 | +10% |
| S2 | 13,868 | 18% | 10,529 | 2,018 | 1,073 | 248 | 2.3 | 1.9 | 3.7 | 5.3 | 5.2 | 12,481 | -10% | 15,255 | +10% |
| S3 | 7,757 | 10% | 4,685 | 1,212 | 1,339 | 521 | 2.3 | 1.7 | 3.5 | 4.6 | 3.3 | 6,982 | -10% | 8,533 | +10% |
| S4 | 18,987 | 25% | 7,160 | 4,105 | 2,650 | 5,072 | 3.0 | 2.5 | 3.7 | 5.4 | 2.5 | 17,088 | -10% | 20,885 | +10% |
| S5 | 8,968 | 12% | | 1,214 | 2,309 | 5,445 | 3.5 | - | 3.3 | 3.9 | 3.4 | 8,071 | -10% | 9,865 | +10% |
| S6 | 8,623 | 11% | | 1,217 | 2,253 | 5,154 | 3.0 | - | 2.8 | 3.2 | 3.0 | 7,761 | -10% | 9,486 | +10% |
| S7 | 3,546 | 5% | | 806 | 363 | 2,377 | 3.8 | - | 2.3 | 5.8 | 3.9 | 2,482 | -30% | 4,610 | +30% |
| S8 | 2,707 | 4% | | 417 | 912 | 1,378 | 4.1 | - | 2.4 | 4.0 | 4.5 | 1,895 | -30% | 3,519 | +30% |
| S9 | 3,756 | 5% | | 526 | 1,195 | 2,035 | 3.3 | - | 4.3 | 4.0 | 2.8 | 2,629 | -30% | 4,883 | +30% |
| S10 | 1,571 | 2% | | | 1,571 | | 1.8 | - | - | 1.8 | - | 1,100 | -30% | 2,042 | +30% |
| **TTL** | **75,993** | **100%** | 27,343 | 12,659 | 13,761 | 22,231 | **2.8** | **2.0** | **3.5** | **4.1** | **3.2** | | | | |

**Dispatching mode:** DBR thinks non-B/N has only to match B/N scheduling, usually FIFO is adopted, but when B/N seems lacking material, give process priority to parts which would cause bottleneck filled short.

According to Figure 1, a dispatching principle is set as follows:

(1) Set $S_n$ high priority, if WIP of $S_n$ over upper limit;

(2) Set $S_{n-1}$ high priority, if WIP of $S_n$ below lower limit;

(3) If $S_n$ below lower limit and $S_{n-1}$ over upper limit, set $S_{n-1}$ High Priority lot double;

(4) If consecutive Sectors (ex: $S_n$ an$_d$ $S_{n+1}$) below lower limit, upside priority forward and quantity of upside priority Sectors = below lower limit Sectors.

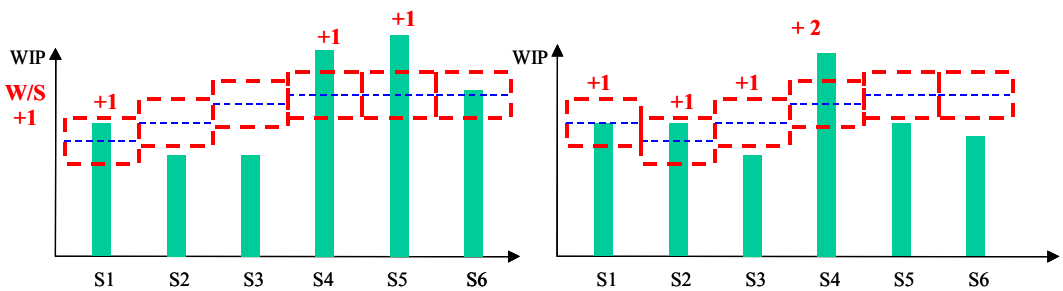
According to above principle, design dispatching rules the computers can recognize, as Figure 2 and Table 4.

**Step 4: Monitor bottleneck deviation and take remedial action**

Besides monitoring control system, we need to know what impact “Murphy” would exert on us and what effect next remedial action would bring, we need to build a prediction

**Table 4.** Dispatching rules point table

| Sector | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | Rule Discription |
|---|---|---|---|---|---|---|---|---|---|---|---|
| WIP | N | N | L | H | L | L | N | N | N | N | |
| Init. Score | 0 | +1 | 0 | +2 | +1 | 0 | 0 | 0 | 0 | 0 | See Dispatchin Rule |
| Qty Gap | 100 | 500 | -1,000 | 3,000 | -1,000 | -2,000 | 0 | 0 | 0 | 0 | Qty Gap = Act WIP-STD WIP |
| Gap Accu. | -400 | -500 | -1,000 | 0 | -3,000 | -2,000 | 0 | 0 | 0 | 0 | Gap $Accu_{-n}$ = Qty $Gap_n$ + Gap $Accu_{-n+1}$ |
| Gap Score | +1 | | | | | | | | | | If Gap-Accu. < & Qty Gap > 0 & Init. Score = 0, Gap Scroe = +1 |
| Score | +1 | +1 | 0 | +2 | +1 | 0 | 0 | 0 | 0 | 0 | Score = Init. Score + Gap Score |




Note: +1 means 30% WIP upside priority to (2, 20), W/S +1 means more wafer start
+2 means 60% WIP upside priority to (2, 20)

**Figure 2.** Schematic diagram of dispatching rules

system. Use an analytical tool, Utilization FCST System (spreadsheet mode, as Table 5) to know (FCST) position of B/N in one week or one month, take remedial measures and predict the effect of remedial measures. Batch size: bigger process batch of B/N is better, so that the bottleneck doesn't need to setup constantly, and the capacity loss can be decreased. Non-B/N had better carry out small batch process, because non-bottleneck has remaining capacity, even if waste some setup that would not affect the whole, and small batch process can shorten the cycle time effectively. Impact of reducing crash on Profile: use the Buffer Management of TOC, monitor whether the work at B/N is carried out prior to the preset time or not, if yes, the work must be done faster or machine allocated to avoid losing capacity due to bottleneck in short supply.

Monitor management: we can know which material has not yet arrived through the bottleneck resource usage buffer management, but we cannot know in which stations the material is delayed, so it is necessary to carry out monitor management for important non-bottleneck resource (key machine). Bottleneck resources which provide less protection for capacity or machines which have higher crash rate shall be regarded as key machine, judge whether the

key machine brings bottleneck (abnormity of work-in-process), and find out causes and take remedial actions (machine allocation).

**Table 5.** Utilization FCST

| EQP. Group | D01 | D02 | D03 | D04 | D05 | D06 | D07 |
|---|---|---|---|---|---|---|---|
| High Temp | **102.6%** | 72.9% | 83.6% | **110.2%** | **136.5%** | **185.6%** | **266.3%** |
| High Current Implanter | 71.5% | 68.4% | 82.2% | 95.0% | **102.1%** | **121.0%** | **146.9%** |
| Mid Current Implanter | 9.25% | 98.0% | **118.4%** | **145.0%** | **187.3%** | **237.9%** | **308.6%** |
| SIN | 90.3% | 92.8% | 76.1% | 61.0% | 96.2% | **129.1%** | **188.4%** |
| NS | **108.5%** | 56.2% | 61.3% | **100.2%** | 95.0% | 80.6% | 74.5% |
| Gate Oxide | 87.7% | 83.1% | 99.3% | 85.2% | 84.9% | 70.3% | 85.6% |
| D-POLY | 96.7% | 68.3% | 86.7% | **111.1%** | **103.7%** | 91.3% | 75.7% |
| Thin Oxide | **115.9%** | 91.2% | 65.3% | 76.3% | 86.6% | **112.6%** | **129.1%** |
| HTO | 65.5% | 50.7% | 65.5% | 77.9% | 55.6% | 67.0% | 69.6% |
| ANNL | 79.7% | **101.2%** | **104.3%** | **110.7%** | **123.1%** | **145.4%** | **175.7%** |
| **BPSG FLOW + S/D密化** | 76.7% | 68.6% | 57.3% | 46.7% | 63.3% | 59.0% | 67.1% |
| **ALLOY(AL9)** | 62.2% | 80.0% | 95.9% | 86.9% | 77.8% | 83.8% | 84.6% |
| ALLOY(Baking + Curing) | 70.4% | 83.8% | 72.5% | 95.4% | 83.4% | 95.7% | 94.4% |
| BPSG(DSABP) | 87.2% | 67.6% | 59.6% | 46.4% | 61.6% | 60.8% | 61.9% |
| SIH4 | 99.8% | **114.9%** | **128.9%** | **148.3%** | **178.0%** | **205.7%** | **235.6%** |
| Sputter(non_mocvd, non_ms) | 87.9% | 69.8% | 83.3% | 83.5% | 83.1% | 85.9% | 90.0% |
| Sputter(MOCVD) | 92.7% | 77.8% | 71.3% | 87.2% | 74.8% | 77.2% | 79.5% |
| Sputter(AI-MS) | 57.0% | 97.3% | 68.9% | 80.8% | 96.3% | 74.4% | 74.1% |
| MCVD | 87.2% | 91.6% | 86.8% | 93.7% | 89.6% | 94.0% | 88.4% |

**Step 5: Reduce WIP Level gradually**

The cycle time improvement is a time continuing process, when above steps can be performed stably and bottleneck has no capacity loss, reduce more WIP level. For example, a foundry's monthly output 60,000 pcs, average stage number of each product is 120, present output rate is 3.0, cycle time is 40 days, STD WIP = 60,000 × 40 ÷ 30 = 80,000, STD WIP of each station is determined, so it is easy to know the problems and make improvement accordingly, machines which were liable to stack WIP originally would be improved, we are confident to reduce WIP by 5%, STD WIP = 80,000 × 95% = 76,000, here the cycle time target value changed into (76,000 ÷ 60,000 × 30) = 38 days, as long as we control the variation of machine group, repeat above steps, STD WIP can be reduced gradually, repeat above steps.

# 4. Demonstration of WIP Statistical Process Control's Effect

## 4.1 Analysis and Comparison of Production Data

For foundries want to increase the competitive advantage of "quick due date and on-time delivery", this study starts on the control and management of WIP, firstly determines STD WIP of each sector, and then uses SPC, when WIP exceeds control limit, we take action plan to make WIP resume balance without fear of B/N loss and stack of remaining WIP, when WIP can be controlled reasonably, reduce the WIP level gradually, and the cycle time would be improved by slow degrees (as Table 6).

**Table 6.** Production data before and after improvement

| Performance indices | Before improvement (May-06~Jul-06) | After improvement (Aug-06~Oct-06) |
|---|---|---|
| Per Layer Cycle time (Days/L) | 1.84 | 1.60 |
| Wafer out per Month (pcs) | 54,500 | 61,400 |
| Average WIP (pcs) | 79,400 | 83,175 |
| CLIP (%) | 92.5% | 98.4% |
| Daily Movement | 208,440 | 240,278 |
| Stepper Utilization | 90.2% | 97.8% |

## 4.2 Effectiveness Demonstration

In order to demonstrate new WIP management means is effective on improvement of cycle time, we adopt testing of hypothesis to demonstrate the result. May-06~Jul-06 (total 92 days) use outdated production management mode ($\mu_1$= 1.84, $\sigma^2$ = 0.15), Aug-06~Oct-06 adopt new management model (WIP SPC, $\mu_2$ = 1.60, $\sigma^2$ = 0.02), whether both cycle times have remarkable difference or not?

**Table 7.** Testing of hypothesis of cycle time

| Cycle time | | May~Jul | Aug~Oct |
|---|---|---|---|
| Sample number | | 92 | 92 |
| Sample average | | $\mu_1$ = 1.84 | $\mu_2$ = 1.60 |
| Variance ($\sigma^2$) | | 0.15 | 0.02 |
| Tested statistic (Z) | | 7.01 | |
| $H_0$: $\mu_1$ <= $\mu_2$ | Throw aside field | Z > 1.65 | |
| $H_1$: $\mu_1$ > $\mu_2$ | $\alpha$ = 5% | Reject H0 | |

According to Table 7, after used new WIP statistic process management model (WIP SPC), the cycle time has notable improvement, the confidence degree is greater than 95%.

### 4.3 Other Benefit

Besides the production index is improved, the production line supervisor's working load is improved, too. Before admitting STD WIP SPC, the production line supervisor must pay attention to the output line in order to reach the due date (Customer Line Item Performance, CLIP) and (Customer Volume performance, CVP), increase the priority of comparatively behindhand products, such behavior causes destruction of line balance. Additionally, the line balance must be aligned for Movement, two behaviors and dispatching for production line, besides production line supervisor exhausted from running, sometimes he needs to take care the output line, and sometimes the line balance, and spot operating personnel always have no idea with dispatching changed too frequently, as time passes they overtly agree but covertly oppose the dispatching instruction from production line supervisor, that damages the prestige of supervisors. After STD WIP SPC admitted, the production line supervisor only needs to pay attention to the output line and due date, the line balancing problem is adjusted by STD WIP SPC automatically, operating personnel only need to follow the priority operation, so that the production line supervisor's working load is lightened, and he can spend much time on other production indexes.

## 5. Conclusions

For foundries want to increase the competitive advantage of quick due date and on time delivery, this study adopts one of two great orientations, aiming at how to reduce WIP without influencing output. According to real production data, it is evident that WIP SPC can reduce the cycle time and increase product delivery effectively. As Figure 3, after improvement (Jul-06~Oct-06), even if WIP and Movement are increased, the cycle time is still shorter than that of before improvement, the average could be kept at about 1.6 day/Layer.

As Figure 4, after improvement (Jul-06~Oct-06), even if the output and utilization are increased, but CLIP (Customer Line Item Performance) is still increased from 95% to 98%. As for determination of STD WIP in the course of study, the whole foundry is divided into 10 sectors in order for convenience, in fact, if it is permitted by the resource, we suggest using Stage as the unit of WIP SPC, so that Profile of fine WIP can be considered more effectively. In addition, when determine STD WIP of each machine group, there are some factors exert influence on WIP, due to the focal point of this study is not the determination of STD WIP, factors which can hardly be measured are neglected, such as:

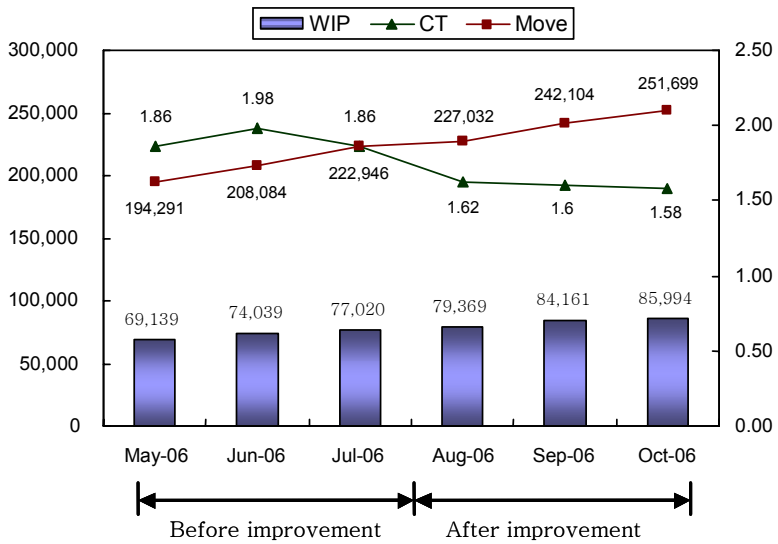



**Figure 3.** Correlation diagram of WIP and cycle time before and after improvement

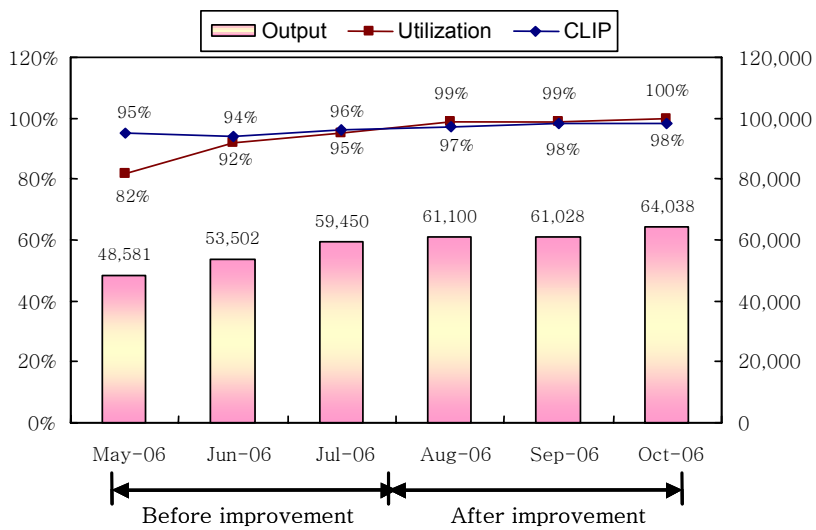



**Figure 4.** Correlation diagram of utilization rate and CLIP before and after improvement

(1) Recipe match dispatching (Furnace/CS): Chemical Station is for cleaning before entering the furnace tube, different furnace tube recipes need to be collocated with different chemical station recipes, if lot of two batches of different furnace tube recipe reaches the chemical station, the chemical station only can Run next furnace tube for lot of Run, every order for lot shall be waited, so there would be some extra WIP in chemical station, and STD WIP must be higher.

(2) Photo: Photo process would have photo phenomena in Critical layer, for example, one lot uses machine 1A-I200 at process P1, when reaches next key process contact, only 1A-I200 can be applied. If 1A-I200 crashes or other lot needs Run at this point, even if other machines are idle, this lot cannot be run, so there would be some extra WIP of Photo, and STD WIP should be higher.

How to make more precise STD WIP considering above circumstances can be regarded as the direction of future studies.

## References

1. Akcah, Kazunori Nemoto and Reha Uzsoy(2001), "Cycle-time improvements for photo-lithography process in semiconductor manufacturing," *IIEEE Transactions on Semiconductor Manufacturing*, Vol. 14, No. 1, pp. 48-56.
2. Chen, S. H.(2006), "fluidics of IC manufacturing maintaining work-in-process spread around workstation uniformly," master's thesis, Tung-Hai University, Taiwan.
3. Glassey C. R. and Resende, M. G. C.(1988a), "Closed-loop Job Release Control for VLSI Circuit Manufacturing," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 1, No. 1, pp. 36-46.
4. Glassey, C. R. and M. G. C. Resende(1988b), "A Scheduling Rule for Job Release in Semiconductor Fabrication," *Operations Research Letters*, Vol. 7, No. 5, pp. 213-217.
5. Goldratt, Eliyahu M.(1990a), "The Theory of Constraints," The North River Press.
6. Goldratt, Eliyahu M.(1990b), "What is the thing called theory of constraints and how should it be implemented," North River Press.
7. Goldratt, Eliyahu M., Eli schragenheim, and Carol A. Ptak(2000), "Necessary but not sufficient," The North River Press.
8. Goldratt, Eliyahu M.(2006), "The Strategy and Tactic trees-Consumer Goods-Viable Vision implementations," TOC Insights 2006.
9. Hsu, F. N.(2007), "Flow control design of IC manufacturing accelerating wafer flow to bottleneck zone," master's thesis, Tung-Hai University, Taiwan.
10. Huang, C. L.(1998), "analysis on bottleneck shifting and research on its management game," master's thesis, Department of Industrial Engineering and Management, National Chiao-Tung University, Taiwan.
11. Hung, Y. F. and R. C. Leachman(1996), "A production planning methodology for semiconductor manufacturing based on interactive simulation and linear programming calculation," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 9, No. 2, pp. 257-269.
12. Lawton, J. W., Drake, A., Henderson, R., Wein, L. M., Whitney, R., and Zuanich, D.(1990),

"Workload Regulating Wafer Release in a GaAs Fab Facility," *IEEE Int'l Semiconductor Manufacturing Science Symposium*, pp. 33-88.

13. Leachman, Robert. C. and David A. Hodges(1996), "Benchmarking semiconductor manufacturing," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 9, No. 2, pp. 158 -169.
14. Levitt, M. E. and J. A. Abraham(1990), "Just-In-Time Methods for Semiconductor Manufacturing," *IEEE/SEMI Advanced Semiconductor Manufacturing Conference*, pp. 3-9.
15. Lou, S. and P. W. Kager(1989), "A Robust Production Control Policy for VLSI Wafer Fabrication," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 2, No. 4, pp. 159 -164.
16. Lu, J. J.(2004), "Release and dispatching technology of IC manufacturing oriented production plan," master's thesis, Tung-Hai University, Taiwan.
17. Malmstrom, C.(1997), "Though Love: Real-time Planning and Scheduling at Philips Semiconductor," *Manufacturing System*, pp. 76-78.
18. Miller, D. J.(1990), "Simulation of a semiconductor manufacturing line," *Communication of The ACM*, Vol. 33, No. 10, pp. 99-109.
19. Spearman, M. L., David L. woodruff, and Wallace J. Hopp(1990), "CONWIP: A Pull Alternative to Kanban," *International Journal of Production Research*, Vol. 28, No. 5, pp. 879-894.
20. Tu, Y. M.(1998), "work-in-process management mode of wafer manufactory," master's thesis, Department of Industrial Engineering and Management, National Chiao-Tung University, Taiwan.
21. Uzsoy, R., C. Y. Lee and L. A. Martin-Vega(1992), "A review of production planning and scheduling models in the semiconductor industry. Part I: system characteristics, performance evaluation and production planning," *IIE Transaction*, Vol. 24, No. 4, pp. 47 -60.
22. Uzsoy, R., C. Y. Lee, and L. A. Martin-Vega(1994), "A review of production planning and scheduling models in the semiconductor industry. Part II: shop-floor control," *IIE Transaction*, Vol. 26, No. 5, pp. 44-55.
23. Wein, L. M.(1988), "Scheduling Semiconductor Wafer Fabrication," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 1, No. 3, pp. 115-130.
24. Wu, H. H. and Li, R. K.(2003), "Drum-Buffer-Rope Scheduling and management technology," Chuan-Hua Technology Books, Taiwan.