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Reliability of Multiple Oxides Integrated with thin $HfSiO_x$ gate Dielectric on Thick SiO_2 Layers

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Abstract: Reliability and performance in metal gate/high-k device with multiple gate dielectrics were investigated. MOSFETs with a thin $HfSiO_x$ layer on a thermal SiO_2 dielectric as gate dielectrics exhibit excellent mobility and low interface trap density. However, the distribution of threshold voltages of $HfSiO_x/SiO_2$ stack devices were wider than those of SiO_2 and $HfSiO_x$ single layer devices due to the penetration of Hf and/or intermixing of $HfSiO_x$ with underlying SiO_2. The results of TZDB and SILC characteristics suggested that a certain portion of $HfSiO_x$ layer reacted with the underlying thick SiO_2 layer, which in turn affected the reliability characteristics.

Keywords: multiple oxide, $HfSiO_x/SiO_2$ stack gate, thick oxide reliability

1. Introduction

Hafnium based high-k dielectrics have been proposed to replace a thermally grown-silicon dioxide (SiO_2) due to their high dielectric constant (high-k), large energy bandgap, high thermal stability, and process compatibility.[1-6] In conjunction with high-k dielectric study, dual metal electrode process rather than poly-Si gate is essential for further equivalent oxide thickness (EOT) lowering because of no poly depletion and boron penetration into poly-Si.[7-9] Recently, CMOS device with gate metal and high-k gate dielectric has successfully demonstrated for low standby power (LSTP) application. Reliability studies for various high-k gate dielectrics have performed at very thin EOT ranges.[10] Unlikely the devices with SiO_2 dielectric, bulk charge trapping in high-k layer has well known to be a dominant mechanism for threshold voltage instability and lower activation energy. In a real semiconductor chip circuit, however, gate dielectrics with different thicknesses should be integrated within a chip.[11] For instance, an internal circuit needs the thinnest EOT for improving performance but an I/O circuit needs a thicker EOT for maintaining its functionality under high external applied voltage. The reliability of multiple oxides including high-k dielectric seriously degrades because metallic impurity penetration leads additional defects in dielectrics, which in turn deteriorate device characteristics such as threshold voltage, gate leakage current, and dielectric reliability. However, in our knowledge, no reports have been addressed for the reliability of high-k based multiple dielectrics.

In this work, the reliability and performance of gate dielectric systems which have a high-k gate dielectric layer (~3nm) deposited on 2-4nm thick SiO_2 films are examined for multiple oxide application.

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Table 1. Multiple oxides stacks used in this study.

Sample	A	B	C	D
Electrode	$HfSi_x$	$HfSi_x$	$HfSi_x$	TiN
HfSiOx (nm)	3	3	3	0
SiO_2 (nm)	0	2	4	6
EOT (nm)	1.4	2.7	4.6	6.0
V_{fb} (V)	-0.71	-0.71	-0.72	-0.70

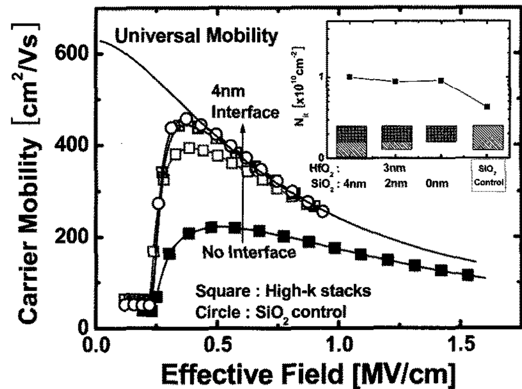

Fig. 1. Carrier mobility of various structures. N_{it} in inlet is measured from nMOSFET at 100 kHz by using charge pumping method. The arrow means the thickness increase of SiO_2 layer in 3 types of high-k stacks.

2. Experiment

To fabricate the multiple oxide structures, after a standard cleaning of a p-type (100) silicon wafer, thin $HfSiO_x$ layer as high-k dielectric was deposited on SiO_2 layers with different thicknesses. SiO_2 films were grown using in-situ steam growth process and $HfSiO_x$ was deposited using atomic layer deposition (ALD) system. Subsequent post-deposition annealing was performed at 700°C for 1min in NH_3 ambient. After then, ALD-TiN (10nm) or MOCVD-$HfSi_x$ (10nm) electrode was deposited followed by 100nm poly-Si layer as a stack electrode. The samples used in this study were summarized in Table 1. After gate stack formation, conventional CMOS flow with a spike annealing at 10750°C was carried out to complete transistor fabricate.

Electrical characterization was performed using a HP 4284A impedance/gain phase analyzer and a HP 4156A semiconductor parameter analyzer. EOT was calculated using NCSU CVC program based on capacitance-voltage (C-V) curves measured at 100 kHz. Charge pumping measurements were also done to evaluate interface state density.

3. Results and discussion

Figure 1 shows the calculated carrier mobility for all stack structures to see how gate stacks with different thicknesses of SiO_2 layers affect the carrier mobility. The $HfSiO_x$ single layer gate dielectric sample shows the lowest mobility in all electric field regime. The carrier mobility increases with underlying SiO_2 thickness. Eventually, the mobility of $HfSiO_x$(3nm)/SiO_2(4nm) sample is almost identical to that of control SiO_2 device. In addition, there is no degradation of high field mobility for $HfSiO_x$(3nm)/SiO_2(2nm) sample even though there is low field mobility degradation due to remote charge scattering. For the thinnest sample which shows mobility degradation in high-field regime, its surface or morphology must be rougher than those of other samples with thicker interfacial oxides.

To evaluate the Si-SiO_2 interfacial state of each device, the interface state density (N_{it}) was measured using charge pumping method (inset of Fig. 1).[12] The values of N_{it} with 3nm $HfSiO_x$ devices are sufficiently low (~10^{10} cm^{-2}) and similar each other. From these results, it can be speculated that thin $HfSiO_x$ deposited on multiple oxide region has no affection to the quality of thick oxide such as interface state density.

Figure 2 shows the time zero dielectric breakdown (TZDB) characteristics. Regarding the breakdown voltage (BV), all of the structures show tight distribution of BV and negligible area dependence, indicating that the TZDB is an intrinsic characteristic of gate stack structure. However, the value of breakdown field, calculated from BV divided by

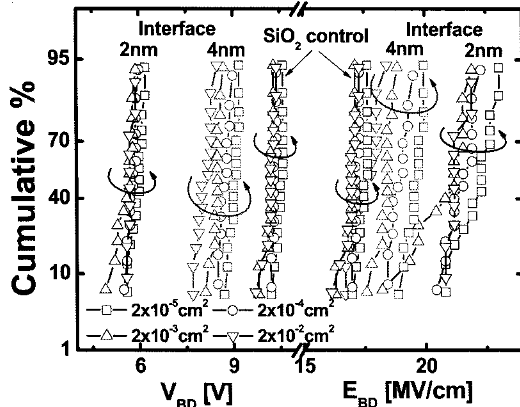

Fig. 2. Weibull plots with gate area of breakdown voltage (V_{BD}) and breakdown field (E_{BD}) under TZDB stress. Negligible area dependence indicates TZDB characteristics are intrinsic. Device A is excluded due to indistinct breakdown.

EOT of the gate stack, are more than 15MV/cm for all samples. These values are abnormally high compared to that of SiO_2, suggesting that the dielectric constant of SiO_2 layer is increased by oxygen deficiency. Therefore, the effective field in SiO_2 layer can be reduced to reasonable level. Especially, $HfSiO_x$(3nm)/SiO_2(2nm) sample shows the highest breakdown field, suggesting that Hf metal is more penetrated into SiO_2 and more intermixed with SiO_2.

As shown in Fig. 3, however, the threshold voltage of thick oxide device appears to be affected by $HfSiO_x$ layer. The distribution of threshold voltage for SiO_2 and $HfSiO_x$ single layer devices are tighter than those of $HfSiO_x$/SiO_2 stack devices. The wider distribution in stack devices comes from the Hf penetration into interfacial layer and/or intermixing of $HfSiO_x$ with underlying SiO_2 during post-annealing processes. This phenomenon is more pronounce for pMOSFET. If the penetration and/or the intermixing between two layers mainly cause into a wider distribution of V_{th}, however, there should be no difference between nMOSFETs and pMOSFETs. In addition to the chemical reaction, these results indicate that the injected charges are the main reason of the wider V_{th} distribution. For pMOSFETs, the charges injected from the gate electrode can be accumulated at the interface between $HfSiO_x$ and SiO_2, which in turn affects V_{th} distribution. On the other hand, nMOSFET shows relatively stable V_{th} because the thick oxide layer suppresses the tunneling from the substrate. These V_{th} distributions raise the concern about the dielectric reliability because typical reaction between $HfSiO_x$ layer and SiO_2 leads to a reduction of interfacial layer and an oxygen deficient oxide formation. Therefore, it is expected that the reliability of dielectric could be degraded.

According to the previous BV results, it is expected that stress induced leakage current (SILC)

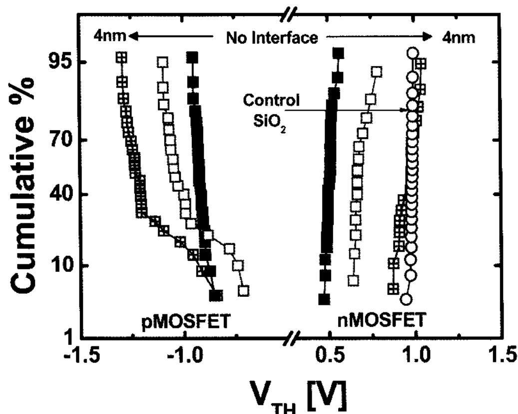

Fig. 3. V_{th} distribution of nMOSFET and pMOSFET. Difference in V_{th} is due to the EOT difference.

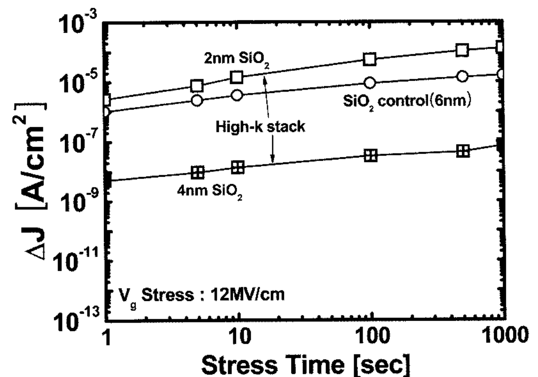

Fig. 4. SILC characteristics of stack structures at effective electric field of -12 MV/cm.

characteristics of 2nm interface device will be worse than other stack structures because of its oxygen deficient interfacial layer. To clarify the gate stack effect on oxide reliability, SILC measurements were performed (Fig 4). From the SILC results, 2nm interface device shows higher ΔJ_g slope. For the 2nm interfacial oxide device, in addition to the wider distribution of breakdown field (E_{bd}), J_g is also widely distributed as shown in the insect of Fig. 4. These results suggest that there is Hf penetration and/or interfacial reaction with $HfSiO_x$ and SiO_2, which in turn lead to the worse SILC characteristics and wider distribution of E_{bd} and J_g for 2nm interface device. For the 4nm interface device and the control SiO_2 device, the gate leakage current follows the Fowler-Nordheim (F-N) tunneling mechanism (data not shown). However, the 2nm interface device shows a trap assist tunneling (TAT) behavior rather than F-N tunneling, evidencing that traps are generated from the intermixing between $HfSiO_x$ and SiO_2 and/or Hf penetration into interfacial layer during post-annealing process.

4. Conclusion

For the fist time, the potential reliability problems of gate dielectrics with thin $HfSiO_x$ layer on thick SiO_2 region were investigated for multiple oxide application. Compared 6nm SiO_2 single oxide device, $HfSiO_x/SiO_2$ multiple oxide devices have no degradation in device performance such as high field mobility. In conjunction with charge trapping, however, the V_{th} distribution and TZDB characteristics are also affected by the reaction between $HfSiO_x$ layer and underlying SiO_2 layer. Since the stacking of a high-k layer on thick SiO_2 can reduce leakage current or improve the SILC properties, both electrical and reliability characteristics can be improved by optimization to minimize the reaction between high-k and SiO_2 layer.

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