CMOS Direct-Conversion RF Front-End Design for 5-GHz WLAN

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Abstract

Direct-conversion RF front-end for 5-GHz WLAN is implemented in 0.18-μm CMOS technology. The front-end consists of a low noise amplifier, and low flicker noise down-conversion mixers. For the mixer, an inductor is included to resonate out parasitic tail capacitances in the transconductance stage at the operating frequency, thereby improves the flicker noise performance of the mixer, and the overall noise performance of the front-end. The receiver RF front-end has 6.5 dB noise figure, −13 dBm input IP3, and voltage conversion gain of 20 dB with the power consumption of 30 mW.

Key words : IEEE802.11a, CMOS, HiperLAN2, OFDM, Radio Frequency(RF), Transceiver, WLAN.

Ⅰ. Introduction

In the last few years, there has been enormous growth in wireless LAN(WLAN) markets with the demands for mobility and convenience of wireless communications network. High data rate WLAN has been defined in the 5-GHz band that allows up to 54 Mbps, offering attractive solution for real-time imaging, multimedia, and high speed video application. There are two standards for the 5-GHz band, one is called HiperLAN2 and the other is IEEE802.11a[1],[2]. Both standards can operate in the lower 5.15~5.25 GHz band, the middle 5.25~5.35 GHz band, and the upper 5.725~5.825 GHz band occupying channel bandwidth of around 16.3 MHz with different modulation schemes such as binary phase shift keying(BPSK), quadrature phase shift keying(QPSK), quadrature amplitude modulation(QAM) which are mapped into subcarriers of an orthogonal frequency division multiplexing(OFDM) signal. The signal is constructed of forty-eight data and four pilot subcarriers spaced 312.5 kHz apart. In the spectrum, the zero-th subcarrier is not used to avoid the difficulties in digital-to-analog and analog-to-digital converter offsets and carrier feedthrough in the RF system. The required minimum detectable sensitivity level for IEEE802.11a standard is −82 dBm at the lowest data rate of 6 Mbps, and 65 dBm at the highest data rate of 54 Mbps.

The maximum input power is −30 dBm for 802.11a, and −20 dBm for HiperLAN2. The modulation accuracy of the transceiver is characterized by error vector magnitude(EVM) parameter. The standard requires better than −25 dB for the 64-QAM modulated signal. The receiver sensitivity level can be evaluated with packet error rate (PER) or bit error rate(BER). The required PER is less than 10 % at a PSDU(PHY Sublayer Service Data Units) length of 1,000 bytes[3].

With the advancement of short channel length processing technologies, CMOS becomes an attractive solution for 5-GHz range applications since it allows the single chip integration. Currently, many researches have been done to integrate all the transceiver blocks into a single chip to reduce the cost and complexity[3],[7].

This paper presents 5-GHz WLAN receiver RF front-end design implemented in 0.18-μm CMOS technology, which employs low flicker noise down-conversion mixers.

Ⅱ. Receiver Architecture

The wireless receivers can be implemented as heterodyne, low-IF or direct conversion(zero-IF)[8],[9]. To implement a low cost fully integrated chip, zero-IF or low-IF can be considered as candidates. The zero-IF has disadvantages of flicker noise($1/f$) which is especially troublesome for CMOS technologies, DC offset, even-order distortion, in-phase/quadrature(I/Q) mismatch, and LO pulling and leakage. The low-IF also suffers signaldegradation from even-order distortion, and LO pulling and leakage. Further, it requires an image rejection, whereas the zero-IF does not. Since the signal bandwidth in low-IF scheme is twice that in zero-IF, it requires doubling the channel selection filter bandwidth and analog-to-digital(ADC) sampling rate, and thus requires higher power consumption[10]. Several techniques have been already developed to tackle the disadvantages of zero-IF[3]~[5]. Therefore, a direct conversion scheme is chosen as the transceiver archi-

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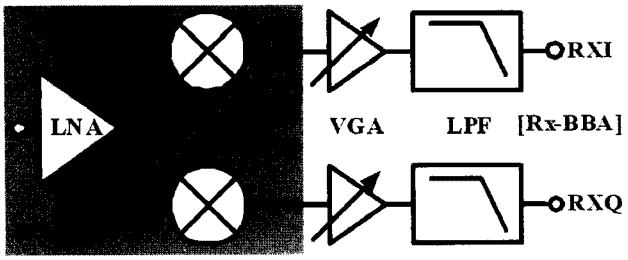


Fig. 1. Simplified direct conversion radio transceiver architecture.

tecture.

Fig. 1 shows the overall block diagram of the direct conversion receiver architecture. The receiver can be divided into: Rx-RF including an LNA and down-conversion quadrature mixers and receiver baseband analog (Rx-BBA) including VGA and LPF.

According to the Fri is equation explained in [8], the overall *NF* of the receiver is given by

$$NF_{Rx} = NF_{Rx-RF} + \frac{NF_{Rx-BBA} - 1}{A_{p,Rx-RF}}. \quad (1)$$

where NF_{Rx-RF} and NF_{Rx-BBA} are the *NF* of $Rx-RF$ and $Rx-BBA$ blocks, respectively. The power gain of the $Rx-RF$ block is given by

$$A_{p,Rx-RF} = \left(\frac{R_{in,Rx-RF}}{R_s + R_{in,Rx-RF}}\right) A_{v,Rx-RF}^2 \frac{R_S}{R_{out,Rx-RF}}. \quad (2)$$

where R_s is the source impedance usually with 50 Ω, R_{in}, R_{out}, and A_v are the input and output impedance, and voltage gain of the $Rx-RF$, respectively.

From (1) and (2), the receiver NF is mainly determined by the NF of the $Rx-RF$ block when the gain of the $Rx-RF$ is sufficiently high. So, the $NF_{Rx} \approx NF_{Rx-RF}$ at the high gain mode of the receiver.

Another consideration of the receiver is the third order nonlinearity. Typically, a loworder LPF is inserted between the down conversion mixer and the $Rx-BBA$ to have higher overall receiver linearity. The filter attenuates the interferers sufficiently, and the cumulative input IP_3 of the cascaded mixer plus *Rx-BBA* is mainly determined by the mixer linearity[8]. So, $IIP_{3,mixer}$ plus $Rx-BBA \approx IIP_{3,mixer}$.

The cascaded input IP_3 of the receiver is given by

$$\frac{1}{IIP_{3,Rx}^2} = \frac{1}{IIP_{3,LNA}^2} + \frac{A_{v,LNA}^2}{IIP_{3,mixer\ plus\ Rx-BBA}^2}. \quad (3)$$

The cumulative Rx-RF linearity is given by

$$\frac{1}{IIP_{3,Rx-RF}^2} = \frac{1}{IIP_{3,LNA}^2} + \frac{A_{v,LNA}^2}{IIP_{3,mixer}^2}. \quad (4)$$

Comparing (3) and (4),

$$\frac{1}{IIP_{3,Rx}^2} \approx \frac{1}{IIP_{3,Rx-RF}^2}. \quad (5)$$

From (5), it can be concluded that the overall receiver nonlinearity is approximately determined by the nonlinearity of the $Rx-RF$.

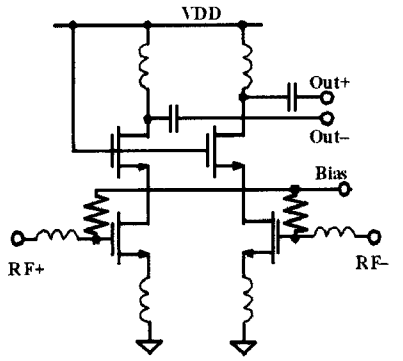
In Fig. 1, the signal path is implemented as fully differential to minimize the even-order distortion. The RF signal is applied to a differential low noise amplifier(LNA), translated to baseband signal through *I/Q* down-conversion mixers.

Ⅲ. Circuit Implementation

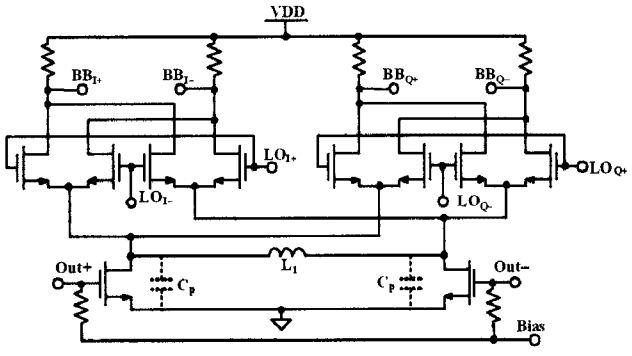
Fig. 2 shows the receiver front-end RF blocks which consist of an LNA, and down-conversion *I/Q* mixers. A differential cascode amplifier is also chosen in the LNA to reduce the LO leakage to the LNA input, and even order distortion. According to [11], the low frequency output noise current of the down-conversion mixer is given by

$$i_{o,n} = \frac{2C_p}{T} V_n \times \frac{(C_p \omega_{LO})^2}{g_{ms}^2 + (C_p \omega_{LO})^2} \quad (6)$$

where C_p is the tail capacitance of the mixer transconductance stage, V_n is the low-frequency noise at the gate of switch, ω_{LO} is the LO frequency, g_{ms} is the switch transconductance, and T is the LO period. From (4), it can be shown that the noise contribution is very



(a) An LNA



(b) Down-conversion I/Q mixers

Fig. 2. Receiver RF front-end blocks.

small when ω_{LO} is very small compared to g_{ms}/C_p. However, it rapidly increases as the tail capacitance goes up. The low frequency noise can be reduced by including an inductor, L_1, to resonate out the tail parasitic capacitance, and thereby increasing the conversion gain, and lowers flicker noise contribution from the indirect mechanism[11],[12].

As clearly shown in Fig. 3, the flicker noise in the down-conversion mixer below 100 kHz is significantly reduced with the on-chip spiral inductor compared to that without the inductor, and thereby the cascaded RF receiver NF is substantially improved around 100 kHz. The on-chip inductor does not occupy large chip areas and quality(Q) factor over ten at the 5-GHz operating frequency. Each differential input of the LNA is matched to 50 Ω using on-chip inductors to simplify the external matching.

Ⅳ. Experimental Results

The 5-GHz WLAN receiver are fabricated in single-poly, six-metal 0.18 μm CMOS technology as shown in Fig. 4. The die size is 1.9×1.3 mm^2. All the pads are

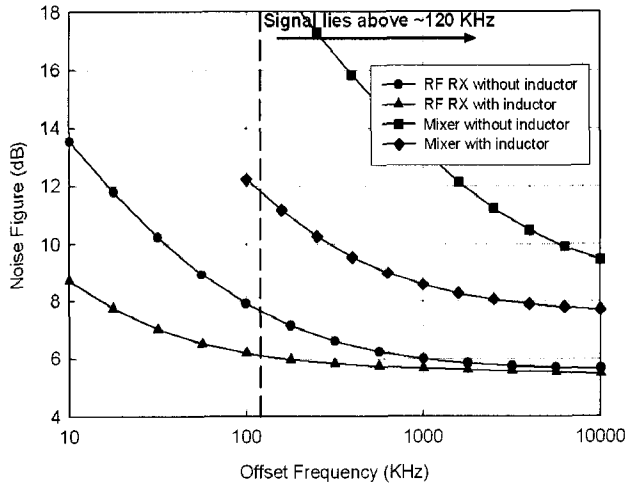


Fig. 3. Simulated receiver RF front-end and mixer-only NF with and without the inductor, L_1, in Fig. 2(b).

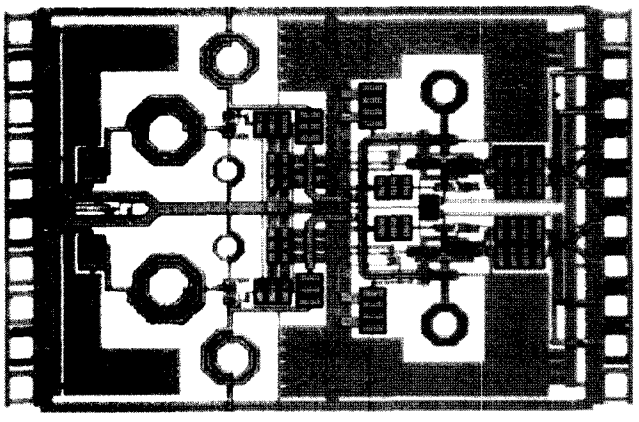
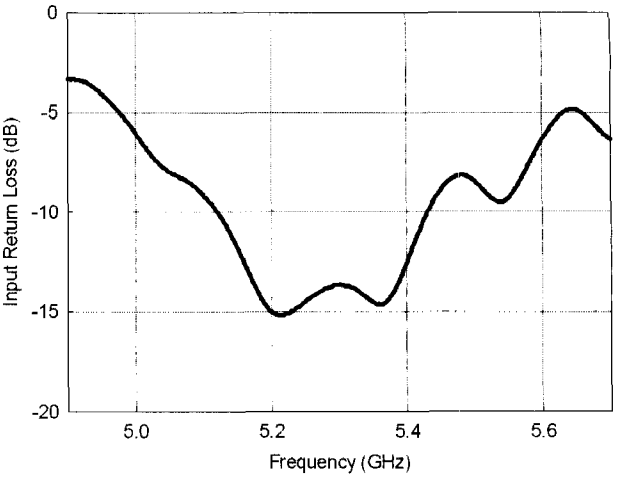
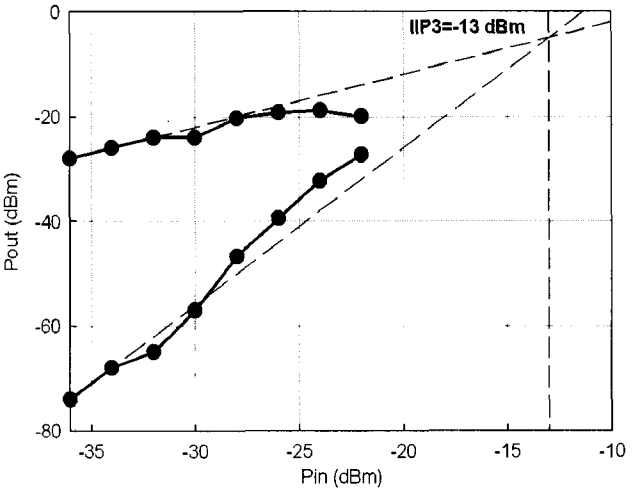


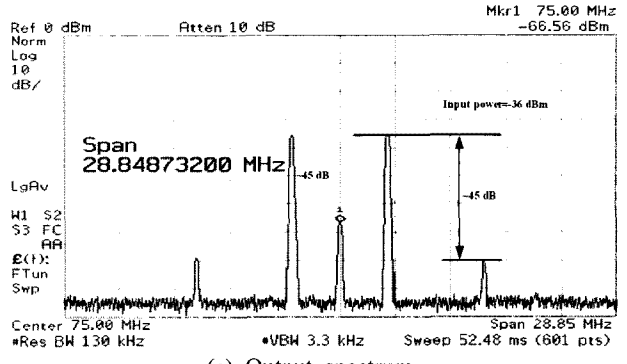
Fig. 4. Chip micrograph. The die size is 1.9×1.3 mm^2.



(a) Input return loss



(b) Input IP3



(c) Output spectrum.

Fig. 5. Measured results of the receiver RF front-end.

electrostatic discharge(ESD) protected. The receiver RF front-end measurement is performed by applying 5.26 GHz LO frequency and 5185±2.5 MHz two tone RF frequencies. 180° ring hybrid baluns[13] are implemented on test boards for the RF input of the receiver to divide powers. Fig. 5 shows the measured performance of the receiver front-end. The input return loss of the receiver is matched less than −10 dB in the operation frequency range of 5.15~5.35 GHz. The measured input IP3 is −13

Table 1. Performance comparison of 5 GHz receiver front-end.

		This work	[14]	[15]	[16]	[17]
Architecture		Zero IF	Zero IF	Zero IF	Double conver-sion	Double conver-sion
Supply voltage [V]		1.8	1.8	3	1.8	2
Receive front-end	Gain [dB]	20	30	18	31	12
	Input IP3 [dBm]	13	8	11.3	11.8	2
	NF [dB]	6.5	5*	3	5.1	5.2
Technology		0.18 μm CMOS	0.18 μm CMOS	0.25 μm CMOS	0.18 μm CMOS	0.25 μm CMOS

*Total receiver chain NF.

dBm. Including the RF cable loss of −2.2 dB@5 GHz and ring hybrid balun loss of −1 dB@5 GHz, the calibrated voltage conversion gain of the receiver front-end is 20 dB, and NF measured at 10 MHz IF is 6.5 dB. The total power consumption is 30 mW from a 1.8 V supply. Table 1 compares performances of several 5 GHz receiver front-end.

V. Conclusion

In this paper, a direct-conversion receiver for 5-GHz WLAN has been implemented using 0.18-μm CMOS technology. An inductor resonates out parasitic tail capacitances in the transconductance stage of the down-conversion mixer at the operating frequency, thereby improves the flicker noise performance of the mixer, and the overall noise performance of the front-end. The measured performance of the receiver RF front-end has 20 dB voltage conversion gain, NF of 6.5 dB, and −13 dBm input IP3 while consuming 30 mW from a 1.8 V supply.

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