Direct Duty Ratio Pulse Width Modulation Method for Matrix Converters

Yulong Li, Nam-Sup Choi*, Byung-Moon Han, Kyoung Min Kim, Buhm Lee, and Jun-Hyub Park

Abstract: This paper presents a new carrier based pulse-width modulation (PWM) method for matrix converters. By using the concept of average over one switching period, the modulation algorithm and the required equations are derived to synthesize the desired output voltage and to achieve the controlled input power factor. The proposed method uses a continuous carrier and the predetermined duty ratio signals to directly generate the gating signals and, thus, is referred to as "direct duty ratio PWM (DDPWM)". The feasibility and validity of the proposed method were verified by simulation and experiment.

Keywords: AC-AC power converter, carrier based PWM, matrix converter, pulse-width modulation (PWM).

1. INTRODUCTION

A matrix converter is a direct AC-AC converter which employs an array of bidirectional switches to provide an AC load with the desired AC voltages from AC input source voltages [1]. It is well known that this converter has several attractive features, as follows;

1) a simple and compact power circuit without any large energy storage elements
2) the generation of output voltages with variable magnitude and frequency
3) sinusoidal input and output currents
4) controlled input power factor
5) inherent regeneration capability.

The matrix converter can be applied to variable power conversion, AC drive and renewable power generation [2-4].

The key elements of a three-phase to three-phase matrix converter are the nine fully controlled four-quadrant bidirectional switches. These switches have to be controlled on or off simultaneously, resulting in complex modulating tasks. Several modulation methods have been developed up to now. The principle of the matrix converter was first proposed by Alesina and Venturini [5], where the voltage transfer ratio, q, which is defined as the ratio of the magnitudes of the output voltage to the input voltage, was limited to 0.5. In [6], the Optimum Alesina–Venturini(OAV) method was proposed, in which q was extended to 0.866 by using the third harmonic injection technique. It was also proved in [6] that a q of 0.866 is the physical limitation of the matrix converter with balanced input voltages. In [7], the scalar control modulation algorithm was proposed, whose performance is similar to that obtained by the OAV method. These modulation methods in [5] to [7] have the disadvantage of incurring a formidable amount of complex calculations.

Space vector pulse-width modulation(SVPWM) methods for matrix converters were developed in [8-12]. In the SVPWM method, the modulation task of the matrix converter can be resolved into the pulse-width modulation(PWM) converter and the inverter modulations by supposing a virtual configuration of a PWM rectifier and a PWM inverter linked by an imaginary DC link. Through the modulation of the output voltage space vector and input current space vector, the control of input power factor and maximum voltage conversion can be achieved with the sophisticated SVPWM. However, lookup tables with stored switching patterns need to be initialized ahead of its implementation. Also, the generation of the gating signal is far from intuitive, since several vectors are utilized in one switching period.

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A carrier-based modulation technique, which is basically identical to the SVPWM method, was explored in [13] and [14]. This method involves the use of proper offset voltages to generate output pole voltage references which are compared with a discontinuous carrier to generate the gating signals. This method can be implemented without complex calculations and lookup tables. However, it is difficult to intuitively understand the modulation principle because it employs a discontinuous carrier waveform. Also, the modulation algorithm requires additional complicated modifications in order to get a q value of 0.866 [13]. Because of the introduction of offset voltages, this method cannot be applied to other matrix converter topologies with a neutral connection between the input and output neutrals.

In this paper, a new carrier based PWM method for matrix converters is developed by using the concept of the per-output-phase average over one switching period, i.e., per-carrier cycle. When the desired output phase voltage references are given, they can be synthesized by utilizing the input phase voltages over one switching period in the average sense. At the beginning of each switching period, the duty ratio values ranging from 0 to 1 for each output phase are predetermined. These duty ratio values will be compared with a continuous triangular carrier waveform common to all of the output phases going up from 0 to 1 and down from 1 to 0, in order to generate the corresponding PWM signals. The desired output voltages can be directly synthesized by updating the duty ratio values at each switching cycle and, thus, the proposed method is named "direct duty ratio PWM(DDPWM)". The maximum q value of 0.866 can be simply obtained by injecting the third harmonic components into the output voltage references.

In addition, by simply changing the slope of the carrier, which could be considered as another degree of freedom, the input power factor can be controlled while maintaining the sinusoidal input currents. The calculations for the synthesis of the input power factor and determination of the carrier slope are much simpler than those in [14].

The proposed DDPWM can be easily implemented without complex calculations and lookup tables like common carrier-based PWMs. The feasibility and validity of the proposed method are verified by PSCAD/EMTDC simulations and experiments.

2. OUTPUT VOLTAGE SYNTHESIS

2.1. Proposed DDPWM controller

Fig. 1 shows the circuit configuration including the three-phase input voltages, input filter, three-phase to three-phase matrix converter and resister-inductor(R-L) load.

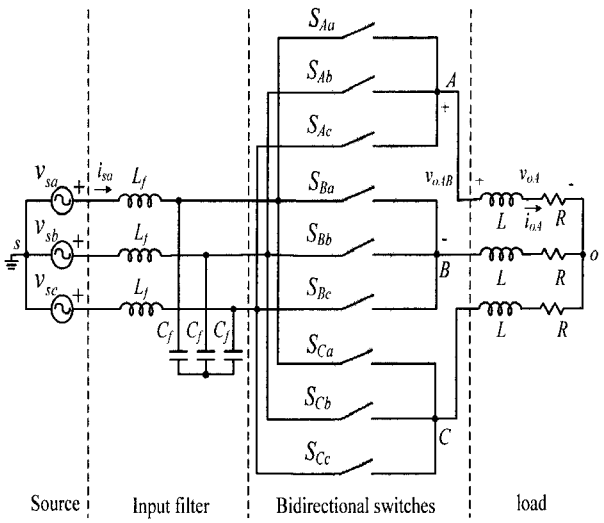

Fig. 1. Three-phase to three-phase matrix converter circuit.

If the only maximum one of the three line-to-line voltages is used as the input voltage to synthesize the output voltages during each switching period, then two of the three input phase voltages will be used. Consequently, one of the input phases does not conduct any current during the switching period, so that the input current will be distorted. The DDPWM uses two out of three of the line-to-line input voltages to synthesize the output voltages. Hence, all three input phases are utilized to conduct current during each switching period and, consequently, the input currents will not be distorted.

A switching period T_s is divided into two time periods, T_1 and T_2. Also, *MX*, *MD* and *MN* denote the maximum, medium and minimum input voltage values, respectively. During T_1, the line-to-line voltage between *MX* and *MN*, which is the maximum line-to-line voltage among the three line-to-line input voltages at the sampling instant, is used. During T_2, the second maximum line to line voltage, which is the larger of *MX* to *MD* and *MD* to *MN*, is used. If *MX-MD* > *MD-MN*, *MX* to *MD* is used during T_2 and the resultant switching pattern is named switching pattern-I. Otherwise, *MD* to *MN* is used during T_2, namely switching pattern-II.

Switching pattern-I: Fig. 2 shows the case of switching pattern-I for generating the A-phase output voltage, where the triangular carrier is compared with the duty ratio value, d_{A1}, resulting in the change of the output phase voltage such that *MN*→*MX*→*MD*. Fig. 3 shows the actual A-phase output voltage synthesis when applying switching pattern-I. As seen in Fig. 2 and Fig. 3, *MN*, *MX*, *MX* and *MD* appear at the A-phase output terminal during T_{A1}, T_{A2}, T_{A3} and T_{A4} respectively. These four sub-intervals can be expressed as

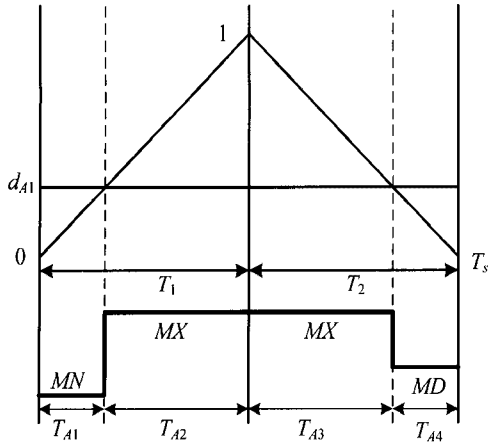

Fig. 2. Output A-phase switching state in switching pattern-I.

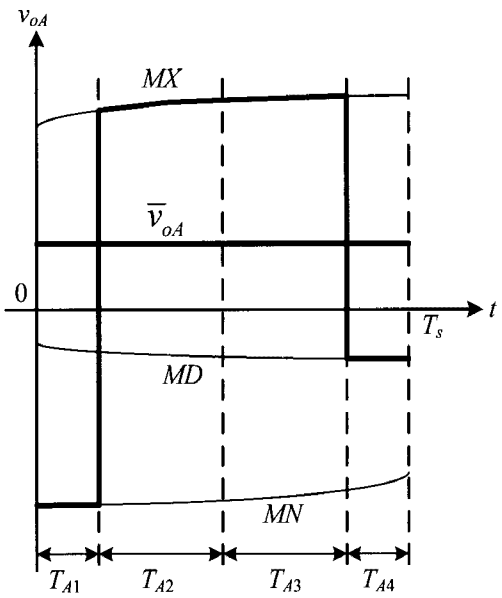

Fig. 3. Output A-phase voltage synthesis in switching pattern-I.

$$
\begin{aligned}
T_{A1} &= d_{A1} n T_s, \\
T_{A2} &= (1 - d_{A1}) n T_s, \\
T_{A3} &= (1 - d_{A1})(1 - n) T_s, \\
T_{A4} &= d_{A1} (1 - n) T_s,
\end{aligned} \tag{1}
$$

where d_{A1} is the A-phase duty ratio value when switching pattern-I is applied and n is defined as $n = T_1/T_s$ which involves the slope of the carrier.

Supposing that the input voltages are almost constant during the switching cycles, the integration of the output voltage v_{oA} over T_s can be written as

$$
\begin{aligned}
\int_0^{T_s} v_{oA}\, dt \;\cong\; & T_{A1} \cdot MN + (T_{A2} + T_{A3}) \cdot MX \\
& + T_{A4} \cdot MD .
\end{aligned} \tag{2}
$$

Then, it is found from (1) and (2) that the averaged value of v_{oA}, $\overline{v}_{oA}$, can be approximated by

$$
\begin{aligned}
\overline{v}_{oA} &= \frac{1}{T_s} \int_0^{T_s} v_{oA} dt \\
&\cong d_{A1} (n \cdot MN - n \cdot MD + MD - MX) + MX .
\end{aligned} \tag{3}
$$

By letting $\overline{v}_{oA}$ be equal to the A-phase output voltage command, v_{oA}^*, that is $\overline{v}_{oA} = v_{oA}^*$, the duty ratio value, d_{A1}, for the present switching period can be calculated as

$$
d_{A1} = \frac{1}{n \cdot MN - n \cdot MD + MD - MX} \left(v_{oA}^* - MX \right). \tag{4}
$$

Fig. 4. Output A-phase switching state in switching pattern-II.

Fig. 5. Output A-phase voltage synthesis in switching pattern-II.

Switching pattern-II: In the same way, switching pattern-II can be analyzed. Fig. 4 shows the case of switching pattern-II for generating the A-phase output voltage where the triangular carrier is compared with

the duty ratio value, d_{A2}, so that the time intervals, viz. T_{A1}, T_{A2}, T_{A3} and T_{A4}, are predetermined as given in equation (1) and the output phase voltage is changed with the sequence of $MN \rightarrow MX \rightarrow MD \rightarrow MN$. When applying switching pattern-II, the A-phase output voltage is actually synthesized as shown in Fig. 5. As seen in Figs. 4 and 5, MN, MX, MD and MN appear sequentially at the A-phase output terminal. In this case, the integration of the output voltage v_{oA} over T_s is expressed by

$$\int_0^{T_s} v_{oA} dt \cong T_{A1} \cdot MN + T_{A2} \cdot MX + T_{A3} \cdot MD + T_{A4} \cdot MN . \quad (5)$$

Similarly, it can be found from (1) and (5) that the averaged value of v_{oA}, $\overline{v}_{oA}$, can be approximated by

$$\overline{v}_{oA} = \frac{1}{T_s}\int_0^{T_s} v_{oA}\, dt \cong d_{A2} \cdot (MN - n \cdot MX - MD + n \cdot MD) + n \cdot MX - n \cdot MD + MD. \quad (6)$$

Again, by letting $\overline{v}_{oA}$ be equal to the A-phase output voltage command, v_{oA}^*, the duty ratio value, d_{A2}, can be obtained as follows

$$d_{A2} = \frac{v_{oA}^* - (n \cdot MX - n \cdot MD + MD)}{MN - n \cdot MX - MD + n \cdot MD}. \quad (7)$$

In summary, the duty ratio value d_A for the A-phase at each switching cycle is determined by

$$d_A = \begin{cases} \dfrac{v_{oA}^* - MX}{n \cdot MN - n \cdot MD + MD - MX} & \text{for Pattern-I} \\ \dfrac{v_{oA}^* - (n \cdot MX - n \cdot MD + MD)}{MN - n \cdot MX - MD + n \cdot MD} & \text{for Pattern-II.} \end{cases} \quad (8)$$

The gating signals of the three bidirectional switches can be directly generated considering the switching states in Fig. 2 and Fig. 4. If the switching state of the output phase "A" is MX, the output phase "A" is connected to the input phase whose voltage is MX. In the same fashion, in the case where the switching state of output phase "A" is MD or MN, the load phase "A" is connected to the input phase whose voltage is MD or MN, respectively. Practically, by using simple digital logic devices, the gating signal can be easily generated.

2.2. DDPWM controller for three-phase matrix converter

The duty ratio control law of the A-phase output is defined by (8). The other two output phases can be treated in the same manner. It should be noticed that the three output phase voltages can be separately controlled to follow their own references. This fact implies that the DDPWM controller can be implemented with a modular structure for each phase.

With the B-phase and C-phase output voltage commands, v_{oB}^* and v_{oC}^*, respectively, the duty ratio values, d_B and d_C for the B-phase and C-phase, respectively, can be obtained in the same way, as follows

$$d_B = \begin{cases} \dfrac{v_{oB}^* - MX}{n \cdot MN - n \cdot MD + MD - MX} & \text{for Pattern-I} \\ \dfrac{v_{oB}^* - (n \cdot MX - n \cdot MD + MD)}{MN - n \cdot MX - MD + n \cdot MD} & \text{for Pattern-II,} \end{cases} \quad (9)$$

$$d_C = \begin{cases} \dfrac{v_{oC}^* - MX}{n \cdot MN - n \cdot MD + MD - MX} & \text{for Pattern-I} \\ \dfrac{v_{oC}^* - (n \cdot MX - n \cdot MD + MD)}{MN - n \cdot MX - MD + n \cdot MD} & \text{for Pattern-II.} \end{cases} \quad (10)$$

2.3 Simulation

A simulation of the three-phase to three-phase matrix converter shown in Fig. 1 is performed by using PSCAD/EMTDC. The simulation parameters are shown in Table 1. The switching period T_s is 200 μs, and T_1=T_2=100 μs, thus n=0.5.

The simulation results are shown in Fig. 6. Fig. 6 shows the output line-to-line voltage v_{oAB}, A-phase output current i_{oA}, input phase voltage v_{sa} and filtered input current $i_{sa\text{-}f}$. In Fig. 6, the waveform of the input current is processed by a second-order low pass filter whose cut-off frequency is 500 Hz and damping ratio is 0.7.

It can be seen from the simulation results that the proposed method is able to well synthesize the output voltages. However, the input current is distorted. This is because no attention has been paid to the synthesis of the input current. In the next section, the input current will be synthesized by controlling n.

Table 1. Simulation parameters.

R-L load	R=20 Ω, L=50 mH
Voltage transfer ratio	q=0.5
Input voltage (line-to-line RMS) $V_{s\text{-RMS}}$	220 V
Output voltage (line-to-line RMS) $V_{o\text{-RMS}}$	110 V
Input frequency f_s	60 Hz
Output frequency f_o	30 Hz

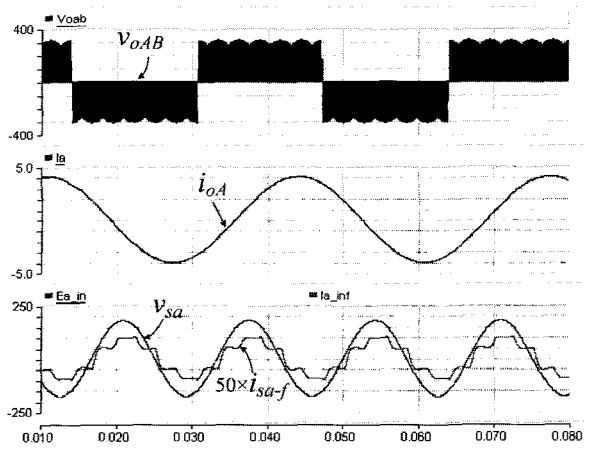

Fig. 6. Simulation results when n=0.5.

3. INPUT CURRENT SYNTHESIS

3.1. Input current synthesis for three-phase matrix converter

In the previous section, the output voltages are well synthesized. However, the input current is distorted, because no effort is made to control the input power factor. In the global duty ratio laws in (8), (9), and (10), there is another degree of freedom, that is n. n can be properly adjusted to synthesize the sinusoidal input current, while maintaining T_s at a constant value. Since n is already considered in the derivation of (8)-(10), the output voltage synthesis will not be disturbed by changing the value of n.

During one switching period T_s, the output current can be treated as a constant value. Therefore, the input current can be synthesized according to the PWM switching pattern. The four subintervals in T_s for each output phase A, B, C can be collected as

$$\begin{aligned}
T_{A1} &= d_A n T_s = d_A T_1,\\
T_{A2} &= (1-d_A) n T_s = (1-d_A) T_1,\\
T_{A3} &= (1-d_A)(1-n) T_s = (1-d_A) T_2,\\
T_{A4} &= d_A (1-n) T_s = d_A T_2,
\end{aligned} \tag{11}$$

$$\begin{aligned}
T_{B1} &= d_B n T_s = d_B T_1,\\
T_{B2} &= (1-d_B) n T_s = (1-d_B) T_1,\\
T_{B3} &= (1-d_B)(1-n) T_s = (1-d_B) T_2,\\
T_{B4} &= d_B (1-n) T_s = d_B T_2,
\end{aligned} \tag{12}$$

$$\begin{aligned}
T_{C1} &= d_C n T_s = d_C T_1,\\
T_{C2} &= (1-d_C) n T_s = (1-d_C) T_1,\\
T_{C3} &= (1-d_C)(1-n) T_s = (1-d_C) T_2,\\
T_{C4} &= d_C (1-n) T_s = d_C T_2.
\end{aligned} \tag{13}$$

Switching pattern-I: Considering the output phase switching state of switching pattern-I, as shown in Fig. 2, the input phase MN is connected to the output terminal A, B, C in T_{A1}, T_{B1} T_{C1}, respectively. In the same way, input phase MD is connected to A, B, C in T_{A4}, T_{B4}, T_{C4} and input phase MX is connected to A, B, C in $(T_{A2}+T_{A3})$, $(T_{B2}+T_{B3})$, $(T_{C2}+T_{C3})$, respectively. In notation, i_{sMN}, i_{sMD} and i_{sMX} are used to denote the input currents whose voltages are MN, MD and MX, respectively. Then, by using the average concept, we have

$$i_{sMN} T_s = T_{A1} i_{oA} + T_{B1} i_{oB} + T_{C1} i_{oC}, \tag{14}$$

$$i_{sMD} T_s = T_{A4} i_{oA} + T_{B4} i_{oB} + T_{C4} i_{oC}, \tag{15}$$

$$\begin{aligned}
i_{sMX} T_s = {} & (T_{A2} + T_{A3}) i_{oA} + (T_{B2} + T_{B3}) i_{oB}\\
& + (T_{C2} + T_{C3}) i_{oC}.
\end{aligned} \tag{16}$$

Substituting (11)-(13) into (14)-(16), one can obtain

$$i_{sMN} T_s = (d_A i_{oA} + d_B i_{oB} + d_C i_{oC}) T_1, \tag{17}$$

$$i_{sMD} T_s = (d_A i_{oA} + d_B i_{oB} + d_C i_{oC}) T_2, \tag{18}$$

$$i_{sMX} = -(d_A i_{oA} + d_B i_{oB} + d_C i_{oC}). \tag{19}$$

Then substituting (19) into (17), (20) can be obtained.

$$n \equiv \frac{T_1}{T_s} = -\frac{i_{sMN}}{i_{sMX}}. \tag{20}$$

Switching pattern-II: Considering the output voltage switching state of switching pattern-II in Fig. 4, the input phase MX is connected to the output terminal A, B, C in T_{A2}, T_{B2}, T_{C2}, respectively. Similarly, the input phase MD is connected to A, B, C in T_{A3}, T_{B3}, T_{C3}, and input phase MN is connected to A, B, C in $(T_{A1}+T_{A4})$, $(T_{B1}+T_{B4})$, $(T_{C1}+T_{C4})$, respectively. Then, in the same manner, we can obtain

$$\begin{aligned}
i_{sMN} T_s = {} & (T_{A1} + T_{A4}) i_{oA} + (T_{B1} + T_{B4}) i_{oB}\\
& + (T_{C1} + T_{C4}) i_{oC},
\end{aligned} \tag{21}$$

$$i_{sMD} T_s = T_{A3} i_{oA} + T_{B3} i_{oB} + T_{C3} i_{oC}, \tag{22}$$

$$i_{sMX} T_s = T_{A2} i_{oA} + T_{B2} i_{oB} + T_{C2} i_{oC}. \tag{23}$$

Substituting (11)-(13) to (21)-(23), we can obtain

$$i_{sMN} = d_A i_{oA} + d_B i_{oB} + d_C i_{oC}, \tag{24}$$

$$i_{sMD} T_s = -(d_A i_{oA} + d_B i_{oB} + d_C i_{oC}) T_2, \tag{25}$$

$$i_{sMX} T_s = -(d_A i_{oA} + d_B i_{oB} + d_C i_{oC}) T_1. \tag{26}$$

Substituting (24) into (26), (27) can be obtained.

$$n = \frac{T_1}{T_s} = -\frac{i_{sMX}}{i_{sMN}}. \tag{27}$$

In summary, n is determined by the following equation.

$$n = \begin{cases} -\dfrac{i_{sMN}}{i_{sMX}} & : \text{pattern-I} \\ -\dfrac{i_{sMX}}{i_{sMN}} & : \text{pattern-II.} \end{cases} \tag{28}$$

It is worth noting that under the condition of unit

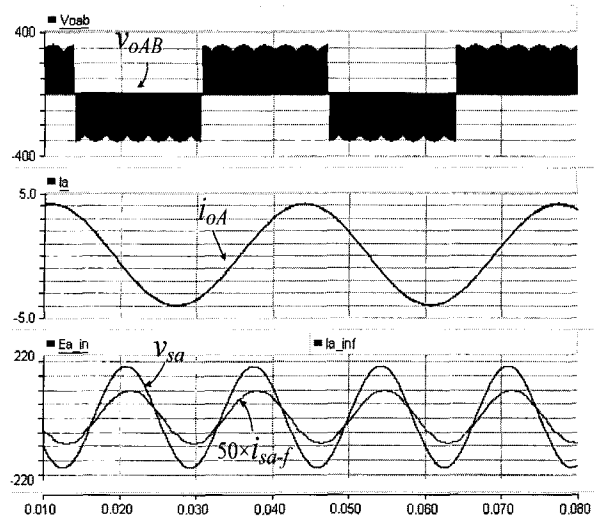

Fig. 8. Simulation results with input current synthesis.

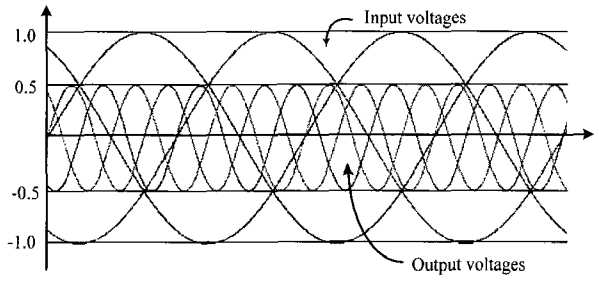

Fig. 9. Sinusoidal output voltages referenced to input neutral, fitting into input three-phase voltage system.

set is expressed by

$$\begin{aligned} v_{oA}^{*} &= V_o \sin(2\pi f_o t) + f(t), \\ v_{oB}^{*} &= V_o \sin\left(2\pi f_o t - \frac{2\pi}{3}\right) + f(t), \\ v_{oC}^{*} &= V_o \sin\left(2\pi f_o t + \frac{2\pi}{3}\right) + f(t), \end{aligned} \tag{30}$$

where V_o is the output voltage magnitude and f_o is the output frequency. The sinusoidal output references ride on a common mode voltage $f(t)$. However, the output line-to-line voltage will not be changed.

In [6], it is found that the term $f(t)$ is a combination of the third harmonics of the input and output voltages, that is

$$\begin{aligned} f(t) = &-\frac{\sqrt{6}}{12} V_{s\text{-RMS}} \sin(6\pi f_s t) \\ &+ \frac{1}{6} V_o \sin(6\pi f_o t), \end{aligned} \tag{31}$$

where $V_{s\text{-RMS}}$ is the rms value of the input phase voltage and f_s is the input frequency.

It should be noted that only the output references are modified and that the input current synthesis is not disturbed.

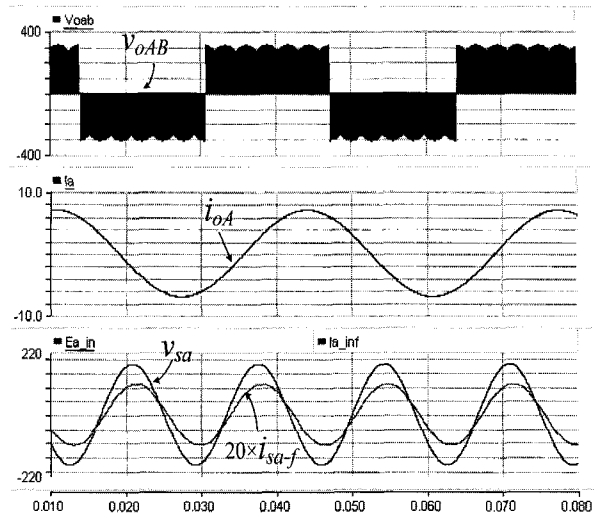

Fig. 10. Simulation results when q=0.866.

Again, the simulation is carried out when q=0.866. Except for the voltage transfer ratio, q, the other simulation conditions are the same as those in Table 1. The simulation results are shown in Fig. 10. It can be concluded that the output voltages whose q is 0.866 and the input currents are well synthesized without any distortions.

4. EXPERIMENTS

4.1. Experimental setup

To verify the feasibility of the proposed DDPWM method, an experimental setup was built and the DDPWM controller was implemented using TMS320VC33 DSP from Texas Instruments and Altera EP1K100QC208-1 CPLD. The matrix converter parameters are given in Table 4. The experimental configuration is shown in Fig. 11. As shown in Fig. 11, two of the three input line-to-line voltages v_{sab} and v_{sbc} are sensed, in order to calculate the three input phase voltages, v_{sa}, v_{sb} and v_{sc}. The sampled values of v_{sa}, v_{sb} and v_{sc} are then used to perform the necessary calculation. An input phase locked loop(PLL) is also incorporated into the DSP to obtain the input voltage angle α_i and to determine the proper switching pattern. The three input phase currents i_{sa}, i_{sb}, i_{sc} are sensed only for protection purposes. The three output phase currents i_{oA}, i_{oB} and i_{oC} are sensed for both control and protection purposes. A picture of the experimental setup is also shown in Fig. 12.

Table 4. Matrix converter parameters.

Rated Input voltage (line-to-line RMS) $V_{s\text{-RMS}}$	220 V
Inductance of input filter L_f	100 μH
Capacitance of input filter C_f	60 μF
Rated voltage of IGBT	600 V
Rated current of IGBT	200 A

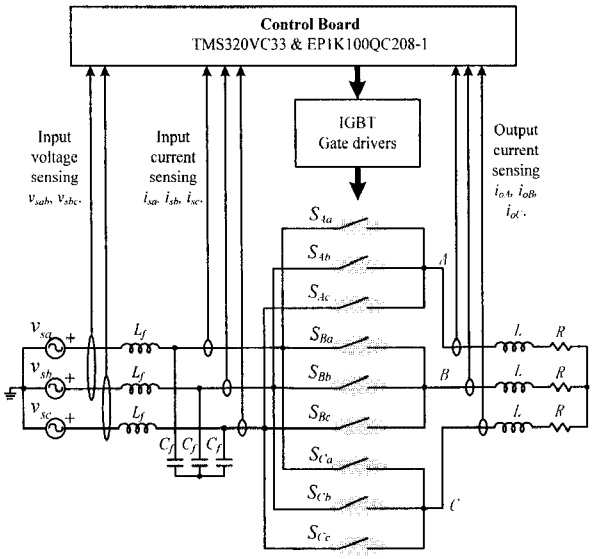

Fig. 11. Configuration of experimental setup.

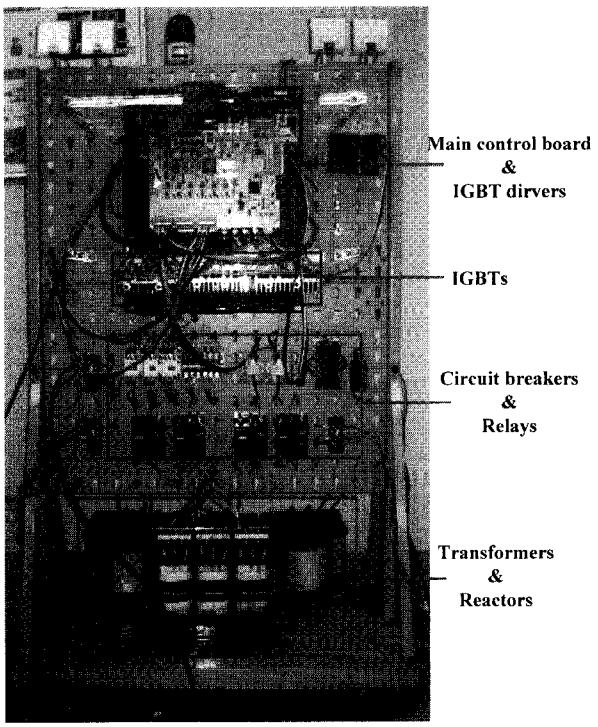

Fig. 12. Picture of experimental setup.

Table 5. Experimental parameters for steady state operation.

R-L load	R=20 Ω, L=50 mH
Voltage transfer ratio q	0.866
Input voltage (line-to-line RMS) $V_{s\text{-RMS}}$	220 V
Output voltage (line-to-line RMS) $V_{o\text{-RMS}}$	190 V
Input frequency f_s	60 Hz
Output frequency f_o	10 Hz
Switching frequency f_{sw}	5 kHz
Switching period T_s	200 μs

4.2. Experimental results

Steady state operation: The experimental conditions are shown in Table 5. The experimental waveforms are shown in Fig. 13. Fig. 13 contains the steady state experimental waveforms of the output line-to-line voltage v_{oAB}, output current i_{oA}, input voltage v_{sa} and input current i_{sa}. In Fig. 13, i_{sa} shows a small phase difference with the leading power factor, because of the input filter. It can be confirmed that the proposed direct PWM method is able to effectively synthesize both the output voltage and input current

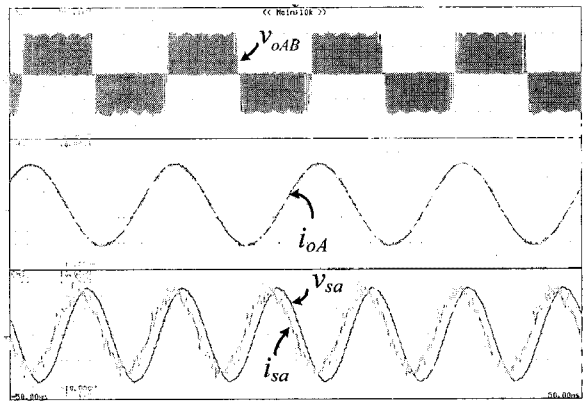

Fig. 13. Experimental waveforms: steady state operation, v_{oAB}(100 V/div, 10 ms/div), i_{oA}(2 A/div, 10 ms/div), v_{sa}(50 V/div, 10 ms/div), i_{sa} (2 A/div, 10 ms/div).

Table 6. Experimental parameters for dynamic operation when q is changed.

R-L load	R=20 Ω, L=50 mH
Voltage transfer ratio q	0.5 to 0.866
Input voltage (line-to-line RMS) $V_{s\text{-RMS}}$	220 V
Output voltage (line-to-line RMS) $V_{o\text{-RMS}}$	110 V to 190 V
Input frequency f_s	60 Hz
Output frequency f_o	30 Hz
Switching frequency f_{sw}	5 kHz
Switching period T_s	200 μs

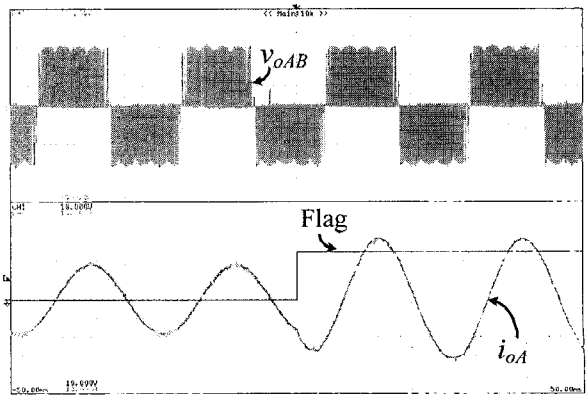

Fig. 14. Experimental waveforms: dynamic operation when q is changed; v_{oAB}(100 V/div, 10 ms/div), i_{oA}(2 A/div, 10 ms/div).

Table 7. Experimental parameters for dynamic operation when f_o is changed.

R-L load	R=20 Ω, L=50 mH
Voltage transfer ratio q	0.866
Input voltage (line-to-line RMS) $V_{s\text{-RMS}}$	220 V
Output voltage (line-to-line RMS) $V_{o\text{-RMS}}$	190 V
Input frequency f_s	60 Hz
Output frequency f_o	30 Hz to 60 Hz
Switching frequency f_{sw}	5 kHz
Switching period T_s	200 μs

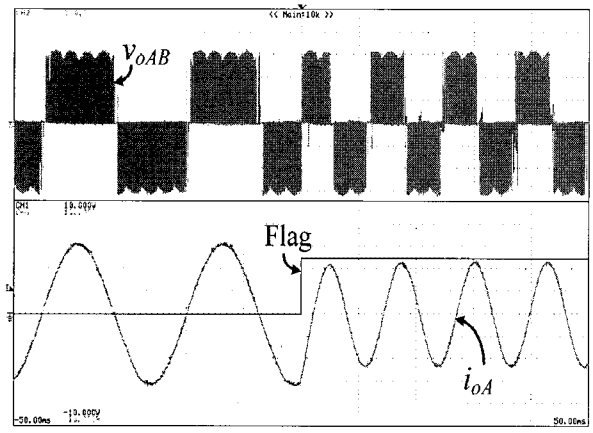

Fig. 15. Experimental waveforms: dynamic operation when f_o is changed; v_{oAB}(100 V/div, 10 ms/div), i_{oA}(2 A/div, 10 ms/div).

while achieving unity input power factor.

Dynamic operation: The experimental conditions when q changes are shown in Table 6 and the experimental waveforms are shown in Fig. 14. Dynamic operation when the output frequency f_o changes is also carried out. The experimental conditions when f_o changes are listed in Table 7 and Fig. 15 shows the experimental waveforms. The output line-to-line voltage v_{oAB} and output current i_{oA} are shown in Figs. 14 and 15 where the instant of Flag signal step change implies the instant of the command change. It can be seen from these dynamic waveforms that the proposed DDPWM control method provides fast dynamics and stable operation.

5. CONCLUSIONS

This paper presents a novel DDPWM based on the use of a continuous carrier to modulate matrix converters. By selecting the proper switching pattern and generating the exact duty ratios, the output voltages can be well synthesized. It is also possible to control the input power factor by changing the slope of the carrier. The DDPWM does not require any complex calculations and lookup tables. The feasibility and validity of the proposed method were verified by means of computer simulations and experimental results. The experimental results show that both the output voltages and input currents can be effectively modulated. Because the DDPWM has good applicability and flexibility, it can be effectively applied to various matrix converters, such as the two-phase, two-phase three-leg and three-phase four-leg matrix converters. Also, it can be applied to a matrix converter with a connection between the input and output neutrals. It can be concluded that the proposed method offers a very simple and effective way to modulate matrix converters.

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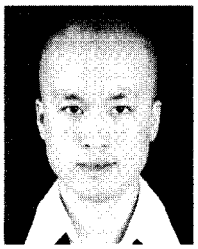

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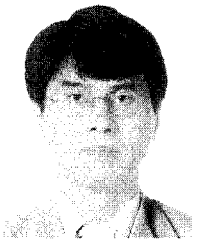

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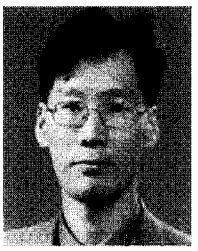

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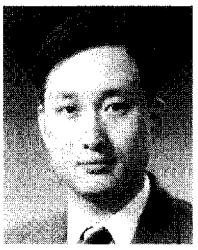

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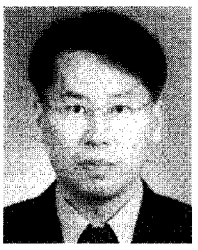

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