Implementation of PDP Driving Circuit for AC-Type

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Abstract—PDP(Plasma Display Panel) driving circuit requires switching devices and capacitors to stand up high voltages over 150volts. Thereby the power consumption and the cost of a PDP driving circuit increase. In this paper, a PDP driving circuit is proposed that can be operated with a lower supply voltage than the supply voltage of conventional driving circuit. The operation of the proposed driving circuit is verified by the computer simulation and experiments. PSPICE simulation and experiments results show that the output signal can drive PDP cells when the supply voltage is higher than 40volts.

Index Terms—PDP, driving circuit, low power, low voltage

I. INTRODUCTION

PDP has the many advantages such as large screen size, fast response and thin thickness[1]. PDP operates in three periods of resetting, addressing and sustaining to display the images. During the sustaining period the sustaining pulses are applied between the scanning and sustaining electrodes, the selected PDP cells emit the light and the image is displayed. However, PDP driving circuit requires the high supply voltage to drive PDP cells over 150 or 160 volts during sustaining period. To implement of the sustain circuit the switching devices and capacitors to stand up to high voltages is required because of applying the high driving voltages[2,3]. This is the main cause that the power consumptions and the cost of PDP driving circuit increase. This problem can be solved if the driving circuit can be operated with low supply voltage[4,5]. Many researchers have targeted decrease of supply voltage to reduce power consumption. The supply voltage of TERES(Technology of Reciprocal Sustainer) circuit is the half of conventional supply voltage to drive PDP cells[3].

In this paper, we propose a driving circuit for AC-type PDP that can be operated with the quarter supply voltage compared to the supply voltage of the conventional circuit during sustaining period. And when the time gap exists between the switch control signals the power consumption is simulated. The operation and characteristics of the designed circuit are confirmed by PSPICE simulation and experiments.

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II. DESIGN OF DRIVING CIRCUIT

Fig. 1 shows the schematic of proposed driving circuit for AC-type PDP which is composed of NMOS and PMOS power transistors, capacitors and diodes. In Fig. 1 the switch SWA and SWA' are NMOS power transistors and the switch SWB and SWB' are PMOS power transistors.

The power consumption is given by[6]

$$P(W) = CV_S^2 f \tag{1}$$

where C is the sum of the capacitance, V_S is the supply voltage and f is the operating frequency. If the supply voltage is reduced into a quarter in Eq. (1), the power loss must be decreased. We design the circuit can operate with just a quarter of the supply voltage used in the conventional circuit. The supply voltage, V_{DD}, is 40volts.

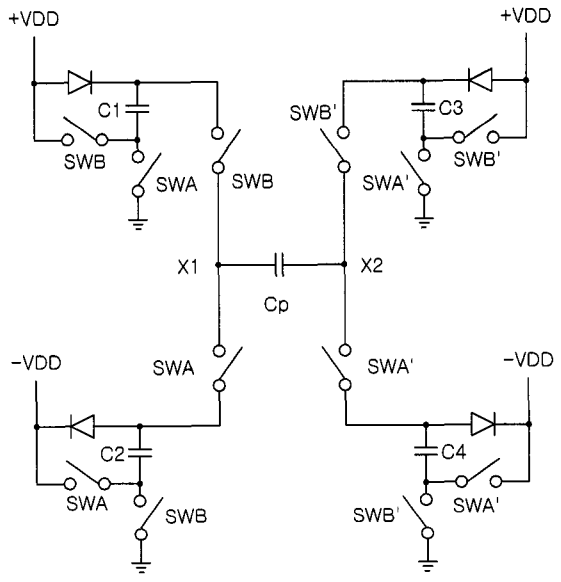

Fig. 1 The schematic of proposed PDP driving circuit

Fig. 2 shows the current flow when the circuit is operated. During the first half period, the switch SWA' and SWB are turned on and the switch SWA and SWB' are turned off. And the switch SWA' and SWB are turned off and the switch SWA and SWB' are turned on during the next half period.

When the switch SWA' and SWB are turned on and the switch SWA and SWB' are turned off the current flow is described by the solid line. The capacitors C2 and C3 are charged with $-V_{DD}$ and V_{DD}, respectively. At the next half period when the switch SWA' and SWB are turned off and the switch SWA and SWB' are turned on the current flow is described by the dotted line, the capacitors C1 and C4 are charge with V_{DD} and $-V_{DD}$, respectively.

When the switch SWA' and SWB are in the on state, the voltage at the node X1 is $+2V_{DD}$ due to the voltage charged across the capacitors C1 and the supply voltage. And the voltage is $-2V_{DD}$ at the node X2 due to the voltage charged across the capacitors C4 and the supply voltage. At that time the capacitors C2 and C3 are charged with $-V_{DD}$ and V_{DD}, respectively. Therefore the potential difference of $4V_{DD}$ is made up across the capacitor Cp.

When the switch SWA and SWB' are in the on state, the voltage at the node X1 is $-2V_{DD}$ due to the voltage charged across the capacitors C2 and the supply voltage. And the voltage is $2V_{DD}$ at the node X2 due to the voltage charged across the capacitors C3 and the supply voltage. At that time the capacitors C1 and C4 are charged with V_{DD} and $-V_{DD}$, respectively. Therefore the potential difference of $4V_{DD}$ is made up across the capacitor Cp. If the supply voltage, V_{DD}, is 40 volts the potential difference is about 160volts across the capacitor Cp.

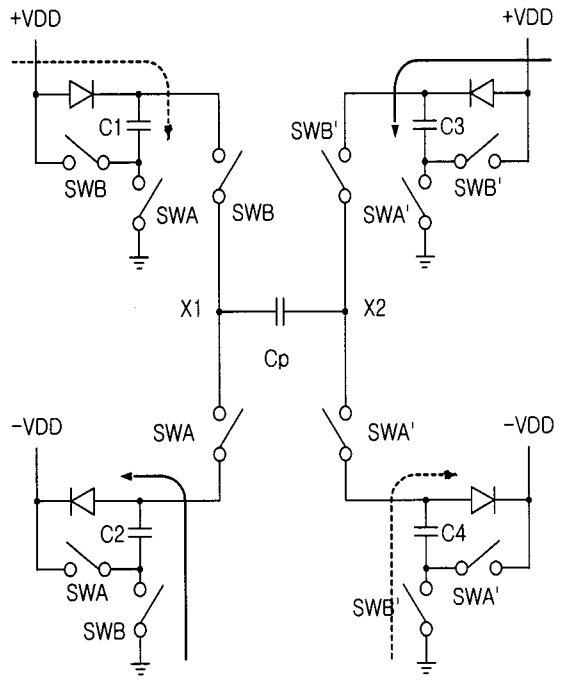

Fig. 2 The operation of driving circuit with switch on and off

III. SIMULATION RESULTS

Fig. 3 shows the voltage across capacitor Cp with the supply voltage which is simulated by PSPICE. From Fig. 3 the voltage across capacitor Cp is about 152volts when the supply voltage is 40volts. Therefore the PDP cells can be enough driven when the supply voltage is over 40volts.

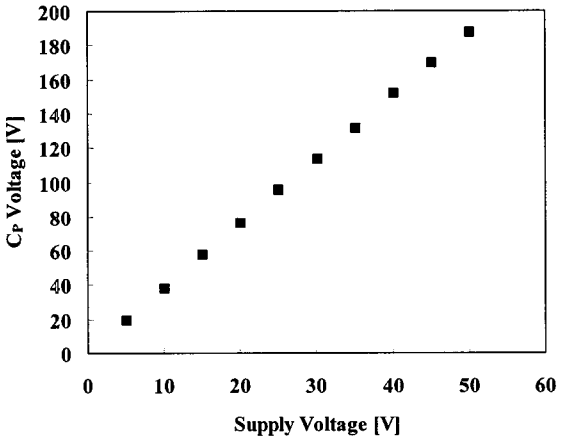

Fig. 3 The voltage across capacitor Cp with the supply voltage

The proposed circuit has an advantage which the lower supply voltage can be used compared to the conventional driving circuit. Also the power consumption can be obviously reduced because the supply voltage is decreased. And the devices are used with low operating voltage.

Fig. 4 (a) shows the input pulse to control switches SWA and SWB and Fig. 4(b) shows input pulse to control switches SWA' and SWB'.

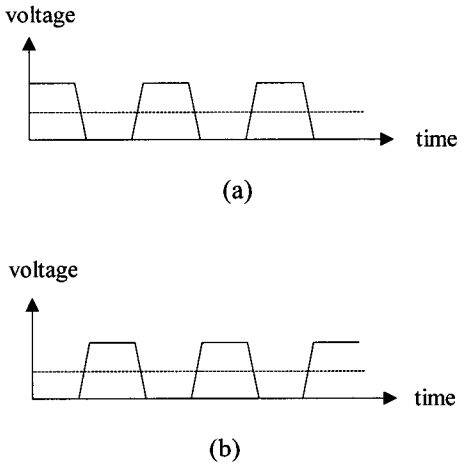

Fig. 4 Input pulses to control switches
(a) input pulse to control switches SWA and SWB
(b) input pulse to control switches SWA' and SWB'

In Fig. 4 both transistors of NMOS and PMOS are momentarily turned on during transition, resulting in a pulse of current drawn from the power supply.

Thereby the power consumption increases.

Fig. 5(a) shows the input signals to control the switches when the rising and falling times of the input pulse are 1μsec and Fig. 5(b) shows the power consumption with t_{gap}. P_{tgap0} is the power consumption when t_{gap} is zero and P_{tgap} is the power consumption when t_{gap} is non-zero. When t_{gap} is 1μsec the power consumption is dramatically decreased because there is no current flow from the V_{DD} to ground. In the proposed circuit t_{gap} is controlled to reduce power consumption.

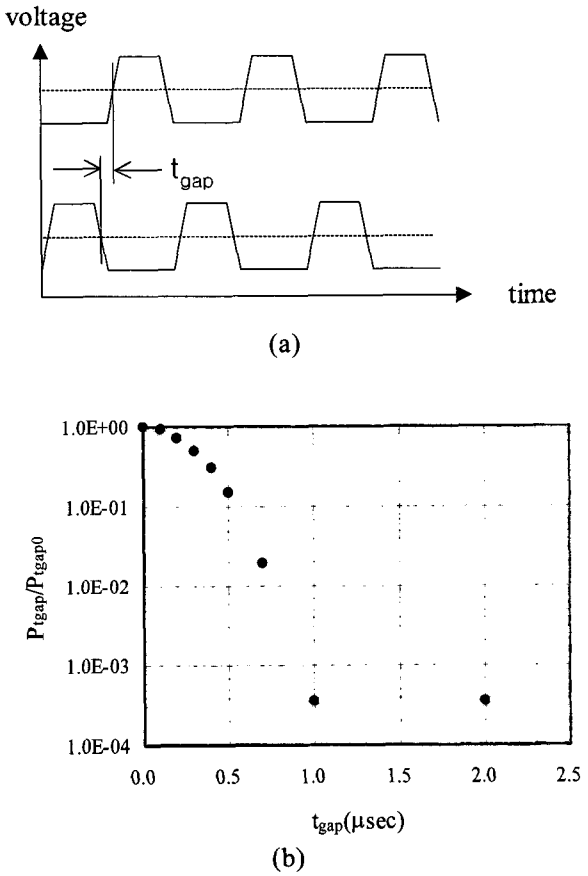

Fig. 5 Input signals to apply MOS switches and power consumption with t_{gap}
(a) input signals to apply MOS switches
(b) power consumption with t_{gap}

IV. EXPERIMENTAL RESULTS

The experiments are carried out by using Fig. 1, NMOS switch is used IRF-630 and PMOS switch is used IRF-9630. Table 1 shows the characteristics of NMOS and PMOS power transistors.

Fig. 6(a) shows the input pulses to control NMOS and PMOS switches and t_{gap} exists to reduce power consumption. Fig. 6(b) shows the experiment result which is the voltage between node X1 and node X2. As shown in Fig. 6(b), we can observe that the potential difference over 150V is produced across the capacitor between the node X1 and node X2.

Table 1 The Characteristics of NMOS and PMOS power transistors used in experiments

NMOS IRF-630	V_{DSS} : 200volts
	I_{DSAT} : 9A
	$R_{DS\ ON}$ <0.4Ω
PMOS IRF-9630	V_{DSS} : 200volts
	I_{DSAT} : 9A
	$R_{DS\ ON}$ <0.8Ω

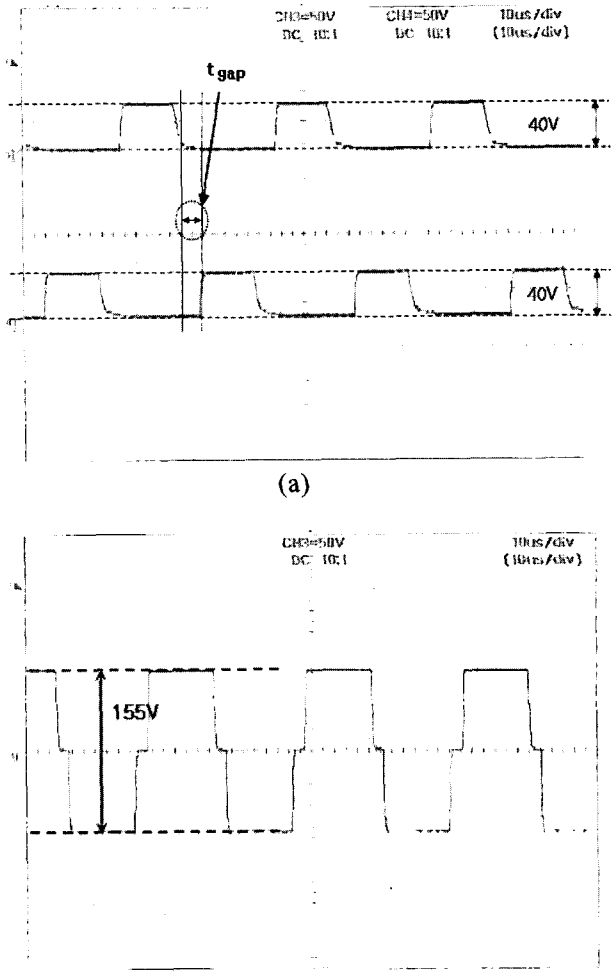

Fig. 6 Input signals to apply MOS switches and voltage waveform in capacitor Cp
(a) input signals to apply MOS switches
(b) voltage waveform in capacitor Cp

V. CONCLUSIONS

In this paper, a driving circuit for AC-type PDP with lower supply voltage than the supply voltage of the conventional circuit is proposed. The operation of proposed circuit is confirmed by the PSPICE simulation and experiments. From the simulation and experiment results when the supply voltage is over 40volts the enough driving voltage can be obtained to drive PDP cells. And the power consumption is simulated with t_{gap}. When t_{gap} is over the rising time and falling time the

power consumption is dramatically reduced. The features of the proposed circuit are as follows; (a)the power consumption can be decreased by the use of low supply voltage and input signals with t_{gap}, (b)the driving circuit for AC-type PDP can be implemented by the use of electrical devices with low operating voltages.

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