Electrical Properties of CuPc FET with Different Substrate Temperature

Ho Shik Lee and Yong Pil Park
Department of Hospital Biomedical Engineering, Dongshin University, 252 Daeho-dong, Naju-si, Jeonnam 520-714, Korea

Min Woo Cheon[a]
Department of Medicine, Chosun University, 375 Seoseok-dong, Dong-gu, Gwangju 501-759, Korea

[a]E-mail : ccuccu7@lycos.co.kr

(Received July 5 2007, Accepted August 19 2007)

Organic field-effect transistors (OFETs) are of interest for use in widely area electronic applications. We fabricated the organic field-effect transistor based a copper phthalocyanine (CuPc) as an active layer on the silicon substrate. The CuPc FET device was made a top-contact type and the substrate temperature was room temperature and 150 ℃. The CuPc thickness was 40 nm, and the channel length was 50 μm, channel width was 3 mm. We observed the typical current-voltage (I-V) characteristics and capacitance-voltage (C-V) in CuPc FET and we calculated the effective mobility with each device. Also, we observed the AFM images with different substrate temperature.

Keywords : CuPc, Organic field-effect transistor(OFET), Effective mobility, Current-voltage characteristics(I-V), Capacitance-voltage characteristics(C-V)

1. INTRODUCTION

Organic semiconductors have recently been used as active layers in electronic devices such as field-effect transistors (FETs), photovoltaic solar cells, and light-emitting diode (OLED)[1]. The mechanism of carrier transport in organic semiconductors is one of the most important research subjects to be elucidated for improving of the device performance[2-4]. The CuPc materials are well known to show excellent semiconductor performance and have been studied for the use as organic field-effect transistors (OFET). Until now much experimental efforts, such as modification of the film quality, has been devoted to improve the device performance[5,6].

In the present paper, we show the I-V, C-V characteristics and AFM images to understand the carrier transport and the effect of the substrate temperature in CuPc FET.

2. EXPERIMENTALS

Figure 1 shows a molecular structure and the device structure of the top-contact CuPc FET. The CuPc FET was fabricated using the silicon substrate and the UV/ozone treatment for 30 min with oxygen gas before deposition of the CuPc material.

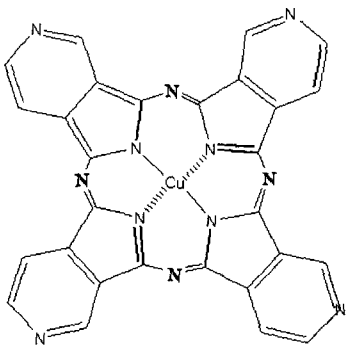
The CuPc was deposited on the substrate by thermal evaporation method with a deposition rate of 0.5 Å/s in 10^{-7} torr. The channel length (L) and width (W) were 50 μm and 3 mm, respectively.

The I-V and C-V characteristics were carried out in an ambient condition by using a source-meter (Keithley type-2400) and LCR meter (Hioki type-3522-50)[3,4].

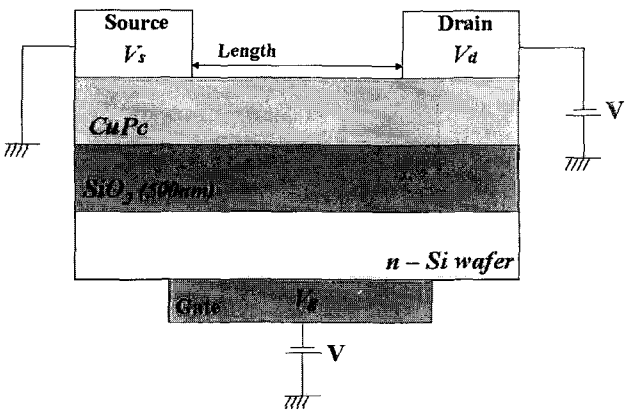
The AFM image measurement was carried out with bulk CuPc thin film on the silicon substrate with different temperature as room temperature and 150 ℃.

3. RESULTS AND DISCUSSION

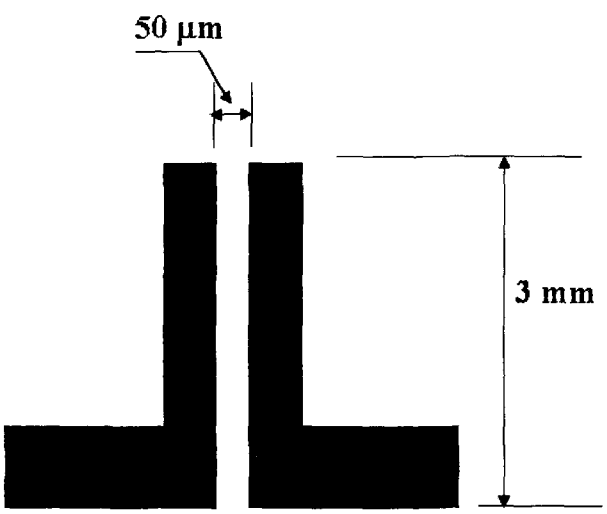
Figure 2 shows the AFM images of the bulk CuPc thin film surface with difference substrate temperature at room temperature and 150 ℃. From the AFM images we could observe the surface characteristics of the CuPc organic thin film. We were guessed that the CuPc materials were layered to parallel with the substrate and we could observe clearly the CuPc grain. Using the 150 ℃



(a) Molecular structure



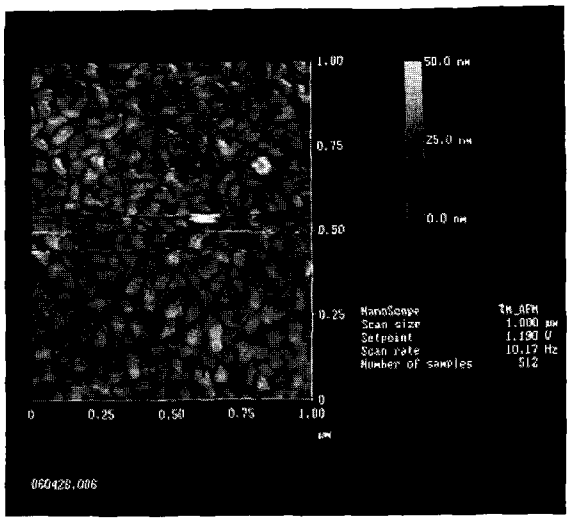
(b) Device structure (side view)



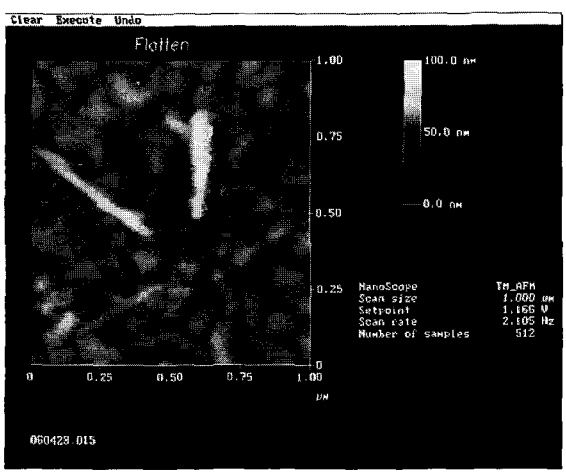
(c) Device structure (top view)

Fig. 1. Device and molecular structure of the CuPc FET.

substrate, the CuPc grain was more than larger and also we observed the line-fiber from the CuPc film surface. Some researchers were reported that we could observe an phase transition and line-fiber of the CuPc film from the changed the substrate temperature[10].



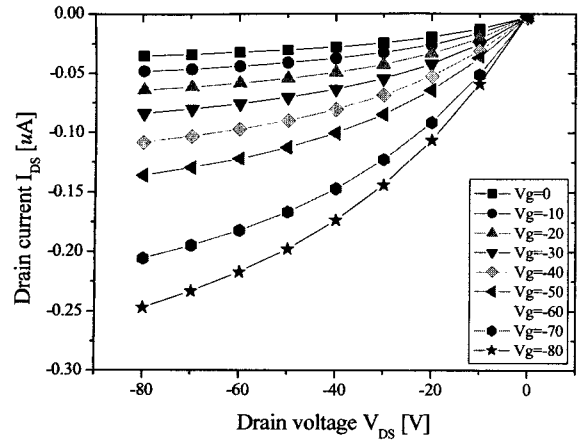
(a) room temperature CuPc thin film surface



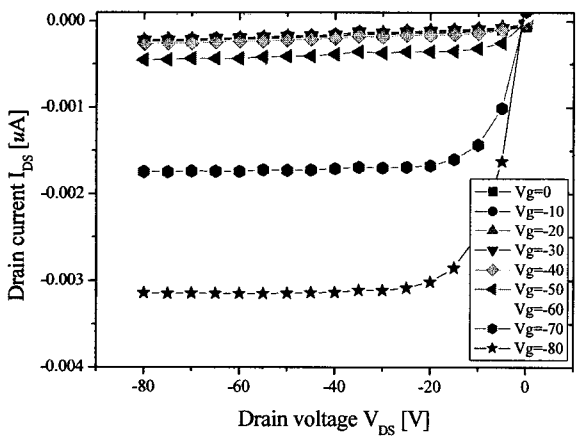
(b) 150 ℃ CuPc thin film surface

Fig. 2. AFM images of the bulk CuPc thin film surface with difference substrate temperature.

Figure 3 shows the I-V characteristics of the CuPc FET with difference substrate temperature such as room and 150 ℃. Figure 3 shows the typical FET characteristics and using the 150 ℃ substrate we observed more than faster saturated region of the CuPc FET. And we were calculated the field-effect mobility of 1.2×10^{-5} cm^2/Vs with 150 ℃ substrate and 1.2×10^{-4} cm^2/Vs with room temperature substrate of the CuPc FET. The field-effect mobility of the 150 ℃ substrate CuPc FET was very low more than room temperature substrate CuPc FET. The reason is maybe the CuPc bulk property was changed by heating (see Fig. 2(b)) such as line-fiber and more than larger grain size from the AFM image Fig. 2(b). The electrical conductivity was depended on grain orientation and the substrate temperature of the CuPc material[10].

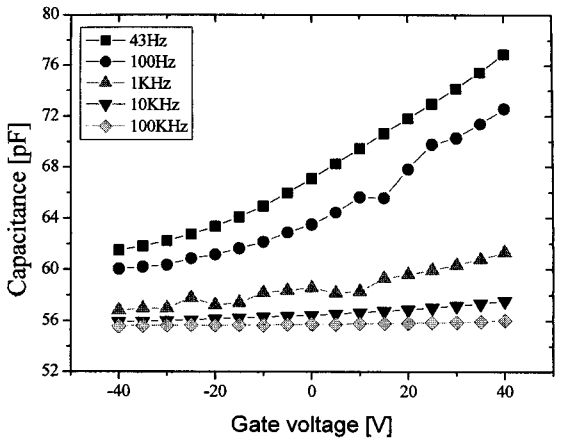


(a) Room temperature substrate

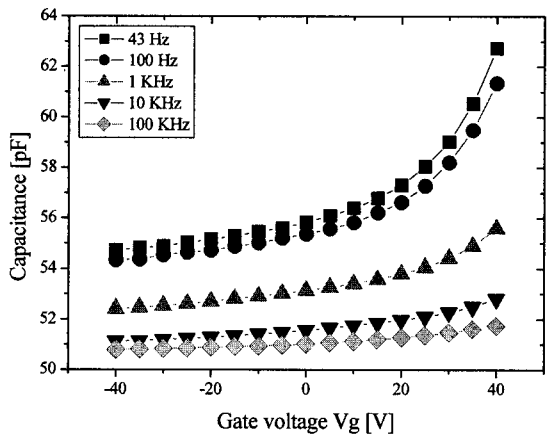


(b) 150℃ substrate

Fig. 3. I-V characteristics of the CuPc FET with difference substrate temperature.



(a) Room temperature substrate



(b) 150℃ substrate

Fig. 4. C-V characteristics of the CuPc FET with difference substrate temperature.

Figure 4 shows the capacitance-voltage (C-V) characteristics of the CuPc FET with difference substrate temperature such as room temperature and 150 ℃. Also, we applied the varying frequency 43, 100, 1 K, 10 K and 100 K [Hz] to the CuPc FET for the capacitance measurement. The capacitance of the room temperature substrate CuPc FET was approached about 78 pF, and the 150 ℃ substrate CuPc FET was reached about 63 pF. The capacitance of the CuPc FET with different substrate temperature was not so much changed.

4. CONCLUSION

The top-contact CuPc FET using the different substrate temperature such as room temperature and 150 ℃ were fabricated. We observed the more than larger grain size from the AFM image at 150 ℃ substrate CuPc FET. Also, we were measured the electrical characteristics of the CuPc FET, we observed the electrical conductivity was depended on grain orientation and the substrate temperature of the CuPc material. From the C-V characteristics, the capacitance of the CuPc FET was not so much changed with the substrate temperature.

ACKNOWLEDGMENTS

This work was supported by the Korea Research Foundation Grant funded by the Korean Government (MOEHRD)(KRF- 2005-214-D00287).

REFERENCES

[1] E. Lim, T. Manaka, R. Tamura, and M. Iwamoto, "Maxwell-wagner model analysis for the capacitance-voltage characteristics of pentacene field effect transistor", Jpn. J. Appl. Phy., Vol. 45, p. 3712, 2006.

[2] T. Manaka, E. Lim, R. Tamura, and M. Iwamoto, "Modulation in optical second harmonic generation signal from channel of pentacene field effect transistors during device operation", Appl. Phys. Lett., Vol. 87, No. 222107, p. 222107-1, 2006.
[3] T. Manaka, E. Lim, R. Tamura, and M. Iwamoto, "Control of the nano electrostatic phenomena at a pentacene/metal interface for improvement of the organic FET devices", Thin Solid Films, Vol. 499, p. 386, 2006.
[4] C. R. Kagan and P. Andry, "Thin-Film Transistors", Marcel Dekker, Inc, New York, p. 333, 2003.
[5] Z. Y. Cui, N. S. Kim, H. G. Lee, and K. W. Kim, "Effect of channel length in LDMMOSFET on the switching characteristics of CMOS inverter", Trans. EEM, Vol. 8, No. 1, p. 21, 2007.
[6] H.-N. Lee, Y. G. Lee, I. H. Ko, S. K. Kang, S.-E. Lee, and T. S. Oh, "Passivation layers for organic thin-film transistors", Trans. EEM, Vol. 8, No. 1, p. 36, 2007.