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EER 구조의 응용과 PBG를 이용한 고효율, 고선형성 Class-F 전력 증폭기

(A Highly Linear and Efficiency Class-F Power Amplifier using PBG and application EER Structure)

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요 약

본 논문에서는 class-F 전력 증폭기의 높은 선형성과 고효율을 얻기 위해 PBG구조와 EER (Envelope Elimination and Restoration) 구조를 적용하였다. class-F급 전력 증폭기의 효율을 개선시키기 위해 EER 구조의 포락선 검파기를 응용하여 전력 증폭기의 구동 전력을 조절하였다. 또한 PBG 구조를 class-F 전력증폭기의 출력단에 적용함으로써 정합회로의 비정합에 의한 고조파 성분들을 제거하여 높은 선형성을 얻었다. 본 논문에서 제안한 PBG 구조의 응용과 EER 구조를 응용한 전력 증폭기 구조는 적응형 바이어스를 이용한 Doherty 전력 증폭기에 비해 PAE가 34.56% 개선되었고 일반적인 Doherty 증폭기에 비해 3^{rd} IMD가 -10.66 dBc 이상 개선되었다.

Abstract

In this paper, the Power Added Efficiency (PAE) and linearity of class-F PA has been improved by using the PBG structure and the application of EER structure, simultaneously. The adaptive bias control circuit has been employed to improve the PAE through the application of EER structure. The PBG structure has been adapted for improving the Linearity by suppressing the harmonics on the output of amplifier. The PAE and the 3rd Inter-Modulation Distortion (IMD) has improved 34.56%, 10.66 dB, compared with those of the conventional Doherty amplifier, respectively.

Keywords: EER, PBG, Class-F PA, PAE, IMD

I. Introduction

The effort to maximize the efficiency of power amplifier has been made from early communication system up to now in various kinds of forms. Especially, now it has become more important in fast change to personal unit centered on hand-set. Recently becoming multi-band (WCDMA, Wibro) of unit to give good service has been needed, so it is sure that the durability of unit battery is another issue[1-2].

There are many kinds of methods to improve the efficiency of power amplifier. : Doherty amplifier has been improved PAE by only operating main amplifier at low input power level and both operating main amplifier and peaking amplifier at high input power level[3], switched gain stage has been improved PAE by operating each difference power amplifier according to input power level[4], adaptive bias controller has been improved PAE by controlling bias

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condition according to input power level[5]. But these methods have been not good in the characteristics of linearity because these are designed focused on efficiency.The PBG structure has had the characteristics of broad band filter and this stop band filter has removed the harmonics of output signals [6-8]. EER structure by Kahn has consisted of structure that detects envelope of RF signal using class-S modulator and as the result of it controls drain voltage[9]. This structure has a good point to maximize efficiency, but it also has a weak point with time delay and complication of circuit.

In this paper, the envelope detector has detected the amplitude of input signal applying structure. The PAE has been increased by controlling the dynamic power using envelope detector. The adaptive structure has been applied to EER to make structure simple and to minimize time delay.

Ⅱ. Adaptive bias control circuit and PBG design

$$PAE = \frac{P_{out} - P_{in}}{(V_{gs} \times I_{gs}) + (V_{ds} \times I_{ds})} \tag{1}$$

Fig. 1. shows that there are the methods increasing output of converting quiescent point (Q-point) of power amplifier to improve PAE. There are three ways to convert Q-point as Fig 1 above. For example, there are waysto convert drain or gate, or way to convert drain and gate simultaneously. But, because substantially it is difficult to control both

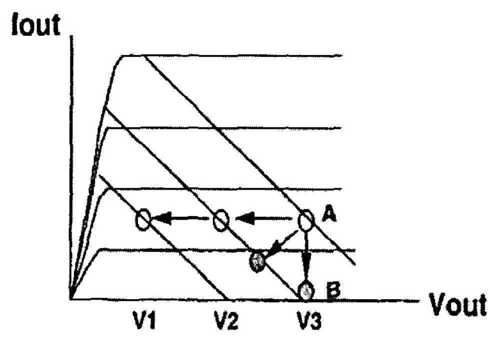


그림 1. RF 부하선과 적응형 DC 바이어스점

Fig. 1. RF load line and Various DC Bias point.

voltages simul-taneously, in common only one between the two is used as the way to control.

PBG structure forms stop band focused on frequency corresponding to the period of lattice, 2Λ. Using the principle of this PBG structure, wanted stop band can be formed. The period of lattice, Λcan be expressed as the formula below.

$$\Lambda = \lambda_g / 2 \tag{2}$$

At this point, λ_g is a wavelength of wave exposed from microstrip line structure. It is produced by effective per-mittivity and center frequency of wanted stop band.

$$\lambda_g(f) = \frac{v_p(f)}{f} = \frac{C}{f\sqrt{\mu_r \epsilon_{r,eff}(f)}} \tag{3}$$

Where f means center frequency of wanted stop band, and $\epsilon_{r,eff}(f)$ means an effective permittivity that center frequency of stop band in micro-strip structure has.

In generally, when it make the period of lattice Λis fixed and width W is increased, stop band moves to low frequency band. But if its width is increased excessively, the ripple of through band will be increased, and be met with a loss.

The fundamental, 2nd and 3rd harmonics of S21 has been -0.00027 dB,-1.12 dB, and -22.49 dB, respectively.

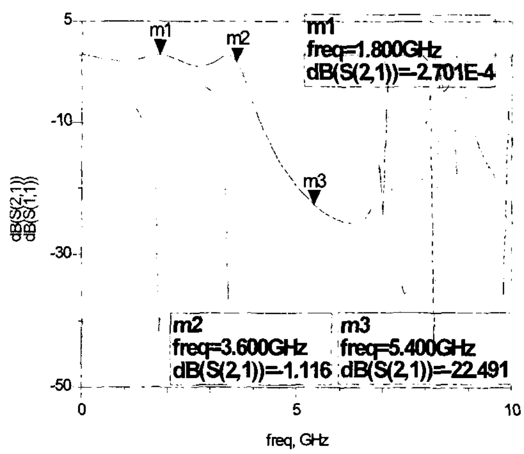


그림 2. HFSS를 이용한 PBG구조의 S-parameter 특성

Fig. 2. Characteristic of S-parameter of PBG Structure using HFSS.

Ⅲ. Class-F Power Amplifier Design

1.8GHz class-F power amplifier has been designed using load-pull matching technique with FET MRF281SR1.

The condition for DC bias of MRF281SR1 at 1.8GHz has been designed and simulated in Q-point that Vds is 26 V and Vgs is 3.4V.

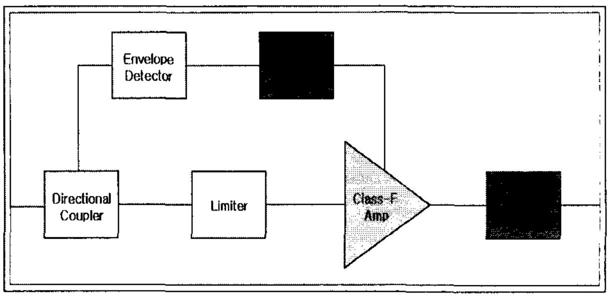
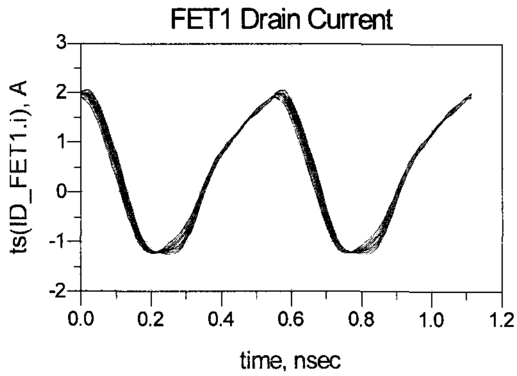
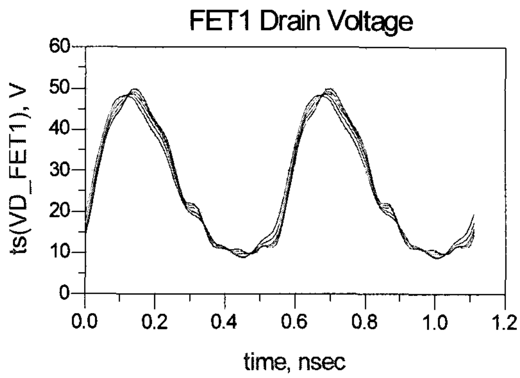


그림 3. EER 구조와 PBG 구조를 이용한 제안된 전력 증폭기 구조

Fig. 3. Proposed Power Amplifier Structure using EER and PBG Structure.



(a) Drain Current



(b) Draing Voltage

그림 4. Class-F급 전력증폭기의 Drain 전압과 전류 파형

Fig. 4. Drain Voltage and Current of Class-F PA.

Also, it is confirmed through 1 dB compression simulation, input value, P1dB has been 21dBm. To get maximum output power at this input value, the

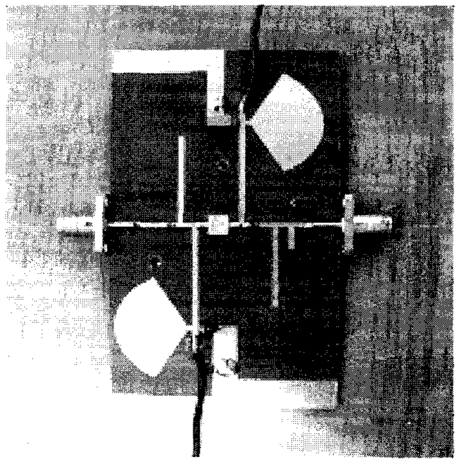
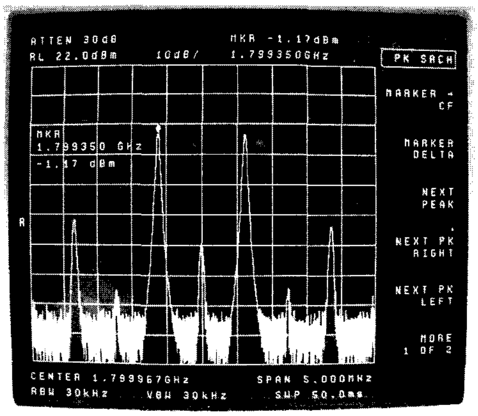
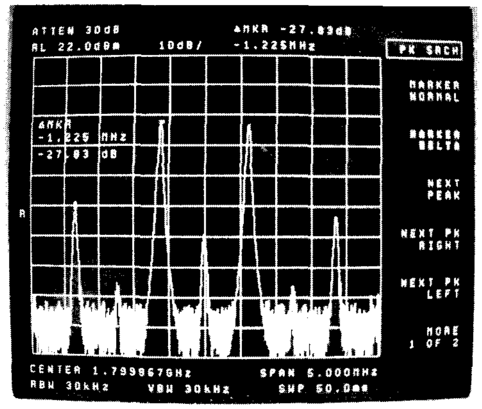


그림 5. Class-F급 전력증폭기 제작 기판

Fig. 5. Fabrication of Class-F PA.



(a) Output Power



(b) 3rd IMD

그림 6. Class-F급 전력증폭기의 출력전력 및 3차 IMD 측정치

Fig. 6. Measurement of Output Power and 3rd IMD in Class-F PA.

maximum power impedance point through load-pull simulation has been taken. The output matching in class-F has been designed with shortening 2nd harmonic and opening 3rd harmonic at maximum power impedance point.

Fig. 3. shows block diagram of power amplifier in class-F using EER and PBG structure. Fig. 4. shows the characteristics of drain current and drain voltage of class-F power amplifier. Fig. 5. shows actually fabricated the layout in class-F power amplifier. Fig. 6. shows measurement value of output power and 3rd IMD for fabricated class-F power amplifier.

The fabricated class-F power amplifier is optimized to 26V in drain voltage, and its input power has been 20 dBm. The output power and 3rd IMD has been 32.83 dBm/2tone and -27.93 dBc, respectively.

The maximum efficiency of power amplifier in class-F is 100% theoretically. Fig. 4. shows that the maximum power efficiency has been 63% due to the leakage of the drain current.

The proposed EER structure has been designed using fabricated class-F power amplifier. The drain voltage has been supplied by changed DC voltage which has been detecting envelope of input signal. The drain voltage has been swing from 25V up to 27V as every 0.25V range. Fig. 7. shows fabricated substrate using both the adaptive bias controller and the PBG structure proposed. Fig. 8. shows

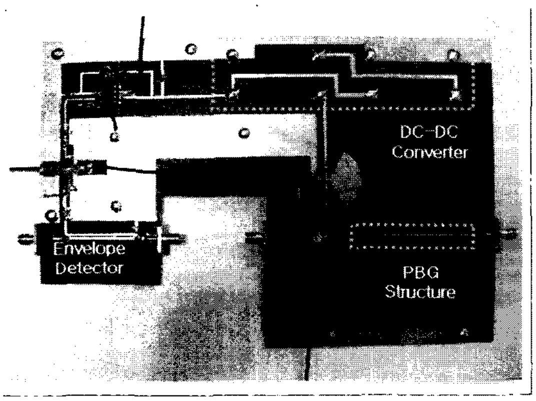


그림 7. 적응형 바이어스와 PBG 구조를 적용한 EER 구조

Fig. 7. EER Structure with Adaptive control bais & PBG Structure.

measurements value of both output power and 3rd IMD. The output power, 3rd IMD and PAE has been 32.43 dBm/2tone, -40.66 dBc and 66.48 %. Fig. 9. shows characteristic graph of output power, 3rd IMD and PAE according to the changing of drain voltage from 25V to 27V.

When the drain voltage has been fixed at 26V, its output result has been compiled in table 1. about proposed EER structure using adaptive bias and Doherty structure made in MRF281SR1.

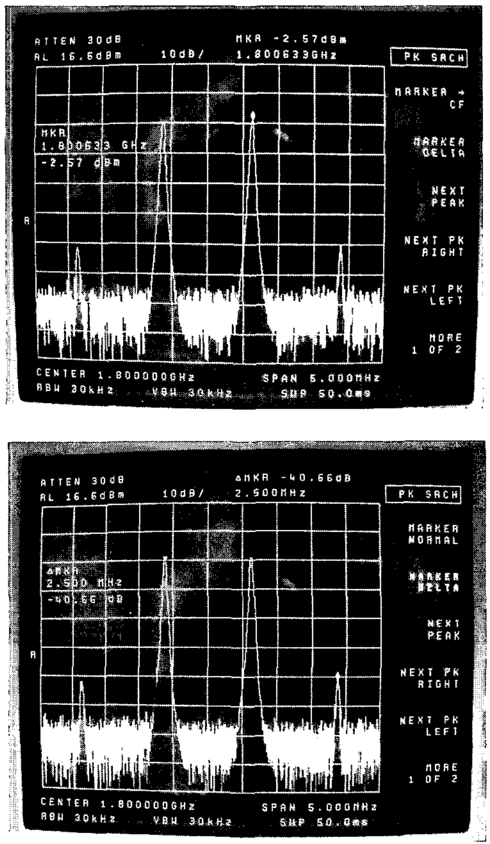


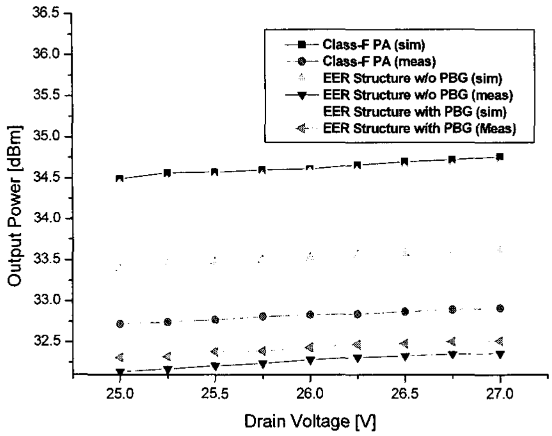
그림 8. 적응형 바이어스를 적용한 EER 구조의 출력전력 및 3rd IMD 측정치

Fig. 8. Measurement of Output power and 3rdIMD in EER with Adaptive control bias.

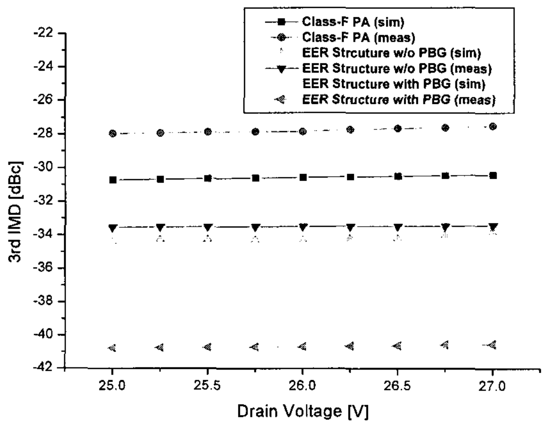
표 1. V_{ds}=26V에서 Doherty 전력 증폭기와 제안된 구조의 각 특성 비교

Table. 1. Caparison of each Characteristic in Doherty Amp and Proposed Power Amp at V_{ds}=26V.

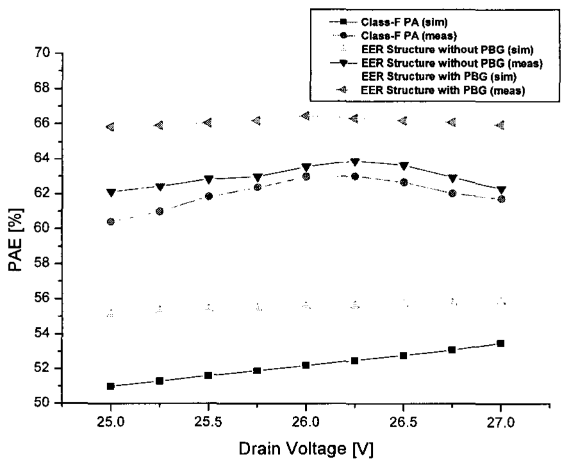
@ V_{ds} = 26V	Doherty PA	EER using Adaptive
출력 전력 (dBm)	32.86	32.43
3rdIMD (dBc)	-30	-40.66
PAE (%)	31.92	66.48



(a) Output Power (dBm)



(b) 3rd IMD (dBc)



(c) PAE (%)

그림 9. Drain Voltage에 따른 출력전력, 3rd IMD, PAE 의 특성 그래프

Fig. 9. Characteristic graph of Output power, 3rdIMD and PAE according to the changing of Drain voltage.

IV. Conclusion.

In this paper, the envelope detector has detected the amplitude of input signal applying structure. The PAE has been increased by controlling the dynamic power using envelope detector. The PBG structure has been employed on output of amplifier to remove of 3rd harmonic component. The PAE and 3rd IMD has been improved 34.56% and -10.66 dB compared with those of the conventional Doherty amplifier, respectively.

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