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포락선 검파를 통한 이중 바이어스 조절과 PBG를 이용한 도허티 증폭기 전력효율과 선형성 개선

(Research on the Improvement of PAE and Linearity using Dual Bias Control and PBG Structure in Doherty Amplifier)

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요 약

본 논문에서는 이중 바이어스 조절과 PBG 구조를 이용하여 Doherty 증폭기의 효율과 선형성을 개선하였다. PBG 구조를 출력 정합회로에 구현하였으며, 이중 바이어스 조절을 Carrier Amplifier에 적용하여 낮은 입력레벨에서도 Doherty 증폭기의 효율을 개선 할 수 있었다. 제안된 구조를 이용한 Doherty 증폭기는 기존의 전력증폭기에 비해 PAE는 8 %, IMD3는 -5 dBc 개선하고, 모든 입력전력레벨에서 30 % 이상의 고효율을 가질 수 있었다.

Abstract

In this paper, the PAE (Power Added Efficiency) and the linearity of the Doherty amplifier has been improved using dual bias control and PBG (Photonic BandGap) structure. The PBG structure has used to implement on output matching circuit and dual bias control has applied to improve the PAE of the Doherty amplifier at a low input level by applying it to a carrier amplifier. The Doherty amplifier using the proposed structure has improved PAE by 8% and 5dBc of IMD3 (3rd Inter-Modulation Distortion) compared with those of the conventional class AB amplifier. In addition to, it has been evident that the designed the structure has showed more than a 30% increase in PAE for flatness over all input power level.

Keywords : Dual bias control, Doherty amplifier, power added efficiency, power amplifier, PBG

I. Introduction

The significance of high-output amplifiers in wireless communication has been emphasized due to the rapid distribution of mobile communication systems. The current HPA require high power added efficiency and linearity[1]. In a solution for the linearity of conventional power amplifiers, various methods, such as back-off, feedback, predistortion, feedforward, and PBG, have been used. Among these methods, feedforward and predistortion methods have exhibited the disadvantage of requiring additional elements. Thus a PBG based method has been used to implement linearization[2, 3]. In general, a Doherty amplifier has used two different classes of amplifiers in which if a main amplifier is designed as an class-A or class-B amplifier, an auxiliary amplifier will be applied as a class-B or class-C amplifier. In the case of the class-B and class-C amplifier, they may have a linearity problem. Furthermore, a class-A and class-AB amplifier in Doherty amplifier increase distortion elements due to saturation because the input

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signal in the operation of a class-B,-C amplifier is high. Thus a Doherty amplifier has exhibited problems in linearity although it improves the power added efficiency[4 6].

There are three kinds of using bias control to obtain high PAE in HPA[7 9]. This paper has implemented a DC voltage control for drain and gate and PBG structure on the output matching circuit of a Doherty amplifier. The circuit has been based on a dual bias control method under the conditions that a class-A or class-AB carrier amplifier had certain degradations in linearity due to saturation when a class-B or class-C peaking amplifier was operated. It is possible to improve the problem of the PAE and the IMD_3 in the power amplifier and characteristics occurring in non-linearity simultaneously. In addition, there is a possibility that it may improve performance by more than 32% on all bandwidth for input signals.

Ⅱ. Theory and design of dual bias control

PAE can be expressed as Eq. (1)

$$PAE = \frac{(RF_{outputpower}) - (RF_{inputpower})}{(V_{gs} \times I_{gs}) + (V_{ds} \times I_{ds})} \tag{1}$$

In this paper, both voltages of gate and drain have been controlled by input power level. This paper has been used a dual bias control circuit that controlled both drain and gate voltages in which an envelope detector using an AD8313 Analog Device with an excellent linearity and temperature insensitivity.

As shown in Fig. 2, although the output voltage

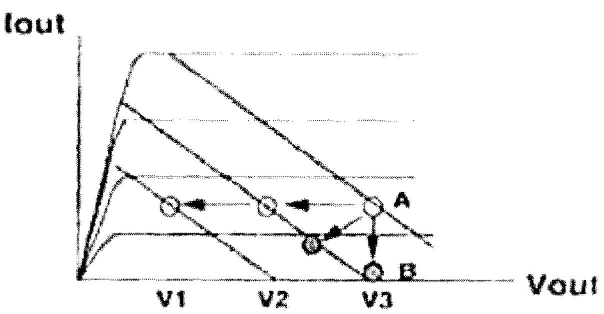

그림 1. RF 부하선과 DC-바이어스 점

Fig. 1. RF load line and various DC-bias points.

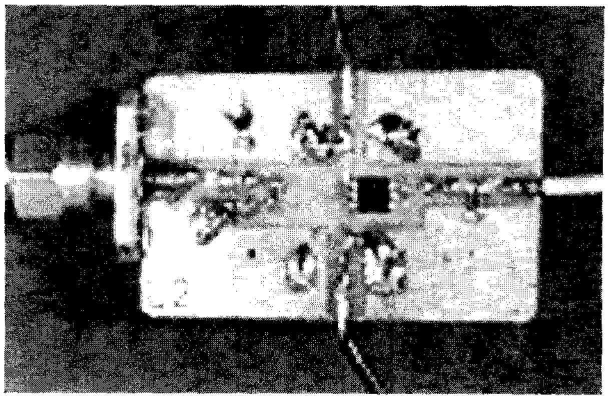

그림 2. AD8313을 이용한 포락선 검파기

Fig. 2. Envelope detector circuit using AD8313.

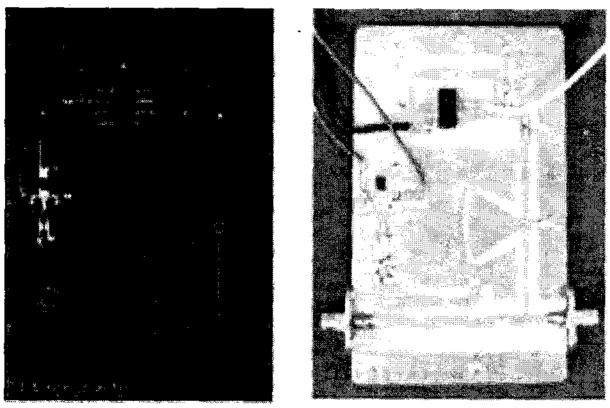

그림 3. 이중바이어스 조절 회로

Fig. 3. Circuit diagram for the dual bias circuit.

(DC) was produced according to the scale of input signals (RF) through an envelope detector, the bias voltage was adjusted with OP-Amps. As shown in Fig. 3, corresponding to increasing in input power, a bias control circuit has been fabricated in this research using a directional coupler due to the decrease in the gate bias voltage value from a class-AB to class-B and finally class-C.

Ⅲ. Theory and design of PBG

Using a PBG structure, the forming of a stop band could be estimated based on the frequency that corresponded to 2Λ in the Bragg lattice principle[10]. It was possible to form a stop band at a desired point based on this PBG structure. The lattice phase Λ can be noted as Eq. (2)

$$\Lambda = \lambda_g / 2 \tag{2}$$

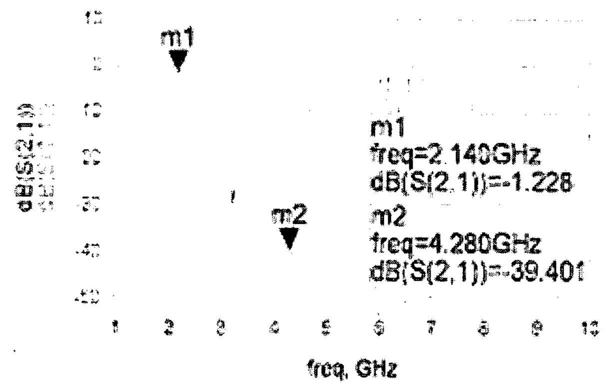

그림 4. PBG 시뮬레이션 결과

Fig. 4. Result of the PBG simulation.

where λ_g is the wavelength of the wave induced from a microstrip line structure and calculated using the effective permittivity and center frequency of a desired stop band as expressed as Eq. (3)

$$\lambda_g(f) = \frac{v_p(f)}{f} = \frac{c}{f\sqrt{\mu_r \varepsilon_{r,eff}(f)}} \tag{3}$$

where $\epsilon_{r,eff}(f)$ is the effective permittivity index of the center frequency of a stop band in a microstrip structure. HFSS by Ansoft has used as a simulation tool in order to design the PBG.

As shown in Fig. 4, the PBG was designed to obtain a minimum signal decreasing at a center frequency of 2.14GHz that was exhibited as S_{21} = -1.2dB. In addition, it was designed to obtain S_{21} = -39.4dB levels at a secondary harmonic frequency of 4.28GHz in order to decrease a harmonic frequency that affects the nonlinearity of HPA.

Ⅳ. Design of a Doherty amplifier using a dual bias circuit and PBG structure

Teflon board with a permittivity of 3.2 has been used in this research. In addition, ATF34143 of Agilent has been used in power amplifier. A loadpull simulation using ADS2005A was applied to determine an output matching point. Then, a Doherty amplifier has been designed using output matching according to this output matching point. Fig. 5 shows the implementation of an output matching circuit

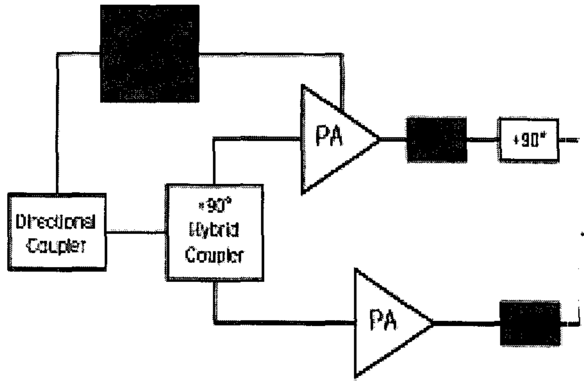

그림 5. 제안된 이중 바이어스와 PBG를 적용한 Doherty 전력증폭기 구조

Fig. 5. Structure of a Doherty amplifier using the proposed dual bias control circuit and PBG structure.

including the PBG in an offset-line when the output matching circuit was produced by determining the loadpull matching point of the power amplifier. Based on processes, a Doherty amplifier was designed to using the PBG in order to improve the linearity.

At first, a class-AB power amplifier has been designed as a reference amplifier in order to compare it with this research. As shown Fig. 6, an output power of 19.45dBm was obtained from the 1-tone measurement in this reference amplifier in which the power added efficiency and IMD_3 characteristic were 27.12% and -27.45dBc from 2-tone measurement, respectively.

This paper proposes a structure that improves the PAE of a Doherty amplifier by applying dual bias

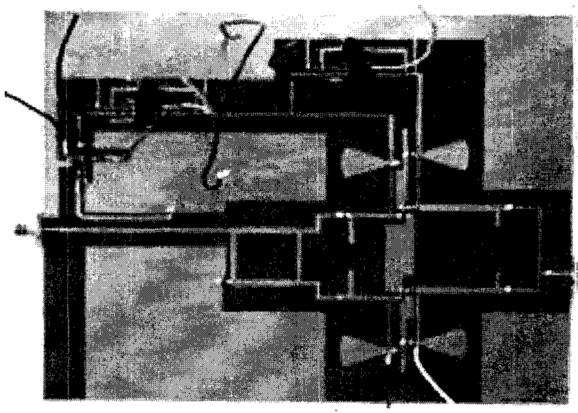

그림 6. 제안된 이중 바이어스와 PBG를 적용한 Doherty 전력증폭기

Fig. 6. Configuration of a Doherty amplifier using a dual bias control circuit and PBG structure.

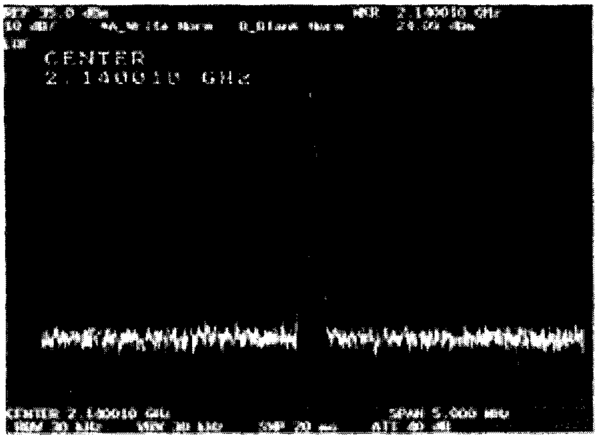

그림 7. 이중 바이어스 회로와 PBG 구조를 이용한 도허티 증폭기의 출력 전력

Fig. 7. Output power of the Doherty amplifier using a dual bias control circuit and PBG structure.

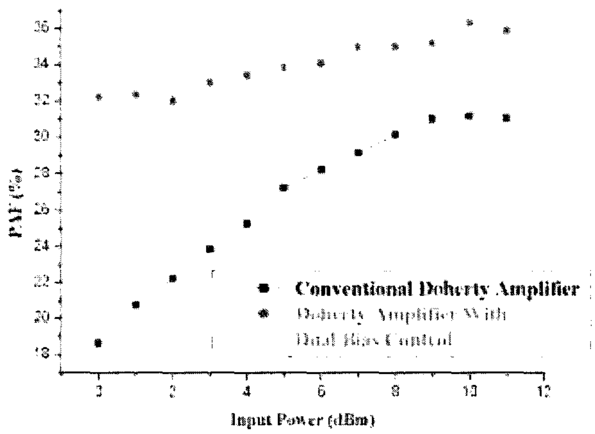

그림 8. 도허티 증폭기의 입력전력과 PAE 비교

Fig. 8. Input power vs PAE of the Doherty amplifier.

control circuit designed using operating amplifiers to control the bias voltage of an envelope detector based on a Doherty amplifier that uses the previously proposed PBG. Fig. 6 shows the fabricated Doherty amplifier using a dual bias control circuit and PBG structure.

DC voltages have been generated through an envelope detector corresponding to each input power level. The determined DC bias voltage has been applied to amplifier through OP-Amp to configure the bias voltage of gate and drain. In addition, linearity has been improved by removing the 2nd harmonic frequency using an additional PBG structure as an offset-line.

As shown in Fig. 7, the Doherty amplifier using the pro-posed dual bias control circuit and PBG structure exhibited an output of 24.09dBm, PAE of 36.25%, and IMD3 characteristic of -32.47dBc. Fig. 8 shows the comparison of the PAE of the conventional Doherty amplifier with that of the Doherty amplifier using the proposed dual bias control circuit and PBG structure. As shown in Fig. 8, the Doherty amplifier using the proposed dual bias control circuit and PBG structure showed a roughly 6% increase in output compared to that of the reference power amplifier.

In addition, this research has achieved the flatness in PAE for all input power level. It has been to obtain more than 30% PAE at low input power level with controlling dual bias point by changing the bias voltage of the gate and drain.

Table 1. shows the voltage variation in gate and drain bias voltage corresponding to the input power level with a value 0 to 10dBm. Table 2. notes the comparison between output power, PAE and IMD_3 for each power amplifier

표 1. 입력전력에 따른 바이어스 전압 변화

Table 1. Bias voltage variation according to the input power.

	Bias Voltage	Input power Level
Gate	0V~0.5V	0~10dBm
Drain	2V~4V	

표 2. 각 증폭기의 측정치 비교

Table 2. Comparison of measured data for each power amplifier.

	Reference (class-AB)	Doherty (classical)	Doherty (with PBG)	Proposed Structure
Output Power (dBm)	19.45	21.14	22.24	24.09
PAE (%)	27.12	30.18	32.85	36.28
IMD_3 (dBc)	-27.45	-28.24	-31.84	-32.26

V. Conclusion

In this paper, the dual bias control and the PBG structure has been employed to improve the PAE and the linearity of the Doherty amplifier. The controlling of the gate and the drain bias voltage corresponding to input power level has been done to improve the PAE of the Doherty amplifier. The PBG structure has been employed on the output of the Doherty amplifier to improve the linearity. The PAE and the linearity has been improved 8% and 5dBc compared with those of the conventional class-AB power amplifier, respectively. Our Doherty amplifier has been very good flatness of output power over all input power range.

참 고 문 헌

[1] Steve C. Cripps, RF Power Amplifiers for wireless Communications, Artech House, 1999.

[2] T. S. Kim, and C. H. Seo, "A Novel Photonic Bandgap Structure for Lowpass Filter of Wide Stopband," IEEE Microwave Guided Wave Lett., January, 2000.

[3] I. Rumsey, P. M. Melinda and P. K. Kelly, "Photonic Bandgap Structures Used as Filter in Microstrip Circuits," IEEE Microwave Guided Wave Lett., vol.8, pp. 336-338, 1998.

[4] W. H. Doherty, "A New High Efficiency Power Amplifier for Modulated Waves," Proceeding of the IRE, vol. 24, no. 9, pp. 1163-1182, 1936.

[5] Upton, David M., and Maloney, Peter R, et al, "A Microwave Doherty Amplifier," Applied Microwaves and RF, Winter, 1994

[6] M. Iwamoto, "An extended Doherty amplifier with high efficiency over a wide power range," IEEE Trans. Microwave Theory Tech., vol. 49, pp. 2472-2479, December 2000.

[7] Adel. A. M. Saleh and Donald C. Cox, "Improving the Power Added Efficiency of FET Amplifiers Operating with Varying-envelop signals," IEEE Trans. Microwave Theory Tech, vol. MTT-31, pp. 51-57, January, 1983.

[8] G, Hanington, "High-Efficiency Power Amplifier Using Dynamic Power-Supply Voltage for CDMA Applications," IEEE Trans. Microwave Theory Tech., vol. 47, pp. 1471-1476, August 1999.

[9] P. B Kenington, High-Linearity RF Amplifier Design, Artech House, 2000.

[10] C. K. Chong et al., "Bragg reflectors," IEEE Trans. On Plasma Science, vol. 20, no. 3, pp. 393-402, 1992.

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