A 3.3-V Low-Power Compact Driver for Multi-Standard Physical Layer

Joon-Young Park, Jin-Hee Lee, and Deog-Kyoon Jeong

Abstract—**A low-power compact driver for multi-standard physical layer is presented. The proposed driver achieves low power and small area through the voltage-mode driver with trans-impedance configuration and the novel hybrid driver,. In the voltage-mode driver, a trans-impedance configuration alleviates the problem of limited common-mode range of error amplifiers and the area and power overhead due to pre-amplifier. For a standard with extended output swing, only current sources are added in parallel with the voltage-mode driver, which is named a 'hybrid driver'. The hybrid architecture not only increases output swing but reduces overall driver area. The overall driver occupies 0.14 mm^2. Power consumptions under 3.3-V supply are 24.5 mW for the voltage-mode driver and 44.5 mW for the hybrid driver.**

Index Terms—**Multi-standard driver, voltage-mode driver, trans-impedance configuration, hybrid driver**

I. INTRODUCTION

AS deep submicron processes are used in mixed-mode communication chips, designers of analog circuitry are faced with an unavoidable obstacle — low supply voltage, whereas designers of digital systems enjoys the benefits of high speed, small device size, and low power consumption. The reduction of supply voltage directly decreases the dynamic range of an output driver while several output drivers still require a large voltage swing to comply with the existing legacy standard. For example, a recent 1000BASE-T physical layer chip can support not only 1000BASE-T, but also 10BASE-T and 100BASE-TX [1-3]. For this purpose, this chip includes interface circuits for each specification because each of them needs different output signaling level. The driver is selected by multiplexer according to operation mode as depicted in Fig. 1. This architecture requires large area due to many drivers for their own specifications.

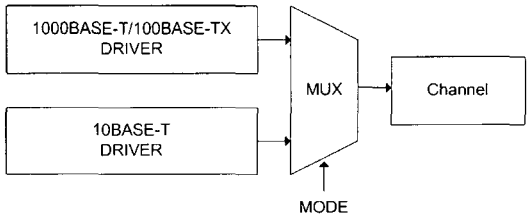

Fig. 1. Block diagram of multiplexed drivers for multiple signaling specifications.

This paper describes a low-power compact driver which is adequate for the application supporting multi-standard physical layer. Employment of a voltage-mode driver for small signaling output results in low power consumption; a new hybrid driver for large signaling reduces power consumption compared with a conventional current-mode driver. Furthermore, the overall chip area can be significantly reduced since the proposed hybrid driver can share many sub-blocks of a voltage-mode driver.

In the next section, two types of driver, a voltage-mode and a current-mode driver are compared in the point of power consumption. In section III, the proposed voltage-mode driver is described. Section IV describes a new hybrid driver. The realization and experimental results are discussed in section V. Finally, a conclusion is drawn.

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II. VOLTAGE-MODE DRIVER AND CURRENT-MODE DRIVER

Driver types can be classified into two categories, current- mode and voltage-mode depending on output impedance of a driver. To eliminate signal reflections at source, a current-mode driver employs a termination resistor connected in parallel. On the other hand, a voltage-mode driver uses a series termination resistor as shown in Fig. 2. Since a shunt configuration of a termination resistor requires additional current, a current-mode driver consumes larger power than a voltage-mode driver. However, minimum supply voltage of a voltage-mode driver is double of maximum output swing because it must accommodate the voltage drop across a series termination resistor.

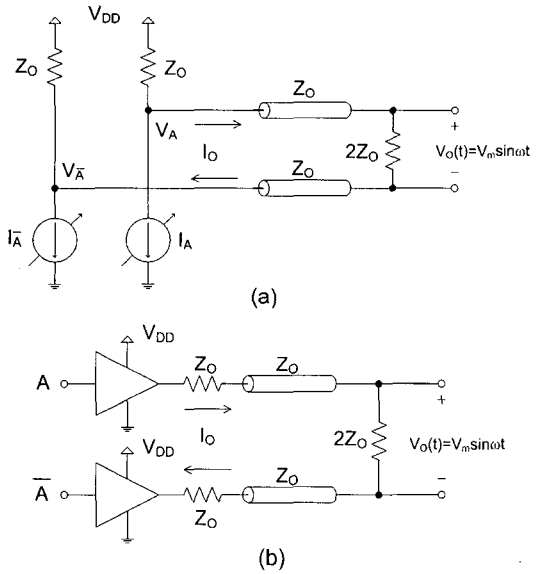

Fig. 2. Conventional (a) current-mode driver and (b) voltage-mode driver.

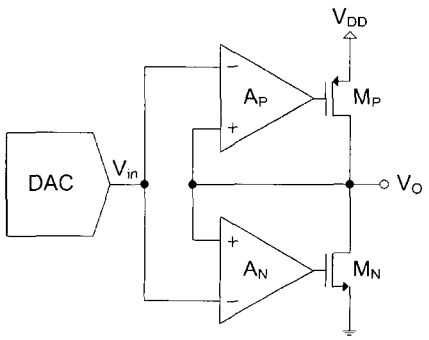

Fig. 3. Conventional pseudo-source amplifier.

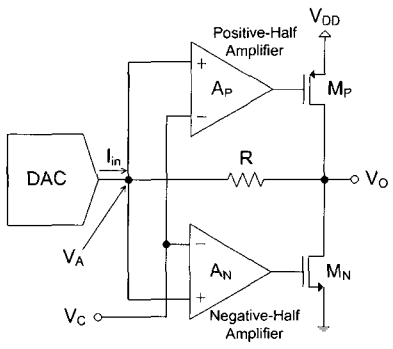

Fig. 4. Proposed voltage-mode driver.

When a sinusoidal wave $V_m \sin\omega t$, is launched to a transmission line with a current-mode driver and a voltage-mode driver, respectively, the power dissipation P_{avg} of each driver can be derived as follows.

In a differential current-mode driver, the output voltage V_A and $V_{\bar{A}}$ are determined as

$$V_A(t) = \left(V_{DD} - \frac{1}{2}V_m\right) + \frac{1}{2}V_m \sin\omega t$$
$$V_{\bar{A}}(t) = \left(V_{DD} - \frac{1}{2}V_m\right) - \frac{1}{2}V_m \sin\omega t \quad (1)$$

Total current of the current-mode driver and power consumption is

$$I_{tot}(t) = I_A + I_{\bar{A}} = \frac{V_{DD} - V_A}{Z_O} + \frac{V_{DD} - V_{\bar{A}}}{Z_O} = \frac{V_m}{Z_O}$$
$$P_{avg} = V_{DD} \cdot I_{tot} = \frac{V_{DD} \cdot V_m}{Z_O} \quad (2)$$

In case of a differential voltage-mode driver, load current I_O is determined with output voltage V_O and load resistance Z_O.

$$I_O(t) = \frac{v_O(t)}{2Z_O} = \frac{V_m}{2Z_O} \sin\omega t \quad (3)$$

Since load current originates from a voltage-mode driver, power consumption of the voltage-mode driver can be represented with load current I_O. Then, average power is

$$P(t) = V_{DD}|I_O(t)| = \frac{V_{DD} \cdot V_m}{2Z_O}|\sin\omega t|$$
$$P_{avg} = \frac{1}{2\pi}\int_{-\pi}^{\pi} P(t)dt = \frac{V_{DD} \cdot V_m}{\pi Z_O} \quad (4)$$

From (2) and (4), we can see that a voltage-mode driver consumes only 32% of the power of a current-mode driver. Thus, a voltage-mode driver may be a good solution for a low power application.

III. VOLTAGE-MODE DRIVER

Many conventional voltage-mode drivers employ a pseudo-source amplifier depicted in Fig. 3 as an output buffer for large signaling and low output impedance [4], [5]. When a current-steering DAC is employed for a multi-level application, a pseudo-source amplifier requires a current-to-voltage converter, generally implemented as a pre-amplifier. This results in additional area and power consumption. In addition, this architecture has the limited output voltage swing problem due to the limited input common-mode range of error amplifier. One solution to prevent this problem is increasing the size of the output transistors. Another solution is designing the improved version of an error amplifier [6], [7].

In this paper, the voltage-mode driver of trans-impedance configuration is proposed to resolve the above problems. In the conventional pseudo-source amplifier, error amplifiers and output transistors form the unity gain amplifier like Fig. 3. On the other hand, in the proposed voltage-mode driver, error amplifiers and output transistors form the inverting amplifier with a resistor R as depicted in Fig. 4. For the negative half of the output voltage swing, an amplifier A_N, a NMOS transistor M_N, and a resistor R form a negative feedback loop which makes the input voltage V_A to be a common-mode voltage V_C which is a half V_{DD}. Conversely, the positive half circuit is formed with A_P, M_P, and R. Since V_A is kept to V_C, the output voltage becomes $V_O=V_C-I_{in}\cdot R$, when the input current I_{in} is applied to the input node. This organization of the proposed driver utilizes a current input, which can minimize the power and area overhead of a pre-amplifier.

The amplifiers (A_N, A_P) in the proposed driver need to have a relatively low gain; otherwise, a typical input offset voltage of tens of mV will cause a huge change in the output quiescent current. Therefore, the gain is generally around 10 [8]. The circuit diagram of a negative-half amplifier is shown in Fig. 5. A positive-half amplifier is the dual of a negative-half amplifier. The amplifier is composed of a simple differential amplifier with an unbalanced current mirror (M_3, M_4) and a diode-connected transistor (M_5) which limits the amplifier's gain. Assuming that the output resistances of the transistors are large, the amplifier's gain is derived as

$$A=\left(g_{m,pmos}/g_{m,nmos}\right)\cdot\left(1/\alpha-1/2\right) \tag{5}$$

where $g_{m,pmos}$ and $g_{m,nmos}$ are the transconductances of the transistors, M_1(or M_2) and M_3, respectively, and α is the split factor of M_4 and M_5. As the equation (5) shows, the gain is limited and controlled by α.

Since one input of error amplifier is large swing driver output in a conventional pseudo-source amplifier, error amplifier output is limited. In the proposed architecture, however, the gate voltage of both M_1 and M_2 is retained at the value of the common-mode voltage V_C. This prevents the problem of the error amplifier output limitation. The maximum output voltage of the error amplifier ($V_{OE,max}$) is

$$V_{OE,\max}=V_C-V_{TH,M2} \tag{6}$$

where $V_{TH,M2}$ is the threshold voltage of NMOS transistor M_2. Since $V_{OE,max}$ is independent to the driver output unlike a conventional pseudo-source amplifier, the error amplifiers can provide good drive capability for the output transistor gate regardless of the driver output voltage. Additionally, the size of output transistors can be reduced as far as the desired driving current can be driven.

Generally, the distortion of output signal is decreased as the quiescent current of the output driver is increased. However, the increased current induces larger power consumption. Thus, the quiescent current should be determined to provide both sufficient linearity and low power consumption of output driver. The quiescent current of the proposed voltage-mode driver can be simply represented by the ratio between the load transistor of the error amplifier and the output transistor. Assuming that the driver output voltage is equal to the common-mode voltage V_C so that the drain currents of M_1 and M_2 are equal to $I_B/2$, the quiescent current is

$$I_q=\alpha\cdot\beta\cdot\left(I_B/2\right) \tag{7}$$

where I_B is the bias current of the amplifier and β is the ratio of M_N to M_5. From (7), the quiescent current can be reduced to any desired value by adjusting the transistor ratio of M_3, M_4, M_5 and M_N. In reality, the size of M_4 can be slightly modified from $(1-\alpha)W_n$ to account for any effect of output resistance of the transistors, and to adjust the amount of quiescent current more precisely.

The low output impedance is important in a voltage-mode driver for driving low impedance transmission lines such as UTP cables of differential 100-Ω impedance. In this case, the sum of a driver's output impedance and series termination resistance should be 50Ω — the alternative 50Ω is included in the other driver. In the proposed driver shown in Fig. 4, the output impedance is determined as

$$R_{out} = r_{o,MN} / \left(1 + g_{m,MN} r_{o,MN} A\right) \approx 1/\left(g_m A\right) \tag{8}$$

where A is the gain of error amplifier, $r_{o,MN}$ is the output resistance of M_N, and $g_{m,MN}$ is the transconductance of M_N. The PMOS output transistor M_P operates symmetrically as M_N. In case of an ideal class AB operation, the pull-up and pull-down circuits are balanced. Then, only one of the two half circuits operates and affects the overall signal swing. The output impedance of the implemented driver is designed to be about 5Ω. Therefore, the external termination resistance is determined to be 45Ω for impedance matching with UTP cables.

IV. HYBRID DRIVER

A voltage-mode driver is a good candidate for low power application. However, output swing is limited by a supply voltage and series termination resistors. When a supply voltage is V_{DD}, maximum differential output swing is V_{DD}, and maximum driving current is $V_{DD}/4Z_O$. In our design, V_{DD} is 3.3V and Z_O is 50Ω. Therefore, the maximum differential output swing is 3.3V and the driving current is 16.5mA. For an application which requires an output swing of larger than 3.3V, a voltage-mode driver cannot meet this specification under 3.3-V supply.

To overcome the limited output swing of a voltage-mode driver, a new hybrid driver is proposed as

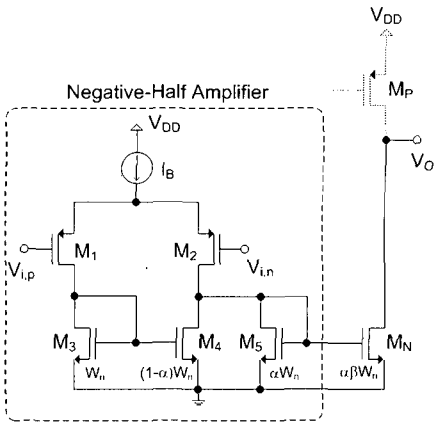

Fig. 5. Negative-half error amplifier of proposed voltage-mode driver.

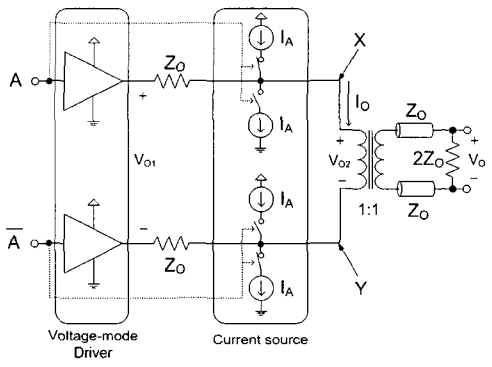

Fig. 6. Proposed hybrid driver.

shown in Fig. 6. The proposed hybrid driver includes both the voltage-mode driver and the current sources. The current sources provide supplementary current in parallel with the voltage-mode driver. This increases the driving current for larger output swing. The name "hybrid" comes from the fact that a voltage-mode driver and two current sources operate simultaneously for transmitting data. Actually, when the voltage-driver and the current sources have proper values, all signal currents can be provided from the current source while the voltage-mode driver produces only the dynamic termination voltage with no signal current. This will be explained later in detail.

The operation of the hybrid driver is as follows. When input data A is high, the voltage-mode driver output V_{O1} goes high, and the current sources are switched so that current I_A flows from node X to node Y. The amount of the required current I_A to develop output voltage of V_{O2} is

$$I_A = \frac{1}{Z_O}\left[V_{O2} - \frac{V_{O1}}{2}\right] \tag{9}$$

where V_{OI} is the voltage of the voltage-mode driver output as shown in Fig. 6.

In case of 5-V_{PP} differential output signaling over UTP cables, V_{O2} is 2.5V and Z_O is 50Ω. According to (9), I_A is decreased as V_{OI} is increased. Considering the margin of the voltage buffer output under a 3.3-V power supply, V_{OI} is set to 2.5V in the proposed design. Thus, I_A is 25mA. When V_{OI} and V_{O2} have the same value, no signal current flows across the source termination resistors unless there is reflection. Compared with a current-mode driver with an open-drain current source shown in Fig. 2(b) which requires 100mA current for 5-V_{PP} differential output swing, the total current of a hybrid driver is reduced to about a quarter of that of a current-mode driver in ideal case.

One of the design difficulties of the proposed circuit is that the two paths of signal A — one path to the voltage-mode driver and the other path to the switching current source — must undergo the same delay. Otherwise, there could be a current glitch at the output of the voltage-mode driver during timing skew. All process, voltage, and temperature variation must be considered to minimize such a glitch, which can be accomplished with extensive circuit simulation.

A voltage-mode driver described in section III can be utilized in the hybrid driver when a voltage-mode driver output swing is controlled. Because the amount of current source is smaller than that of a current-mode driver, the current sources can occupy less area than a current-mode driver. Therefore, overall area of the driver for multiple specifications can be reduced compared with a driver which includes independent drivers.

V. Experimental Results

The proposed driver was fabricated using a 0.13μm 1-poly 8-metal CMOS process with thick-oxide transistor. The microphotograph of the overall driver is shown in Fig. 7. The die area including a voltage-mode driver, current sources for a hybrid driver, and a DAC, is 0.14mm^2. The sizes of the output PMOS and NMOS transistor of a voltage-mode driver are 300μm/0.35μm and 150μm/0.35μm, respectively. The test is accomplished considering Ethernet application which needs both 2-V_{PP} and 5-V_{PP} differential output swing.

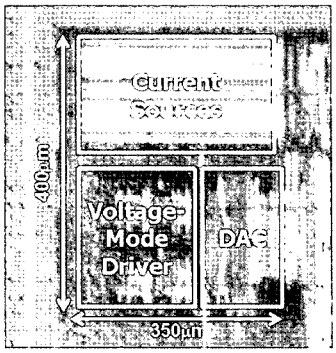

Fig. 7. Microphtograph of a proposed driver.

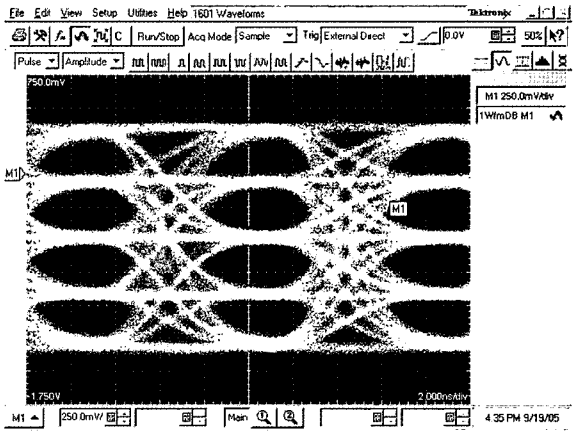

Fig. 8. Measured 5-level 1.8-VPP 125-MHz eye diagram of a voltage-mode driver over 5-m UTP cable.

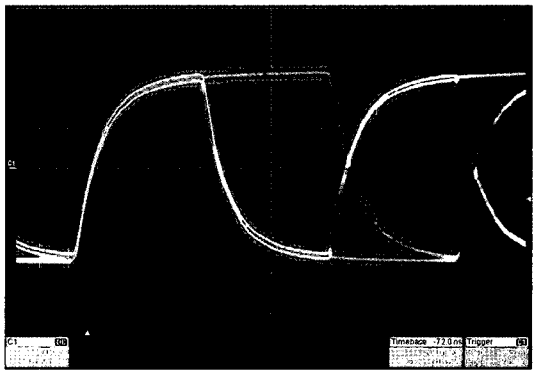

Fig. 9. Measured 4.9-VPP 20-MHz waveform of a hybrid driver over 5-m UTP cable.

Fig. 8 shows a multi-level eye diagram of a voltage-mode driver measured at the end of a 5-m UTP cable. The signal is 1.8V_{PP} at 125-MHz data rate. Fig. 9 shows a hybrid driver waveform for large swing operation. Signal frequency is 20MHz and a differential output swing is 4.9V_{PP}. No detrimental effect is found on the waveform due to possible mismatches of the two timing paths. Table 1. summarizes the performance and characteristics of the implemented driver.

Table 1. Performance Summary for Overall Driver.

Parameter	Value
Technology	0.13μm 1-poly 8-metal with thick oxide
Power Supply	3.3V
Load	100Ω (differential)
Output Swing	$1.8V_{PP}$ (voltage-mode driver) $4.9V_{PP}$ (hybrid driver)
Power Consumption	24.5mW (voltage-mode driver) 44.5mW (hybrid driver)
Overall Area	$0.14mm^2$

VI. CONCLUSIONS

An improved voltage-mode driver and a new hybrid driver have been presented. With the use of trans-impedance configuration, the common-mode range problem of error amplifiers in a voltage-mode driver is removed, thereby simplifying the design. The proposed hybrid driver which combines a voltage-mode driver and current sources, reduces power consumption and the overall area of the driver. With these drivers, a low power compact driver for multi-standard physical layer can be achieved.

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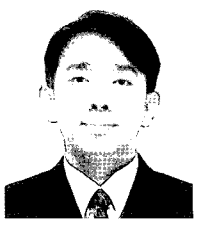

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