An InGaP/GaAs HBT Based Differential Colpitts VCO with Low Phase Noise

Bhanu Shrestha · Nam-Young Kim

Abstract

An InGaP/GaAs HBT based differential Colpitts voltage control oscillator(VCO) is presented in this paper. In the VCO core, two switching transistors are introduced to steer the core bias current to save power. An LC tank with an inductor quality factor(Q) of 11.4 is used to generate oscillation frequency. It has a superior phase noise characteristics of −130.12 dBc/Hz and −105.3 at 1 MHz and 100 kHz frequency offsets respectively from the carrier frequency(1.566 GHz) when supplied with a control voltage of 0 volt. It dissipates output power of −5.3 dBm. Two pairs of on-chip base collector (BC) diodes are used in the tank circuit to increase the VCO tuning range(168 MHz). This VCO occupies the area of 1.070×0.90 mm^2 including buffer and pads.

Key words : VCO, MMIC VCO, Differential VCO, InGaP/GaAs HBT VCO, Voltage Controlled Oscillator, Differential Colpitts VCO, Low Phase Noise VCO.

Ⅰ. Introduction

Integrated voltage control oscillator(VCO) is very important building block in all kinds of wireless communication system applications such as global positioning systems(GPS), personal communication systems(PCS), direct broadcast satellite(DBS), etc. especially such RF-VCOs are used in monolithic transmitter and receiver system. These systems demand a low phase noise. However, a low phase noise oscillator can be realized by using a dielectric stabilized oscillator, but the size will be very big. So, to make device compact, we must fabricate using modern IC technologies like InGaP/GaAs HBT, CMOS, BiCMOS, SiGe and so on.

Therefore, a new differential Colpitts VCO is designed, fabricated and characterized using InGaP/GaAs HBT technology[1]. A Colpitts voltage controlled oscillator is widely used in wireless communication systems, which utilize various technologies, due to its good cyclostationary properties(i.e. noise with periodically time-varying properties) and, also, its potentially lower phase noise characteristics. Xiaoyan Wang *et al.*[2] reported that bipolar transistors have better switching properties when implemented in the Colpitts structure. The Colpitts oscillator has fairly good frequency stability, it is easy to tune and it can be used for a wide range of frequencies in comparison with other oscillator configurations. Hajimiri and Lee[3] developed a theoretical model to describe phase noise in the oscillator. This model uses the impulse sensitivity function(ISF) to describe how a noise source affects the oscillator phase noise across an oscillation period.

Moreover, the InGaP/GaAs HBT process produces further phase noise suppression due to the use of a ledge located between the base metal and emitter to reduce intrinsic semiconductor noise. High linearity transistors, HL_F2×2×20(number of emitter fingers, width and length in micrometer respectively) and base-collector(BC) diodes, BC_35×40(width and length in micrometer respectively), provided by the Knowledge-on semiconductor company, were used in this design. This high linearity process has a cut-off frequency(f_T) of 50 GHz and a maximum oscillation frequency(f_{max}) of 80 GHz.

Section Ⅱ describes topology selection and circuit design, section Ⅲ describes measurement results and finally, conclusion will be in section Ⅳ.

Ⅱ. Topology Selection and Circuit Design

The reason of selecting differential Colpitts topology for this work is due to its superior phase noise characteristics, the possibility of a higher degree of integration and the common-mode rejection ratio(which suppresses even ordered harmonics). Furthermore, a high peak current can be delivered during a signal pulse due to its highly non-linear mode of operation, where the current in the tank circuit is delivered by a narrow pulse, there-

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by minimizing the impulse sensitivity[4]. However, a single ended Colpitts topology is not popularly used for integration due to its uncertain reliability at start up and its common-mode-rejection ratio[5]. Therefore, in this work, transistors are made cross-coupled to achieve superior phase noise and significant output power.

In this design, a differential Colpitts VCO is composed of a VCO core, asymmetric tank circuit, emitter follower buffer and a current mirror for biasing. In the VCO core of Fig. 1, the base of transistors, T3 and T1 are directly connected through resistor and in the same way, transistors T4 and T2 are also connected through resistor. These bases of T3 and T1 are connected again with collector of T4 and bases of T4 and T2 are connected with collector of T3 and made cross coupled, hence results differential configuration. All these transistors are base-biased in the base-emitter junction using optimized value of resistors in both sides. The tapping capacitors(C1 and C2) in the feedback path of T3 and T4 are optimized to obtain maximum signal amplitude and reduce the loading effect on the LC tank. So, this results the negative resistance in those transistors which initiate oscillation. The optimized values of tapping capacitors, C1 and C2 are 1.83 pF and 0.935 pF respectively.

Switching transistors, T1 and T2 are introduced which steer the bias current in the VCO core, thereby saving power. The output buffers are added on both sides of the VCO core output. T5 and T6 are emitter follower buffer circuits with input impedance and they transform 50 ohm load into larger impedance. The reason of using emitter follower is that it gives impedance transformation provided by the feedback capacitors(C1 and C2) and BC diodes(which are used as varactor). The buffers

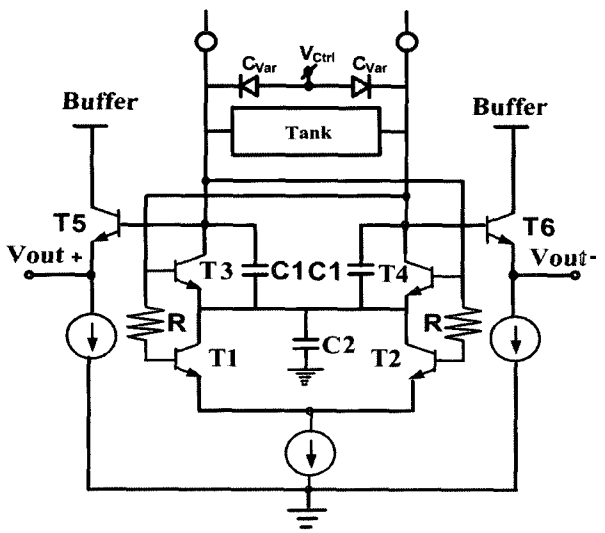

Fig. 1. The differential LC colpitts VCO.

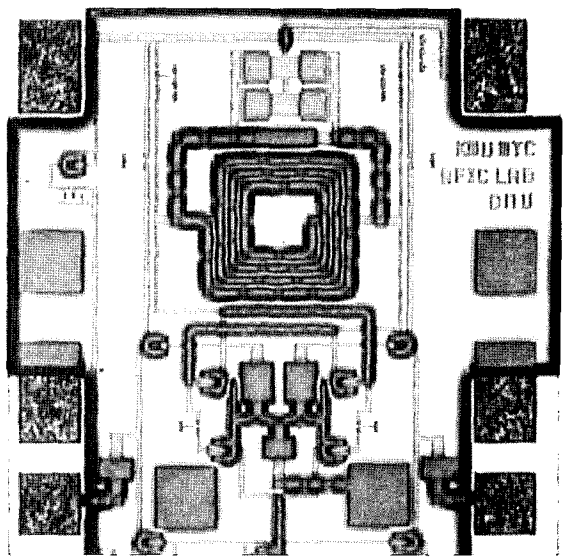

Fig. 2. A microphotograph of the fabricated VCO(size: 1.070×0.90 mm^2).

also make the circuit less sensitive to load pull when driving an active load such as the input to a mixer, and gives increased output power since it can drive 50 ohm without affecting signal amplitude in the VCO core. The bias is provided by using current mirror in the both sides of the core in order to supply continuous current. It helps to enhance the pulling figure of the VCO[6]. Two pairs of BC diodes with an asymmetric LC tank structure are used in the voltage controlled part to produce a wide tuning range since reversed bias is applied to these diodes. The quality factor(Q) determines the degree of phase noise suppression. So, an inductor (Q factor=11.4) with low series resistance is selected for this work.

The layout was generated using Cadence Virtuoso producing a chip size of 1.070×0.90 mm^2 which is shown in Fig. 2. This was performed after repeated m-line simulation using harmonic balance simulator of advanced design system(ADS) and output wave forms, output power and phase noise were also optimized during post simulation.

Ⅲ. Measurement Results

The fabricated bare chip was attached on the PCB using silver epoxy and made wire bonding in the necessary parts like in the power supply, control voltage and output signal lines. Then, the measurement was performed using spectrum analyzer(E4440A). The differential VCO(including buffer amplifier) operates with a supply voltage of 5 V and current consumption of 15 mA. Fig. 3 shows the output spectrum of the VCO. The

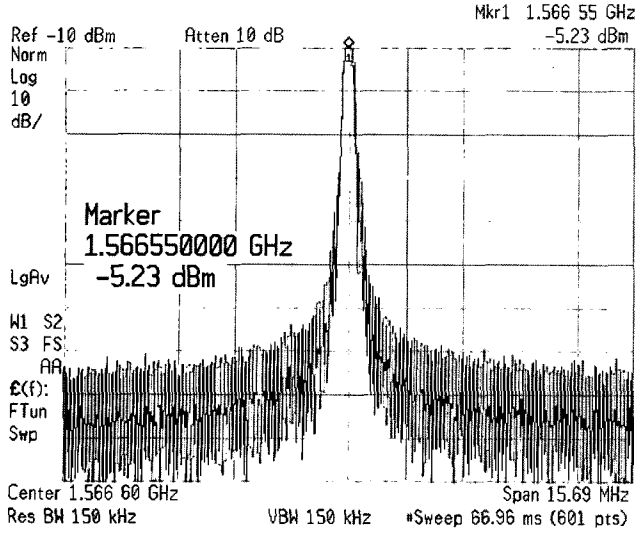

Fig. 3. Output spectrum of the VCO.

fundamental frequency was optimized at 1.566 GHz with a control voltage of 0 V. This produced an excellent output power of −5.3 dBm (including the cable loss). The second harmonics were sufficiently suppressed at −37.4 dBc, so, the spectral purity was enhanced. The designed VCO can be tuned to 168 MHz when supplying a control voltage from 0 to 3.3 V. The measured phase noise is −130.12 dBc/Hz and −105.3 dBc/Hz at 1 MHz and 100 kHz offset frequencies, respectively from the carrier frequency of 1.566 GHz. Fig. 4 depicts a superior phase noise characteristics of designed VCO. The oscillation frequency and output power as a function of control voltage is shown in Fig. 5. This shows that the oscillation frequency decreases with control voltage and output power. Table 1 shows a comparison of phase noise characteristics with other differential Colpitts VCOs with the same and different technologies at 1 MHz offsets. It shows a better phase noise characteristics among those recently published papers. Table 2 shows a summary of designed VCO performances.

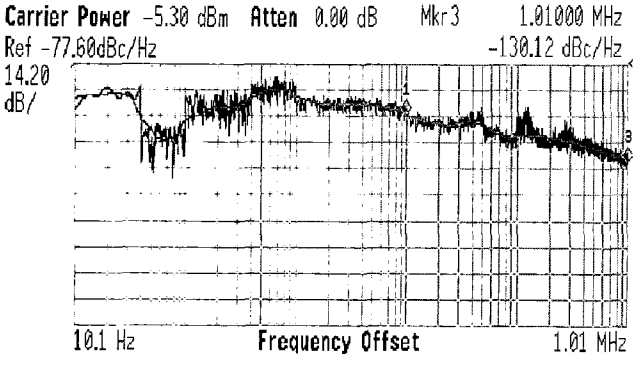

Fig. 4. Phase noise characteristics.

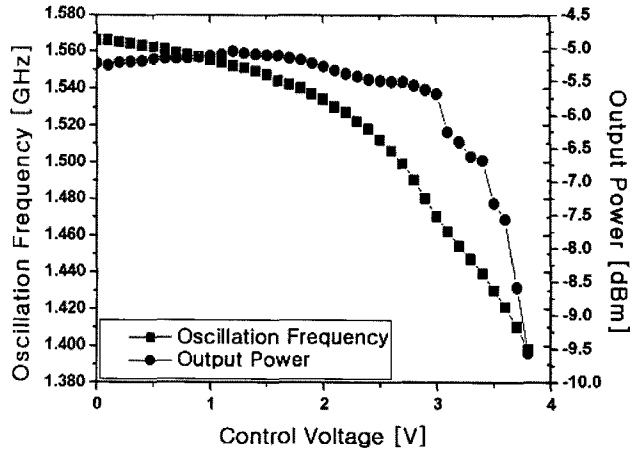

Fig. 5. Oscillation frequency and output power as a function of control voltage.

Table 1. Comparison of phase noise characteristics with recently published papers on Colpitts VCOs.

References	Oscillation Frequency [GHz]	Phase Noise @ 1 MHz [dBc/Hz]
[7] SiGe Biopolar	2.4	−104
[8] CMOS	6.4	−120
[9] CMOS	1.79	−128
[10] InGaP/GaAs HBT	1.664	−122
[10] InGaP/GaAs HBT	1.715	−129.9
[11] CMOS	1.8	−124.3
This Work	1.566	−130.12

Table 2. Summary of VCO performance.

Parameters	Unit	Measurement Results
GHz	GHz	1.566
Supply Voltage	V	5
Tuning Range	MHz	168
Output Power	dBm	−5.3
Phase Noise @ 1 MHz	dBc/Hz	−130.12
Figure of Merits	dBc/Hz	−182
Chip Size	mm^2	1.07×0.9

The figure of merit(FoM) is also another important parameter used in evaluating the phase noise performance of the VCO. It is useful in comparing the performance of oscillators with different parameter values. The widely used Leeson formula can be used for cal-

culating the FoM:

$$FOM = L(\Delta f_m) - 20\log\left(\frac{f_0}{f_m}\right) + 10\log\left(\frac{P_{dc}}{1mW}\right) \quad (1)$$

where $L(\Delta f_m)$ is the phase noise spectral density, *Pdc*, is the DC power dissipation of the VCO core(16.65 mW), f_o, is the oscillation frequency and f_m is offset frequency. This equation describes the maximum suppression of phase noise in the VCO. The calculated FoM for this VCO is around −182 dBc/Hz.

Ⅳ. Conclusion

A fully integrated InGaP/GaAs HBT based differential Colpitts VCO with low phase noise was designed, fabricated and characterized. The VCO was optimized for low phase noise considering tank design and oscillator amplitude. The advantages of this design are reduction of components, integration of BC diodes as varactors for enhancing tuning range and low phase noise characteristics. It achieved a low phase noise of −130.12 dBc/Hz at 1 MHz offset from the carrier frequency of 1.566 GHz with a control voltage of 0 V. However, it has not produced quite stable oscillation frequency. So, it needs to make locking the VCO at the frequency of interest using phase locked loop(PLL), because each element of PLL systems has an overall effect on VCO stability.

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