Copper Phthalocyanine Field-effect Transistor Analysis using an Maxwell-wagner Model

Ho-Shik Lee[a], Seung-Ho Yang, and Yong-Pil Park
Department of Hospital Biomedical Engineering, Dongshin University,
252 Daeho-dong, Naju, Jeonnam 520-714, Korea

Eun-Ju Lim and Mitsumasa Iwamoto
Department of Physical Electronics, Tokyo Institute of Technology,
Tokyo 152-8552, Japan

[a]E-mail : hslee@dsu.ac.kr

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Organic field-effect transistor (FET) based on a copper Phthalocyanine (CuPc) material as an active layer and a SiO_2 as a gate insulator were fabricated and analyzed. We measured the typical FET characteristics of CuPc in air. The electrical characteristics of the CuPc FET device were analyzed by a Maxwell-Wagner model. The Maxwell-Wagner model employed in analyzing double-layer dielectric system was helpful to explain the C-V and I-V characteristics of the FET device. In order to further clarity the channel formation of the CuPc FET, optical second harmonic generation (SHG) measurement was also employed. Interestingly, SHG modulation was not observed for the CuPc FET. This result indicates that the accumulation of charge from bulk CuPc makes a significant contribution.

Keywords : Organic FET, Copper phthalocyanine (CuPc), Maxwell wagner model,
Second harmonic generation (SHG)

1. INTRODUCTION

Organic semiconductors have recently been used as active layers in electronic devices such as field-effect transistors (FETs). The mechanism of carrier transport in organic semiconductors is one of the most important research subjects to be elucidated for improving of device performance[1,2]. CuPc materials are well known to show excellent semiconductor performance and have been studied for the use as organic field-effect transistors (OFETs). Until now much experimental efforts, such as modification of the film quality, has been devoted to improve the device performance. In the present paper, we show the I-V and C-V characteristics to clarify the carrier transport in CuPc FET using a Maxwell-Wagner (MW) model[3,4]. It is noteworthy that the MW model describes of the FET characteristics in which carriers injected from Source and Drain electrode make main contribution, but the resulting FET characteristics are very similar to the FET characteristics derived based on a gradual channel model used in semiconductor device physics[5-7]. Main difference is in that the MW model can explain the Organic FET performance that requests high biasing voltage for the drive. In the present paper, to further discuss the origin of charge carriers, we also examined the enhancement of optical second harmonic generation (SHG) from the FET channel.

2. EXPERIMENTALS

Figure 1 shows a device configuration of the CuPc FET and equivalent circuit for the double layer capacitance. The FET has a bottom-contact structure with the CuPc materials deposited onto an inter-digit Au electrode. The channel length (*L*) and width (*W*) are 50 μm and 11 *cm*, respectively.

We were the UV/ozone treatment on the SiO_2 layer with the Au source and drain electrodes for the duration of 30 minute before deposited the CuPc material. The UV/ozone-treatment was done in an UV/ozone-treatment chamber (NL-UV 253S: Nippon Laser & Electronics Lab.) filled with oxygen gas. During the UV/ozone-treatment, UV light from a low-pressure mercury lamp was irradiated onto the surface of the SiO_2 layer with the Au source and the drain electrodes. The CuPc material

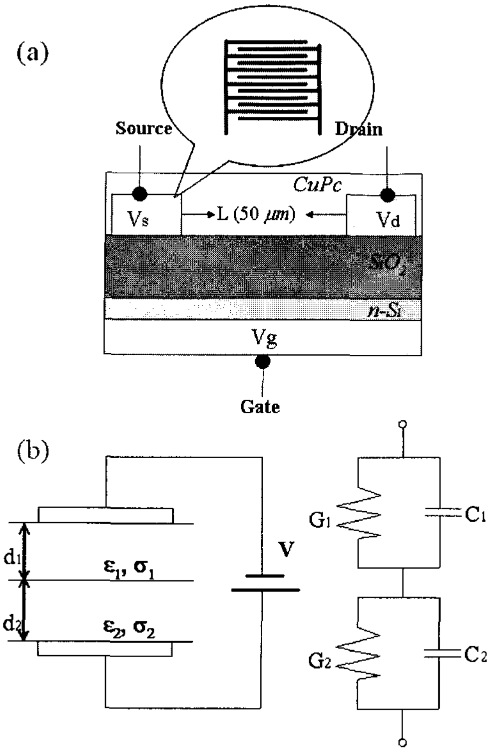


Fig. 1. (a) Schematic diagram of the bottom-contact CuPc FET and (b) equivalent circuit for the double layer capacitance.

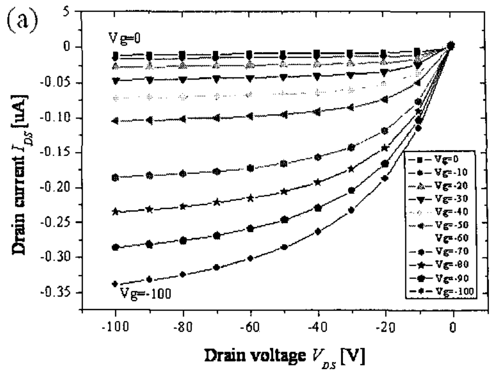
was purchased from Tokyo Kasei Kogyo Co. Ltd. and was used without purification. The CuPc was deposited by thermal evaporation method. During the deposition, the rate was about 0.5 Å/s and the vacuum level less was kept at than the 10^{-7} torr, and the substrate was kept at a room temperature.

To understand the increase of the capacitance and the formation of channel due to bias voltage, Maxwell-Wagner model was introduced to the CuPc FET. Therefore, Fig. 1(b) shows the equivalent circuit for the actual system in our CuPc FET. Then, the capacitance can be approximately express as,

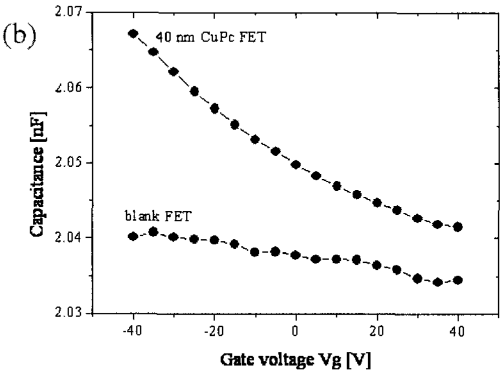
$$G_1 = \sigma_1 \frac{S}{d_1}, C_1 = \varepsilon_1 \frac{S}{d_1} \tag{1}$$

$$G_2 = \sigma_2 \frac{S}{d_2}, C_2 = \varepsilon_2 \frac{S}{d_2} \tag{2}$$

In this model, if the channel conductance changes due to the gate bias, the change of capacitance is expected. To fit the experimental results, we assume the channel conductance is very small at a voltage region less than the threshold at gate voltage is 0 V. So the between applied gate bias and channel conductance is unknown at this stage, it is assumed the channel conductance linearly increases with the applied gate bias[3,4].



(a) I-V characteristics



(b) C-V characteristics

Fig. 2. (a) I-V characteristics and (b) C-V characteristics of bottom-contact 40 nm CuPc FET.

The I-V and C-V characteristics measurements were carried out in an evaporation chamber without breaking of vacuum by using a source-meter (Keithley type-2400) and LCR meter (Hioki type-3522-50).

3. RESULTS AND DISCUSSION

Figure 2(a) shows the current-voltage (I_{ds}-V_{ds}) and the capacitance-voltage (C-V) characteristics of the 40 nm CuPc bottom-contact FET. The applied gate voltage was from 0 to -100 V and also scanning rate to take the I_{ds}–V_{ds} was from 0 to -100 V. From the Fig. 2(a), we observed the typical the FET behavior, though the biasing voltage was very high, e.g., -100 V.

Employing the MW model the FET characteristics were analyzed, and the field-effect mobility was calculated as $\mu = 1.9 \times 10^{-4}$ cm^2/Vs. The mobility of the CuPc FET was not so high in comparison with mobility of pentacene, oligothiophene and fullerene etc[5].

Figure 2(b) shows the C-V characteristics of the CuPc FET with the bias voltage with region is from -40 V to 40 V with 43 Hz. As shown in Fig 2(b), the full circles indicate the capacitance of the sample with CuPc layer, whereas the open circles indicate the capacitance of the sample without CuPc layer (blank FET). From the Fig.

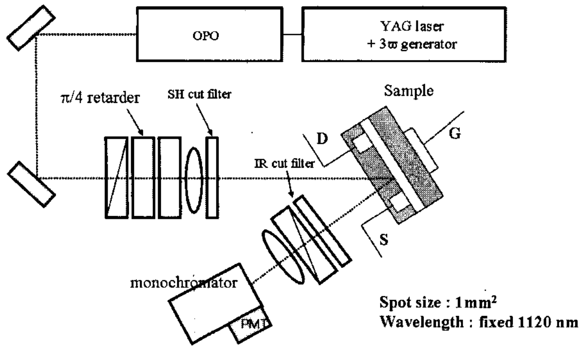


Fig. 3. Setup for the SHG measurement.

2(b), the capacitance of the sample with CuPc layer increases with increase of negative bias voltage and approaches about 256 nF, but not saturate. On the other hand, the capacitance change for the blank FET was very small, about 62 nF. The difference of the capacitance of the samples with CuPc from that without CuPc FET was about 264 nF, corresponding to the amount of accumulated carriers at the interface between CuPc and SiO_2 layer.

To understand the formation of channel at the interface between CuPc and SiO_2, the Maxwell-Wagner capacitor model was employed because we applied a quite large voltage to the FET, e.g., -100 V. This means, we tentatively assumed that carries contributing the channel formation are supplied from Source electrode.

In order to further clarify the origin of charge carriers, the SHG experiment was employed. Figure 3 shows the setup for the SHG measurement. The spot size is a 1 mm^2 and the wave length is a fixed with 1120 nm.

Figure 4 shows the response of the SHG and drain current (I_{ds}) with applying bias voltages as follows: Region Zero (V_{ds} = 0 V, V_g = 0 V), Region Off (V_{ds} = -100 V, V_g = 0 V), and Region On (V_{ds} = -100 V, V_g = -100 V), where V_d and V_g represented applied voltage between drain and source electrodes and gate and source electrodes, respectively. As shown in the Fig. 4(a), the SHG signal was not observed in region zero, off and on state, but from the Fig. 4(b), the drain current was observed at on state. This result indicates that and the injection of carrier from the electrode into bulk CuPc was very fast, and very smoothly spread to form the channel. However, the possibility of charge carrier accumulation from the bulk CuPc also remains.

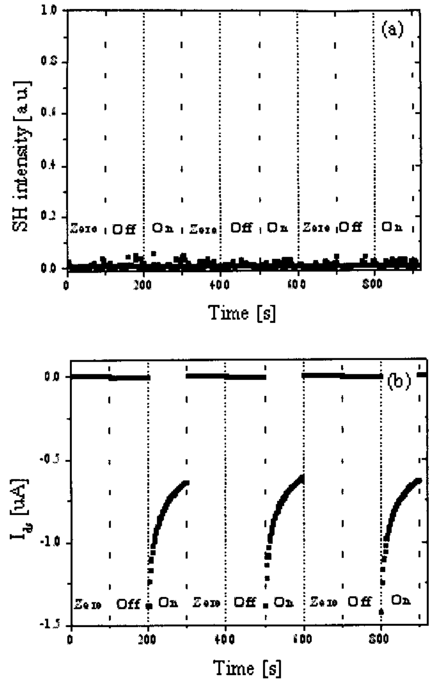


Fig. 4. Response of (a) SHG with applied bias and (b) drain current for CuPc FET.

4. CONCLUSION

Bottom-contact CuPc FETs were fabricated on inter-digit formed substrate with UV/ozone-treatment before the deposition of the CuPc layer. The Maxwell-Wagner model could be employed to analyze the I-V and C-V characteristics of the CuPc FETs. Using the SHG, we investigated the channel region of the CuPc FET, but we did not observed the SHG signal. This result indicates that the accumulation of charge from bulk CuPc makes a significant contribution.

ACKNOWLEDGMENTS

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