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A 8-bit Variable Gain Single-slope ADC for CMOS Image Sensor

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Summary

A new 8-bit single-slope ADC using analog RAMP generator with digitally controllable dynamic range has been proposed and simulated for column level or per-pixel CMOS image sensor application. The conversion gain of ADC can be controlled easily by using frequency divider with digitally controllable divider ratio, coarse/fine RAMP with class-AB op-amp, resistor strings, decoder, comparator, and etc. The chip area and power consumption can be decreased by simplified analog circuits and passive components. Proposed frequency divider has been implemented and verified with 0.65um, 2-poly, 2-metal standard CMOS process. And the functional verification has been simulated and accomplished in a 0.35μm standard CMOS process.

Key words: Single-slope ADC, Pixel level ADC, CMOS Image Sensor, Ramp generator, Class-AB op-amp

1. Introduction

The advantage of CMOS image sensors is the ability to integrate sensing and processing on the same chip. This advantage is especially important for implementing imaging systems requiring significant signal processing such as digital cameras and computational sensors. Most of the reported work on single chip CMOS image sensor IC involve one of the ADC type with chip, column or pixel level signal processing[1,2].

Pixel level signal processing promises very significant advantages. Several authors[3,4] shows that pixel level A/D conversion approaches achieve higher SNR and low power consumption than chip or column level A/D conversion. Because it is performed parallel, close to where the signals are generated, and operated at very low speed. In addition, the most important advantage of pixel level processing is that signals can be processed during integration time and also well suited for standard digital CMOS process implementation.

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However, there are some disadvantages and difficulties in implementing high performance analog signal processing circuits for column level or per-pixel signal processing in one-chip CMOS image sensor system. For example, as increasing resolution and conversion gain of ADC, the unit step voltage of analog RAMP becomes significantly small to process, and then the possibility of happening error goes to increase. As a result, in practical application, not theoretically, the RAMP signal generation circuit implementation becomes too difficult.

So, in this paper, to overcome previously mentioned problems, we introduce a single-slope Nyquist-rate ADC for pixel level signal processing with newly observed analog RAMP generator. It uses frequency divider and reduced number of resistor string, just requiring 32 resistors for 8-bit resolution, to generate RAMP signal reference generation. It is suited for meeting the stringent area and power requirement for a pixel level implementation.

The rest of this paper is made up as follows. In section 2, we describe the operation of simple class-AB op-amp, programmable frequency divider and programmable single-slope ADC. In section 3,

we summarize the results of SPICE simulation for proposed single-slope ADC and shows the measured results of frequency divider. Section 4 gives the conclusion.

2. Circuits Implementation

In this section we give a brief introduction about proposed class-AB op-amp, programmable frequency divider, architecture and operation of single-slope ADC.

2.1 Class-AB Operational Amplifier

Low-voltage, high speed rail-to-rail op-amp are designed and simulated to use with reference voltage driver by using the modified fully differential block and class-AB output stage as shown in Fig.1. In the first stage of op-amp, to implement rail-to-rail input dynamic range , PMOS and NMOS differential input pairs(MPINP - MPINN, MNINP - MNINN)are used to converting differential input voltage to single-ended output current, which is buffered with class-AB biased output stage(MPdri - MNdri). The class-AB biasing for low-quiescent current is composed with two sets of floating current sources (MP4 - MP5 , MN4 - MN5).

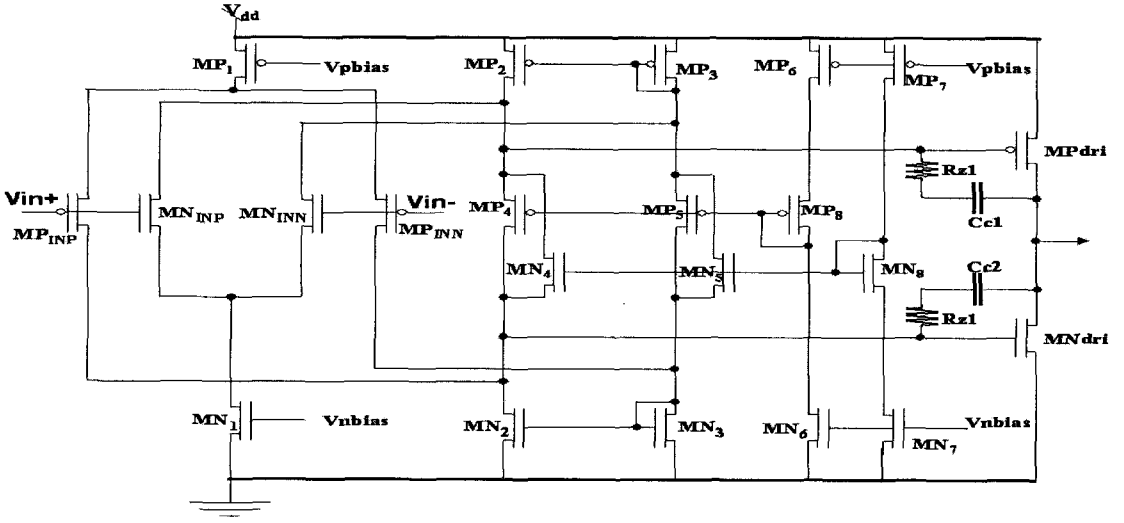


Fig. 1. Circuit of the adopted op-amp with class-AB output

$$C_c = \frac{C_L}{g_{mdri} R_z - 1} \quad (1)$$

where, $g_{mdri} = \sqrt{\mu_{dri} C_{ox} W_{dri} / L_{dri} I_{dri}}$.

The design procedure was very close to the approach proposed in [5].Minimum length transistors are chosen through the design to minimize the stray capacitors as much as possible knowing that this may cause problems due to the channel length modulation effect and process variations. To simplify the design it is assumed to have two dominant poles which are split apart by the compensation capacitor. The CC and Rz values are chosen 1.8pF and 2kΩ according to (1) to give 80° of phase margin at 10pF output load.

2.2 Programmable Frequency Divider

Existing frequency divider are generally applied to implement frequency synthesizer[6,7,8,9]. Its architecture is complicate, but the range of dividing is significantly limited. For example, to implement divide by 32 and divide by 33 functions, it is impossible to divide with typical pre-scaler under 1024 programmable value.

But the frequency divider which is proposed and designed in this study can divide any number of odd or even in the programmed dividing range and

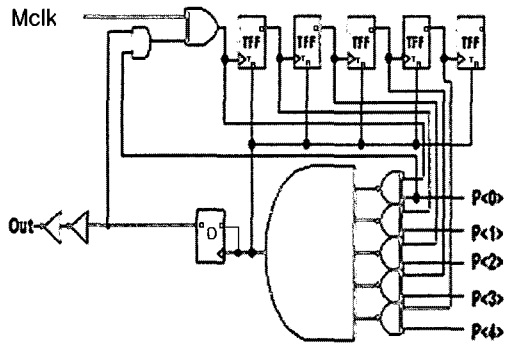


Fig. 2. The architecture of programmable frequency divider

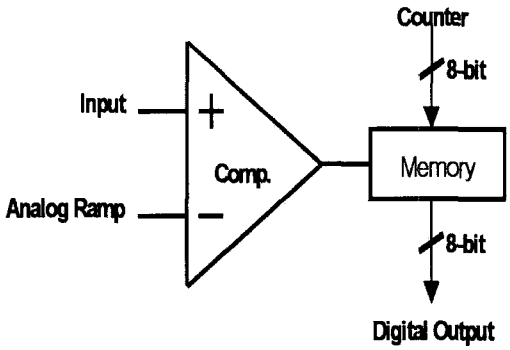
the dividing range is decided by the number of used flip-flops. Fig. 2 shows the conceptual architecture of proposed programmable frequency divider and it's operation is as follows. Divider ratio will be established by programmable input signal P<4:0>. The programmed value is equal to binary value of P<4:0>. For example, if P<4:0> value is divider ratio is divide-by-3. The output that is established by P<4:0> and Mclk signal simultaneously applied to the input of exclusive-OR gate. The output of exclusive-OR gate is counted by negative edge-triggered TSPC-TFF[10]. Its status are reset when the outputs of TSPC-TFF are equal with P<4:0> values.

By this method, even and odd divider ratio will be implemented and easily programmed by setting P<4:0>values. This frequency divider can get divider ratio from 1 to 32 and its divider ratio can be increased simply by adding flip-flop and can be expressed in 2N (N is the number of flip-flop).

2.3 Proposed 8-bit Single-slope ADC

In Fig. 3, a general single-slope ADC architecture for CMOS image sensor is portrayed and its operation is as follows. At the start of conversion, the RAMP voltage goes up to just above the highest expected photo-diode output voltage(input at Fig. 3). This causes the comparator to switch its output to low, which enables the per-pixel memory to begin loading the output of counter values. Then, the RAMP is swept down linearly it exceeds the reset(input) voltage level.

At the same time, the output value of counter sweeps across an equivalent set of values; 256 of them for 8-bit.



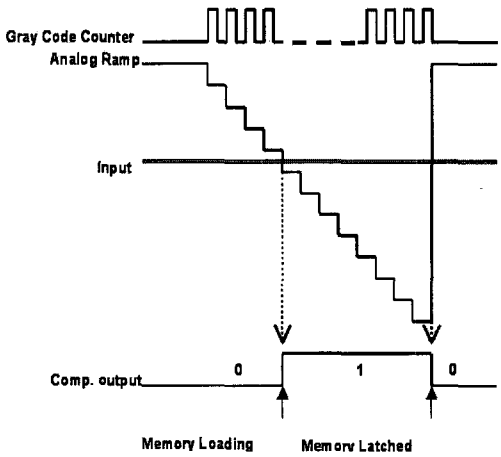
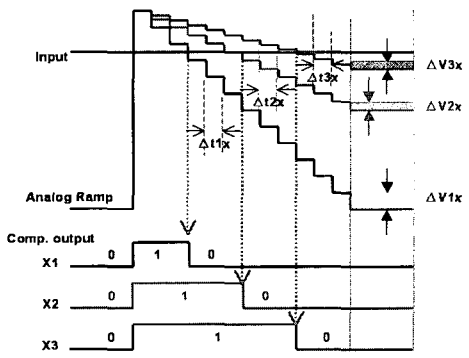
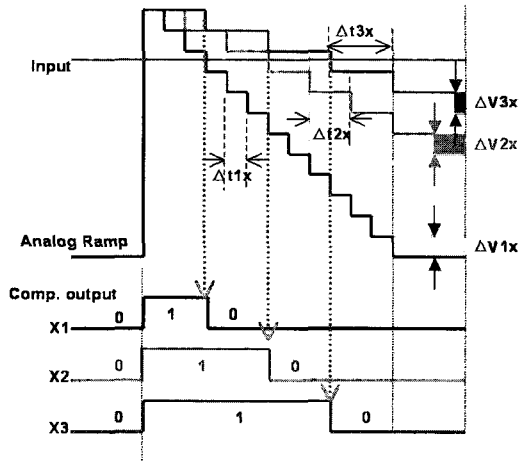


Fig. 3. Typical single-slope ADC operation



(a) Conventional method



(b) Proposed method

Fig. 4 The comparison of gain control method

As the RAMP crosses each photodiode's output voltage level, each per-pixel comparator output switches high, and that the counter's values are latched to pixel's memory at that moment. In the case of conversion gain control methods, conventional method is shown in Fig.4-(a) and proposed gain control method is shown in Fig.4-(b). There is great difference between them which is the factor of conversion gain control. In conventional method, unit step voltage of RAMP(expressed as $\Delta V1x, \Delta V2x, \Delta V3x$) is divided by magnification, and has relationships as (2).

$$\Delta V2x=\Delta V1x/2$$
$$\Delta V3x=\Delta V1x/3 \quad (2)$$
$$\Delta t1x=\Delta t2x=\Delta t3x$$

From (2), we can expect that conversion gain increase higher, unit step voltage of RAMP(ΔV) goes too small. On the other side, Δt is maintained uniformly. So, very precise and matched analog component(capacitor or resistor) of integrator are needed to implement required conversion gain.

$$\Delta t2x=\Delta t1x/2$$
$$\Delta t3x=\Delta t1x/3 \quad (3)$$
$$\Delta V1x=\Delta V2x=\Delta V3x$$

However, as shown in Fig.4-(b), in proposed method, instead of ΔV control , a step up/down time(Δt) is increased or decreased in accordance with conversion gain. Their relationships are expressed in (3). So the burden of analog circuit for precise RAMP signal generation can be significantly reduced. This is the most important advantage of proposed RAMP generation is its very simple and robust conversion gain control method. A block diagram of proposed ADC is shown in Fig.5. It comprises op-amps, counters, decoders, frequency dividers, coarse/fine resistor strings, memories, comparator and etc.

At the start of conversion in Fig.5, the globally distributed clock(Mclk) are applied to programmable N frequency divider and 8-bit counter. If conversion gain is 1, P<4:0> of frequency divider is programmed to 00001. The reference voltage is generated by two set of R-string. The voltage of top and bottom is biased and maintained by designed class-AB op-amps. The RAMP voltage is initially stepped up to highest level just above the expected photodiode reset level and stepped down to the bottom level of reference voltage level by decoders. This RAMP signal is compared with analog input and makes the comparator to switch its output low, which enables the per-pixel memory to begin loading the counter's values. As shown in Fig. 6, it is generated by coarse/fine R-string block.

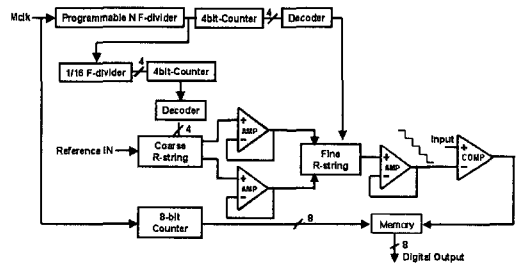


Fig. 5. Proposed 8-bit single-slope ADC architecture

The coarse RAMP sweeps down at every 16 clock of the programmable F-divider output and the fine RAMP sweeps down at every clock of the programmable F-divider output. Simultaneously, the counter sweeps across an equivalent set of values; 256 of them for 8-bit resolution. As the RAMP crosses reset input voltage, the comparator output

switches high, and the counter's value is latched to the memory, retaining the counter value present at that moment. As a result of the conversion process, the memory contains 8-bit counted value which represents digital value of its analog reset input voltage.

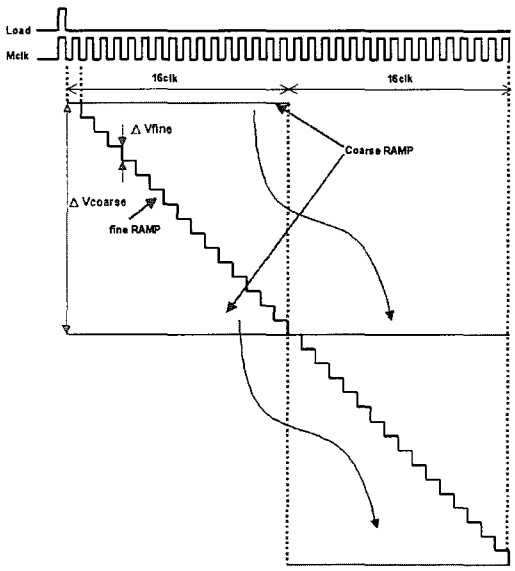


Fig. 6. The Coarse and fine RAMP of proposed ADC

$$\Delta Vfine = \frac{InputDynamicRange}{2^N \cdot m} \quad (4)$$

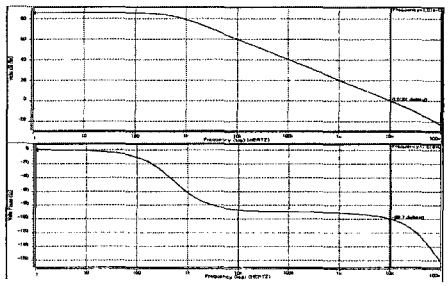
$$\Delta Vfine = \frac{InputDynamicRange}{2^N} \quad (5)$$

where ΔVfine is unit RAMP step voltage, N is the resolution, and m is conversion gain. Because Δ Vfine in (4) goes too small compare to the resolution, conventional method using switched capacitor integrator for the RAMP generation requires very precise amplifier and good capacitor/resistor matching. However, as shown in equation (5), Fig.4-(b) and Fig.6, the proposed conversion gain control method is independent conversion gain m, it is only depend on the resolution N of data converter as shown in equation (4).

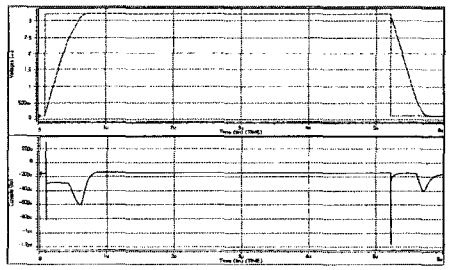
3. Simulation and Measurement Results

3.1 Class-AB Amplifier

As summarized in Table 1, the simulated slew rate is 6V/usec, and the measured quiescent current is 150uA. The open loop gain is 85dB and phase margin is 80dB at 10pF output load as shown in. Fig. 7(a) Fig. 7(b) is step response of designed op-amp at VCC=3.3V, Vin=0.1V~3.2V.



(a) open-loop gain and phase margin



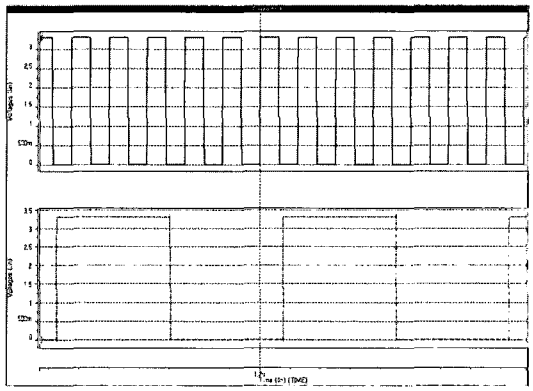
(b) Step response and supply current dissipation

Fig. 7. The simulation results of Class-AB op-amp in Fig.1

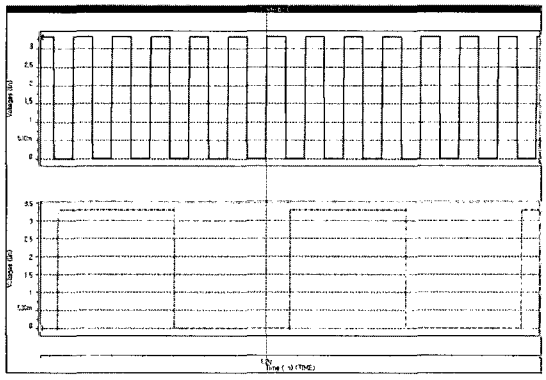
	Design specifications	Simulation
Unit gain frequency	10㎒	10㎒
Current consumption	200uA	150uA
Open loop gain	>	85dB
Phase Margin	>°	80°
Slew Rate	6V/usec	6V/usec
I/O Dynamic Range	0.2V~ VCC-0.2V	0.1V~ VCC-0.1V
Output load	10pF	10pF
Supply Voltage	2.5V~3.5V	2.3V~3.7V

Table 1. Operational amplifier design specifications and simulation results

3.2 Programmable Frequency Divider



(a) The output of divide by 6



(b)The output of divide by 7

Fig. 8. The results of simulated divide by 6 and 7 at Mclk=10MHz

In this section, a novel architecture of programmable divider has been designed, fabricated and verified with using 0.65㎛ 2-poly, 3-metal standard CMOS process. Figure 8 (a), (b) is the simulated output waveform of divide by 6 and 7 in 10㎒ input frequency.

As summarized in Table 2, the simulated operation frequency is 100㎒, and the measured operation frequency is 10㎒. The simulated power consumption is 15㎽ and the measured power consumption is 1.3㎽. The simulated and the measured Duty ratio is 50%. Supply voltage is 3.3V.

Design specifications	Simulation	Measurement
Frequency	100㎒	10㎒
Power consumption	15㎽	1.3㎽
Duty ratio	50%	50%
Supply Voltage	3.3V	3.3V

Table 2. Frequency divider design specifications and simulation results

3.3 Proposed 8-bit Single-slope ADC

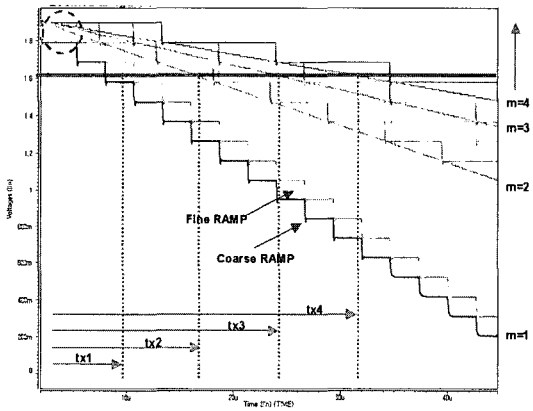


Fig. 9. Simulation results of conversion gain m=1,2,3,4

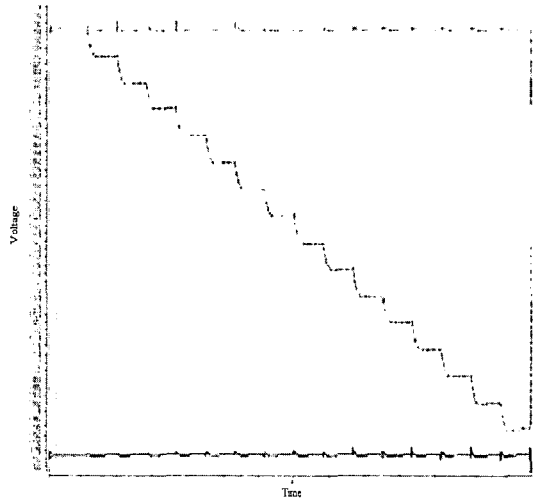


Fig 10. A zoomed waveform view of dotted circle(m=1) in Fig. 9

The proposed 8-bit single-slope ADC has been simulated using Hynix 0.35um CMOS process, and simulation has been performed with HSPICE. It has static current consumption of 260uA at 3.3V supply voltage. Current consumption summary is shown in Table 3. Figure 9 shows coarse/fine RAMP waveform. Coarse RAMP sweeps 16-step and fine RAMP sweeps 16-step at every step of coarse RAMP as shown in figure 9 and 10. Memory loading time for each conversion gain(m=1,2,3,4) are in accord with previously discussed at section II.

Design Blocks	Design specifications	Simulation results
Frequency Divider(2ea)	max. 1mA @ 40MHz	0.5mA @ 40MHz
Operational amplifier(3ea)	max. 0.5mA	0.45mA
Comparator	max. 5uA	4uA
R-string	max. 0.2mA	0.1mA
Bias networks	max. 0.2mA	0.1mA
Total current consumptions	max. 2mA	1.5mA

Table 3. Current consumption summary

4. Conclusions

We have introduced a newly proposed single-slope ADC. By minimizing the usage of analog components (op-amp, resisters etc.), it can be used very simple and robust circuits for CMOS image sensor pixel level signal processing. The simulation results show that the ADC can achieve good performance.

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