Digital Sequence CPLD Technology Mapping Algorithm

Choong-Mo Youn

Abstract—In this paper, The proposed algorithm consists of three steps. In the first step, TD(Transition Density) calculation has to be performed. a CLB-based CPLD low-power technology mapping algorithm considered a Trade-off is proposed. To perform low-power technology mapping for CPLDs, a given Boolean network has to be represented in a DAG. Total power consumption is obtained by calculating the switching activity of each node in a DAG. In the second step, the feasible clusters are generated by considering the following conditions: the number of inputs and outputs, the number of OR terms for CLB within a CPLD. The common node cluster merging method, the node separation method, and the node duplication method are used to produce the feasible clusters. In the final step, low-power technology mapping based on the CLBs packs the feasible clusters. The proposed algorithm is examined using SIS benchmarks. When the number of OR terms is five, the experiment results show that power consumption is reduced by 30.73% compared with TEMPLA, and by 17.11% compared with PLA mapping.

Index Terms—CPLD, Low-power technology mapping, Trade-off

I. INTRODUCTION

Low-power circuits are increasingly being designed to improve the power consumption of circuits vis-a-vis the growing demand for state-of-the-art portable electronic goods with the development of VLSI manufacturing, for which the design technology is appearing on important specifications.

The reason to consume the electricity in the circuit is various. A dynamic power to occupy most many importance in a digital system. A dynamic power generated capacitance and charging, discharging process[1].

Especially in the case of low-power circuit designs, the dynamic power of a circuit decreases, thereby reducing the switch capacitance of the applied node emphasis [2].

Decreased physical capacity of each node and switching activity for reduce number of switch capacity in circuit.

It is known that a more efficient method decreases switching activity compared to a method that reduces physical capacitance. Various methods to reduce power consumption have been suggested [3].

DDMAP and TEMPLA, TMCPLD, and PLA mapping, etc., are proposed in the published CPLD technology mapping algorithm, which does not consider, however, their low power and other shortcomings and does not take into account the trade-off between time and area [4-8].

This paper shows that a circuit can be made low-power when the CPLD's power consumption is considered. Such power consumption has a CLB base supplementation shortcoming, however, as it does not consider the interrelationship between the area and the delay time, the same shortcoming of the existing CPLD technology mapping algorithms. This paper suggests a new CPLD technology mapping algorithm that considers a trade-off between power consumption, area, and delay time.

II. CLB-BASED CPLD LOW-POWER TECHNOLOGY MAPPING ALGORITHM CONSIDERED A TRADE-OFF

A combination circuit is reconstructed in a DAG. To calculate the power consumption of each node's EP(equilibrium probability) for the component gate, the TD must be calculated. The node component gate is the INVERTER and the AND, OR gates EP and TD for each gate should be as follows. For the signal x EP p(x), TD is represented as d(x). Also, the output number of a gate is represented as out(x). For the output signal y, the following equations apply.

INVERTER

$$p(y) = \frac{1 - p(x_1)}{out(x)} \tag{1}$$

$$d(y) = d(x_1) \bullet out(x) \tag{2}$$

AND gate

$$p(y) = \frac{\prod_{i=1}^{m} p(x_i)}{out(x)} \tag{3}$$

$$d(y) = \sum_{i=1}^{m} [\prod_{j=1, j\neq 1}^{m} (p(x_j)) d(x_i)] \bullet out(x) \tag{4}$$

OR gate

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$$p(y)=\frac{1-\prod_{i=1}^{m}(1-p(x_i))}{out(x)} \quad (5)$$

$$d(y)=\sum_{i=1}^{m}[\prod_{j=1,j\neq 1}^{m}(1-p(x_j)))d(x_i)]\bullet out(x) \quad (6)$$

The CPLD must embody low power by calculating the power consumption of the whole circuit and of the component CLB.

The CPLD's power consumption Eq. (7) consists of a CLB.

$$P_{avg}(N)=\sum_{PI_{pi}}(\frac{1}{2}C_{in}V_{dd}^2d(P_i)) + \sum_{CLB\,C_i}\{\frac{1}{2}N_{OR}[C_{out}+fanout(C_i)C_{in}]V_{dd}^2d(C_i)\} \quad (7)$$

in which $d(p_i)$ is the TD of the primary input, $fanout(C_i)$ is the output number of the CLB, $d(C_i)$ is the TD of the CLB, and N_{OR} is the TD of the used OR gate in the CLB, where:

$$used\ OR\ gate=\frac{mapped\ OR\ term}{s\tan dard\ OR\ term\ of\ CLB}\le\frac{\max imun\ OR\ term\ of\ CLB}{s\tan dard\ OR\ term\ of\ CLB}.$$

An early input in accomplishing the proposed algorithm is the Boolean network.

When the Boolean network is converted to DAG and the algorithm is applied to change the DAG, the technology mapping sequence of low power is derived.

To perform technology mapping of low power, must be selected beforehand to embody the given circuit.

To perform minimum-level technology mapping of low power, the element selected must satisfy the condition (k, m, p) using the component CLB's information and the circuit's power consumption, which creates feasible clusters when the power consumption is minimum.

The proposed low-power CPLD technology mapping algorithm is divided into three steps to extract the technology mapping results so that the lowest level of power consumption of a given circuit may be achieved.

A. TD Calculation

Technology mapping must be performed to minimize the circuit's full power consumption and switching action, and to get the technology mapping sequence of low power.

Therefore, to calculate power consumption given the Boolean network, the EP (equilibrium probability) for the gate of each component node and the TD must be calculated.

The component gate calculates the node because the EP and the TD.

B. Feasible Cluster Generation

The TD for each component node given the Boolean network using the calculated sequence must create a feasible cluster. The feasible cluster target element embodies the circuit for all clusters that can do mapping to the component CLB.

The number of OR terms of the CLB is represented as CLB_OR. The created feasible cluster is represented as CLB_OR. The feasible cluster that calculates the expense of a node should be created. Each node expense defines the number of OR terms that a node has. The whole expense of a cluster is represented as CST_C, and the overhead expenses of a cluster refers to the number of OR terms when the cluster is created. Eq. (8) shows the method of calculating the expense of CST_C.

$$CST_C(n)=\begin{cases}\prod_{p=1}^{n}[Child\_Node(p)] & Pre\_Node(k)=1\\ \sum_{p=1}^{n}[Child\_Node(p)] & Pre\_Node(k)>1\end{cases} \quad (8)$$

in which $Child\_Node(p)$ refers to the number of OR terms with input nodes of the target node.

The above equation creates a feasible cluster that considers the CST_C using common node cluster merging, node separation, and node duplication.

1) Common Node Cluster Merging

The number of output edges detects the greatest number of nodes among the DAG nodes after their composition, given the Boolean network by DAG.

The number of output edges has the biggest value if most nodes (Eq. 1) calculate the TD using the numerical formula in Eq. 6.

This means that the switching action occurs mostly when the TD is highest.

Therefore, to determine the technology mapping sequence of low power, the TD value of the biggest node must be calculated. As such, the TD value's feasible cluster, including its biggest node, must first be mapped.

2) Node Separation

Node separation is performed in case common node cluster merging is impossible.

In node separation, the number of output edges achieves node separation control and creates a feasible cluster where there are the most nodes.

The expense of a node should be more than two, since the hand of the output at the most nodes is only occasionally achieved.

3)Node Duplication

The output number creates a feasible cluster that uses node duplication at more than two nodes among the nodes that do not create a feasible cluster, using the

common node cluster merging and node duplication method.

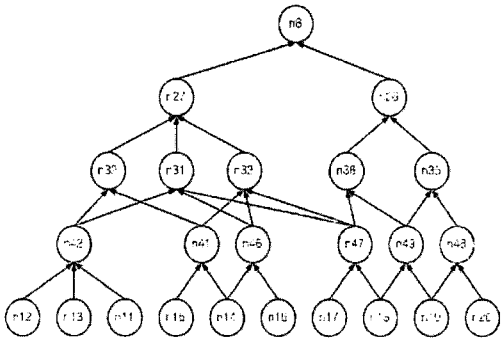
Since the number of nodes increases when node duplication is used for a whole node, this method has a shortcoming in that it increases the feasible cluster generation time.

Therefore, node duplication is achieved at the node where the number of outputs is more than 2 and the expense of the node is one.

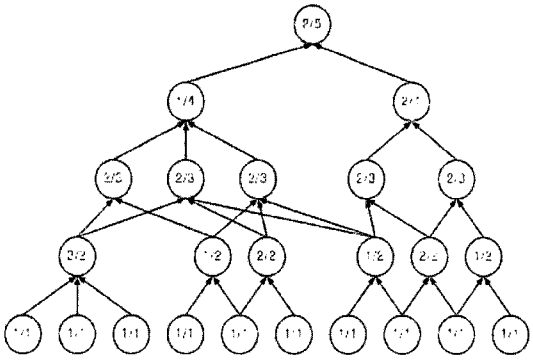
C. CLB Packing

Using the common node cluster merging method and the node separation method, the node duplication, etc. of the feasible cluster creation method created a feasible cluster that is packed to the CLB.

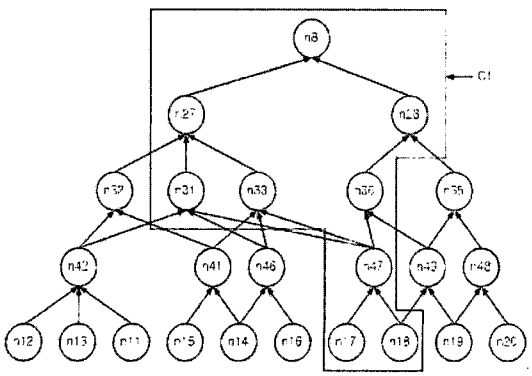
Each feasible cluster becomes packed to the CLB. Fig. 1 shows the whole process of the proposed algorithm.



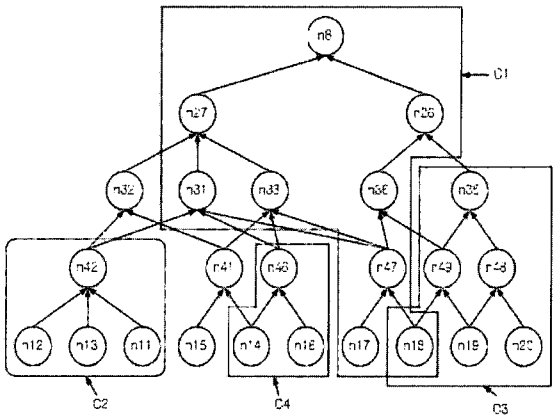
(a) The DAG representation



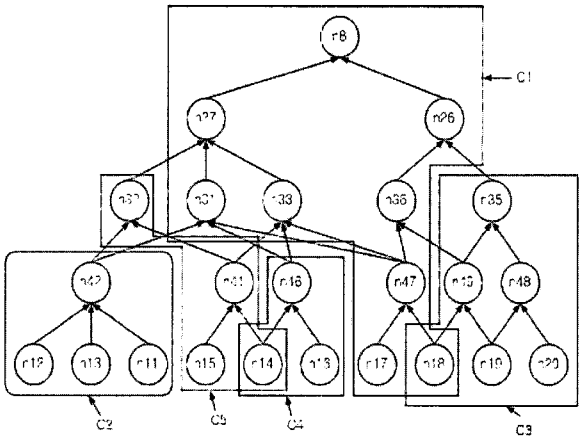
(b) Cost of nodes



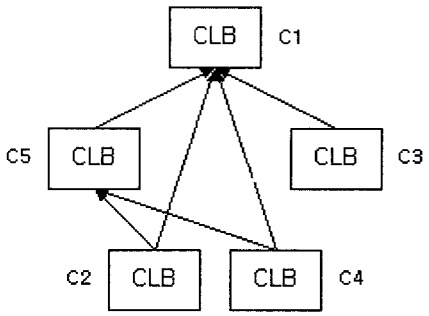
(c) Feasible cluster generation C1 using the common node cluster merging algorithm



(d) Feasible cluster generation C2, C3 and C4 using the node separation algorithm



(e) Feasible cluster generation C5 using the node duplication algorithm



(f) CLB packing

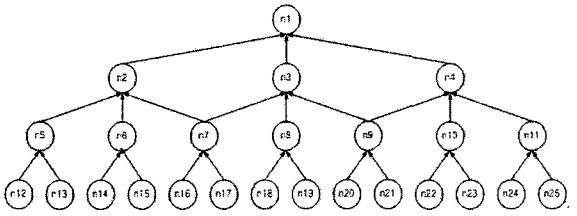
Fig. 1 Example of a proposed algorithm for a partial subcircuit of DALU

D. Trade-off Considering Power, Area, and Delay Time

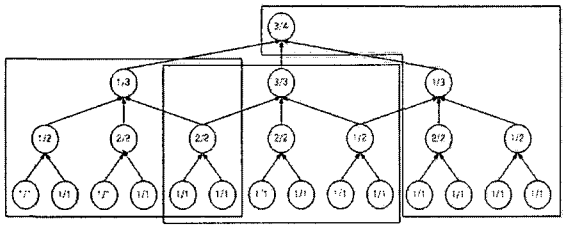
Trade-off that considers power, area, and delay time consumption is a necessary cost to consider the area and the delay time and extracts the optimum technology mapping result as power consumption achieves minimized technology mapping. Fig. 2 compares the results of the wave and a comparative example by parameter when the trade-off is (k, 5, p).

Definition 1

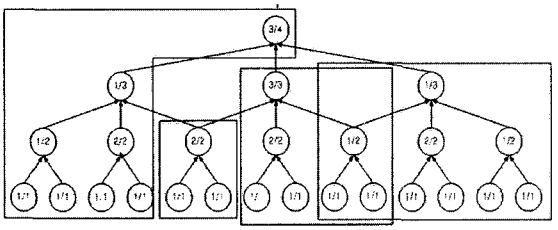
The trade-off of the proposed algorithm is defined as the weight value of power consumption /area/delay time.



(a) The DAG representation



(b) Technology mapping considering only the area and assuming parameter = 0



(c) Technology mapping considering only power consumption and assuming parameter = 1

Fig. 2 Comparison of parameter results

III. RESULTS AND DISCUSSION

The proposed CPLD low-power technology mapping algorithm of a CLB structure that considers trade-off was applied to the benchmarking and measurement of power wastage.

Table 1 Comparison of Areas of the Existing Technology Mapping Algorithm and the Proposed Algorithm

	TEMPLA		PLA Mapping		Proposed Algorithm	
	Block	Power	Block	Power	Block	Power
alu2	56	8.6	56	6.9	54	8.6
alu4	185	32.4	200	31.2	186	33.8
Dalu	483	47.3	480	39.6	476	45.6
ex5p	130	26.2	132	19.3	128	28.3
duke2	68	9.8	69	8.6	67	10.1
t481	97	30.9	94	24.1	94	31.2
Cps	123	31.2	118	28.9	113	33.2
apex4	141	35.6	126	31.5	125	38.3
misex3	141	33.6	141	33.6	135	35.2
Psdes	127	34.8	126	34.2	124	34.8
Sort	105	24.7	102	26.8	99	28.4
Total	1,656	315.1	1,644	284.7	1,601	327.5
Comparison	+3.44%	-3.94%	+2.69%	-15.03%	1	1

The samples in the experiment used the Boolean network of MCNC benchmark circuits, which are offered in SIS by inputs.

The results considered the area of the chosen circuit systems. They are mapped in Table 1.

As can be seen in Table 1, compared to TEMPLA, the proposed CPLD technology mapping algorithm decreased the area by 3.44%, and by 2.69% compared to PLA mapping.

While the area was reduced, however, power consumption was also reduced by 3.94% in PLA mapping but increased by 15.03% in TEMPLA.

IV. CONCLUSION

In this paper, Therefore, the proposed algorithm is proven to be an efficient algorithm for low-power CPLD technology mapping

a CLB-based CPLD low-power technology mapping algorithm considered a Trade-off is proposed.

The proposed algorithm is examined using SIS benchmarks. When the number of OR-terms is five, the experiment results show that power consumption is reduced by 30.73% compared with that of TEMPLA, and by 17.11% compared with that of a PLA map. When the number of OR-terms is seven, the experiment results show that power consumption is reduced by 14.03% compared TEMPLA, and by 8.16% compared with a PLA map.

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