Thermo-Piezoelectric Read/Write Mechanisms for Probe-Based Data Storage

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ABSTRACT

In this paper, a thermo-piezoelectric mechanism with integrated heaters and piezoelectric sensors has been studied for low power probe-based data storage. Silicon nitride cantilever integrated with silicon heater and piezoelectric sensor has been developed to improve the uniformity of cantilevers. Data bits of 40 nm in diameter were recorded on PMMA film. The sensitivity of the piezoelectric sensor was 0.615 fC/nm after poling the PZT layer. And, the 34×34 probe array integrated with CMOS circuits has been successfully developed by simple one-step bonding process. The process can simplify the process step and reduce tip wear using silicon nitride tip.

1. INTRODUCTION

In recent years, probe-based data storage has been studied extensively to overcome the storage density limits of HDD, optical storages and semiconductor memories [1]. Vettiger et al. suggested a thermo-mechanical data storage system where resistively heated AFM tips read and write data bits while scanning over a polymer substrate [2].

We have developed thermo-piezoelectric read/write concept with a resistively heated AFM tip and a piezoelectric PZT sensor [3] as shown in Figure 1. The resistively heated tip records data bits by scanning over a polymer media and the piezoelectric sensor detects data bits by the self-generated charges induced by the deflection of the cantilever as it scans across the indentations on the polymer media. In a piezoelectric cantilever, like PZT, the mechanism of sensing is as follows; as the PZT cantilever scans across the indentation of a polymer film, the cantilever deflects along the indentation of the film, causing stress on the PZT film. The variation of stress in the PZT film produces self-generated charges on the surface of the PZT capacitor without applying voltage. The charges are not generated by the absolute stress, but by the variation of stress. Therefore, the piezoelectric sensing method has the advantages of low power consumption, no off-set voltage and high reading speed compared to thermo-resistive sensing method of IBM. Furthermore, the power consumption during writing can be reduced by selecting low Tg polymer media because the media is not reflowed during reading process with no tip heating.

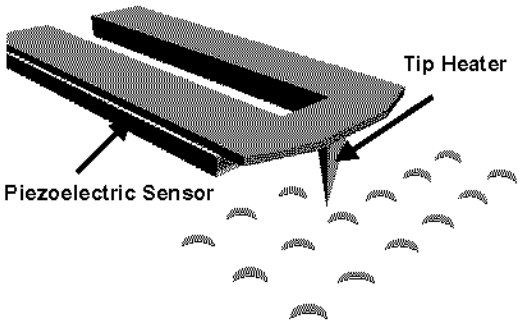


Figure 1 . Thermo-piezoelectric R/W mechanism.

The uniformity in the initial bending of cantilevers is crucial for reliable read/write operation in probe-based storage, which is not attainable with probe array made of SOI wafer due to un-uniformity of device layer of SOI wafer and in tip etching process. We have developed the silicon nitride cantilever with silicon tip heater and piezoelectric sensor to improve the uniformity and the mechanical stability of the probe array.

For high density probe-storage applications, probe arrays should be integrated with ASIC circuits which access the individual cantilever for read/write and control. Previously, Vettiger et. al proposed a new micro-device transfer/interconnect method (DTM) compatible with the CMOS technology. However, this

technique consists of two bonding processes to expose tips; in the first step, cantilevers are formed out of a SOI wafer and the tips are formed on the surface. These cantilevers are transferred onto a glass wafer and the bulk silicon is removed. In the second step, the cantilevers on the glass wafer are transferred onto the CMOS wafer [4].

We have developed a novel wafer-level transfer method in which probe arrays are integrated with a CMOS circuit by single-step bonding process.

2. THERMO-PIEZOELECTRIC READ/WRITE

In this work, we have developed the thermo-piezoelectric cantilever using the silicon nitride film deposited by LPCVD (Low Pressure Chemical Vapor Deposition) method for thickness uniformity of the cantilevers. The silicon nitride cantilever shows uniform initial bending compared to silicon cantilever because the silicon nitride film deposited by LPCVD

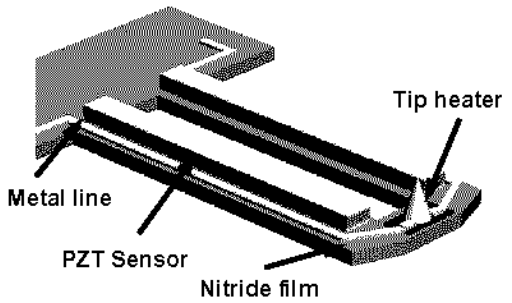


Figure 2. Schematic drawing of nitride thermo-piezoelectric cantilever.

method has superior thickness uniformity. The PZT sensor and the silicon tip heater are formed on the silicon nitride cantilever as shown in Figure 2. The silicon heater is connected through the metal line to supply electrical power. Using these nitride cantilevers, very uniform probe array can be made for reliable read/write operation of probe-based data storage.

Fabrication process for the cantilevers is summarized in Figure 3. The SOI wafers with nitride buried layer were made to make silicon tips for the first time. The oxidized wafers and the low stress nitride deposited wafers were fabricated to make the SOI wafer (a). The wafer pair were cleaned in RCA1 [NN4OH : H2O2 : H2O (1:1:4)] and SPM [H2SO4 : H2O2 (4:1)] solutions. And then, the wafer pair were initially bonded by pressing the center of the wafer at

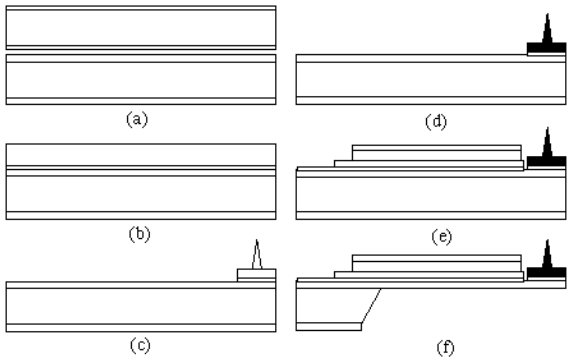


Figure 3. Fabrication process of nitride thermo-piezoelectric cantilever.

room temperature followed by annealing for 2 hours at 1000℃ to improve the bond strength (b). After the silicon tips and the electrical silicon contact regions were formed on the nitride film (c), thermal oxide film of 50 nm thickness was grown on it to reduce surface damage resulting from ion implantation. Boron was implanted at 40 keV with a dose of 5 x 1014 cm-2 at the silicon tip heater regions and with a dose of 5 ×1015 cm-2 at the silicon electric contact regions (d). Then, the wafers were subjected to furnace annealing in N2 ambient at 900℃ for 30 minutes and the oxide film on the surface was removed by etching in BOE solution.

After depositing LPCVD oxide film with 200 nm thickness to protect inter-diffusion between PZT and Si layer, PZT capacitors were formed as described in the previous work [5]. The bottom electrodes were formed by sputtering thin titanium (Ti) adhesion layer, followed by 120-nm thick platinum (Pt) layer. The PZT layer was formed by sol-gel process. The PZT film was annealed at 650℃ for 1 minute using the Rapid Thermal Annealing (RTA) process. The resulting PZT film was 300-nm thick and its composition was near the morphotropic phase boundary. On top of the PZT film, RuO2 film was deposited as the top electrode. The PZT capacitor structure was patterned using an inductively coupled plasma reactive ion etching system (e). The Pt/Ti pads were formed by sputtering and lift-off process. Finally, backside silicon was selectively removed in an aqueous potassium hydroxide (KOH) solution (f). After the wafers were diced into individual cantilevers, the tips on the cantilevers were heated to record a series of data bits on a polymer media. For polymer media, 40-nm thick PMMA film was prepared by spin coating method.

Figure 4 shows the images of the fabricated silicon nitride cantilevers integrated with silicon tips and PZT sensors. The silicon heaters and the PZT sensors on the silicon nitride cantilevers are clearly defined in the figure. The fabricated cantilevers are slightly bent upward. The thickness uniformity of the nitride film is below 2% over the 4 inch wafers. The cantilever

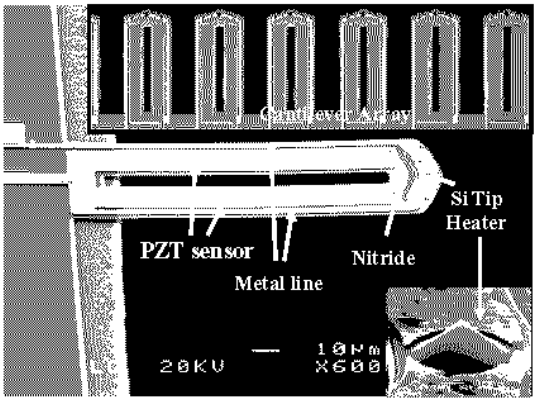


Figure 4. SEM image of the fabricated cantilever.

array shows uniform bending status. The length of the cantilever is 120 ㎛, and the thickness of the nitride film and the PZT film is 500 nm and 300 nm, respectively.

Figure 5 is the schematic drawing of the piezoelectric sensing system where piezoelectric charges are collected from the PZT sensors as the tips are deflected over the bit indentations [6]. The generated charges are amplified by a charge amplifier (model No.: CS515-2, Clear Pulse Company). The amplified signals can be compared to the initial setting value using a comparator to differentiate the data to be

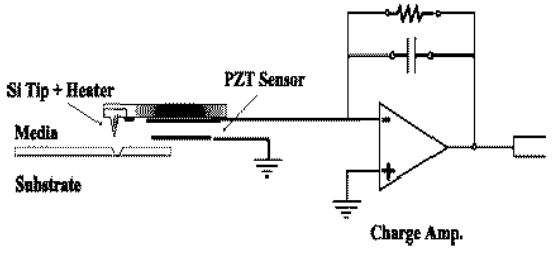


Figure 5. Schematic of thermo-piezoelectric read/write.

either "0" or "1"

To measure the sensitivity of the PZT sensors, the induced charges were collected with various cantilever deflection, as shown in Figure 6. The deflection was measured using a stacked piezoblock which consists of a series of stacked PZT capacitors and produces a

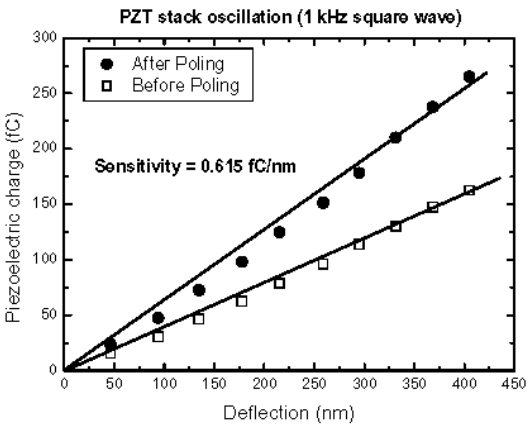
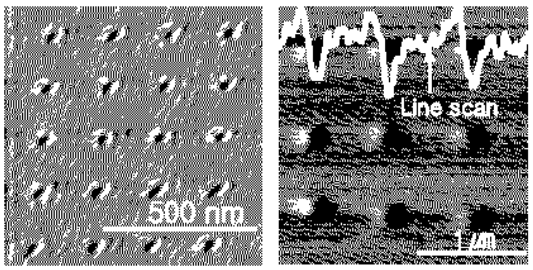


Figure 6. Piezoelectric charge output as a function of various cantilever deflections.

known displacement at a given voltage. Piezoelectric charges were generated from the PZT sensor as the piezoblock moves up and down by applying voltage while the tips just contacted the piezoblock. These charges were collected by a charge amplifier with gain of 2V/pC at a square wave of 1 kHz. The charge signal was linearly proportional to the cantilever deflection. The sensitivity was 0.4 fC/nm and 0.615 fC/nm without and with poling of the PZT film. The PZT film reached the saturated state by poling treatment, which led to the increase of the sensitivity.

Using the fabricated cantilever, a series of data bits were written on a PMMA media, as shown in Figure 7(a). A voltage of 10V with pulse width of 20 micro second was applied under loading force of about 200 nN. Indentation data bits of about 40 nm were recorded on PMMA film. The writing voltage can be further decreased by reducing the silicon heater size. Figure 7(b) shows the piezoelectric charge outputs



(a) Written data bit (b) Piezoelectric read -out

Figure 7. Thermo-piezoelectric read and write on PMMA substrate.

obtained on PMMA media with the data bits of about 150 nm. The readback signal from PZT sensors was observed from the line scan data. As the tip scans across the indentation, negative charges are generated.

The signal from the indentation was clearly distinguished from the noise signal. However, for the data bits below 40 nm, the piezoelectric charge outputs were not clearly differentiated from the noise.

To detect smaller bits, we are attempting to increase the aspect ratio of the indentations and increase the signal to noise (S/N) ratio. The depth of the indentations was below 20nm when the bit width was 150 nm. To improve the indentation profile, development of new media material and optimization of writing condition are crucial. The sensitivity can be increased by optimizing the PZT layer and the cantilever structure. The noise signal from the flat area is mostly due to the system noise. We are trying to find and eliminate the exact sources of the electric noises to improve the S/N ratio.

3. INTEGRATION OF PROBE ARRAY WITH CMOS CIRCUITS

In previous chapter, the uniformity of the initial bending of the cantilevers could be greatly improved using the silicon nitride film deposited by LPCVD method. However, these kind of cantilevers cannot be directly integrated with CMOS circuits because the tips are not exposed on the surface after bonding process with CMOS circuits.

In this research, a novel wafer-level transfer method of 2-dimensional cantilever arrays on a conventional CMOS circuit has been developed for the high density probe-based data storage devices. The cantilevers and the tips are formed with silicon nitride on a conventional p-type silicon wafer and poly silicon heaters and piezoelectric sensors are integrated with

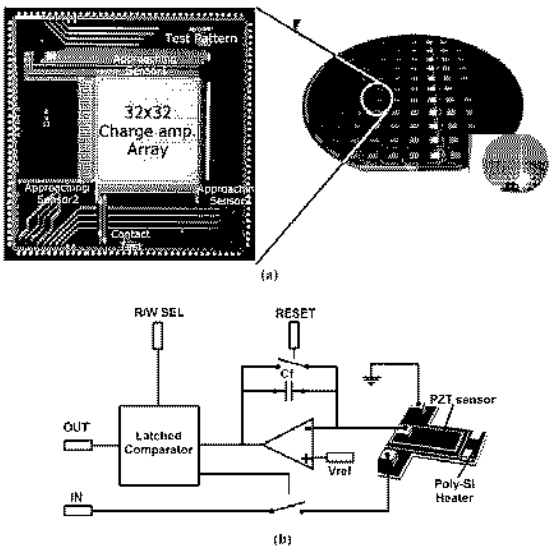


Figure 8. The fabricated CMOS wafer with Charge amplifier circuitry (a) Microscope image of 32X32 cantilever array fabricated in 5inch wafer (b) Block diagram of read/write circuit per one cantilever Thermo-piezoelectric R/W mechanism.

the cantilevers. In this process, the tips are formed in downward direction unlike the previous silicon tips. So, the cantilevers can be directly transferred to the CMOS wafer by one-step bonding process. Our new fabrication process provides simple wafer level transfer method of uniform and mechanically stable cantilever array.

Wafer level transfer of cantilever arrays to the CMOS wafer is explained here. The CMOS wafer consists of arrays of charge amplifier circuits which amplify the signals from the thermo-piezoelectric cantilevers. The wafer was fabricated with 0.8um and 2P2M(2-poly-2-metal) process, provided by a standard CMOS foundry in ETRI(Electronics and Telecommunications Research Institute) , Korea.

Figure 8(a) shows the fabricated CMOS wafer by using 0.8 m conventional CMOS technology. The circuitry for read and write channel per each cantilever are illustrated in Figure 8(b). The read channel includes a charge amplifier and a latched comparator per one cantilever and the write channel includes a switch transistor per cantilever. The latched comparator converts analog output signals from the charge amplifier to digital output signals and stores the data signals. Using an array of this circuit, fully parallel reading operation can be achieved. The output

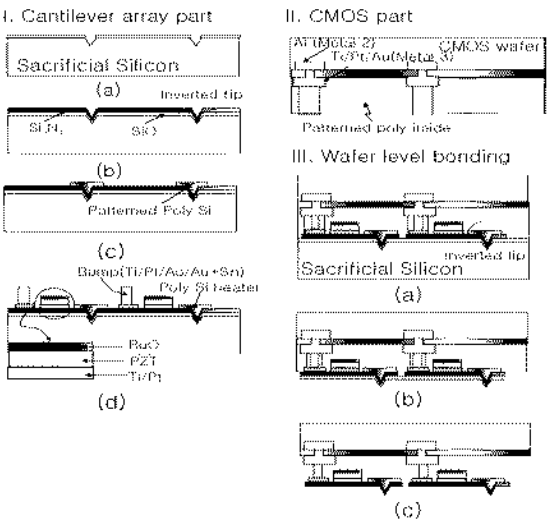


Figure 9. Fabrication process of wafer-level thermo-piezoelectric Si3N4 cantilever transferred on a conventional CMOS wafer.

signal can be acquired from the stored data signals in latched comparators by a column time-multiplexed addressing scheme similar to those implemented in DRAMs.

The wafer-level transfer process of 2-dimensional cantilever array on a conventional CMOS wafer is

illustrated in Figure 9. Some of the process steps were adopted from the mould-and-transfer method [7-8].

First, inverted pyramidal pits are formed by KOH anisotropic etching on a single crystal silicon wafer with Si3N4 thin film as a masking layer (Ⅰ (a)). And 300nm of thermal oxide is grown for the sharpening the tips. Low Pressure Chemical Vapor Deposition (LPCVD) Si3N4 thin film is deposited for the tips and cantilevers (Ⅰ (b)). Si3N4 thin film formed by LPCVD method has superior thickness uniformity and mechanical stability compared to the device silicon layer of a SOI wafer. It is noted that the uniformly formed tips are directed opposite to the wafer surface.

On the silicon nitride film, 300nm of LPCVD poly silicon film are grown and patterned to form the heaters (Ⅰ (c)). Phosphorus is implanted with a dose of 5 x 1014 cm-2 at the heater region and with 1 ×1016 cm-2 at the electric contact region of the poly silicon, both at the energy of 70KeV. Then, the wafer is subjected to a furnace annealing in N2 ambient at 900℃ for 30 minutes.

LPCVD oxide film of 200 nm thick is deposited over the patterned wafer to prohibit the inter-diffusion between PZT and silicon layer. And PZT capacitors are formed as described in the previous chapter (Ⅰ (d)). For the electrical connection to the CMOS wafer, bumps are formed by e-beam evaporation and lift-off process. The bump layer consists of a pad layer of Ti(50nm)/Pt(200nm)/Au(200nm) stack and 3μm thick Au:Sn (80:20) layer which will be eutectically bonded to the CMOS wafer. At this stage the cantilever array is ready to be transferred.

On the CMOS wafer (II), Metal 3 layer of Ti(20nm)/Pt(100nm)/Au(300nm) stack is patterned with lift-off process. The Metal 3 layer acts as the platform for the eutectic bonding process. Using this layer, Metal 2 of Al and bumps on the cantilever wafer are electrically connected. And then, 2μm of photosensitive polyimide layer is spun and patterned and cured.

The cantilever array part and the CMOS part are assembled using the wafer level bonding method (III (a)). The two wafers are pressed with 10 bar at 300 ^{o}C for 20 minutes for the eutectic bonding of Au:Sn. After the wafer-level bonding, the sacrificial silicon layer is grinded to about 50 μm and then etched away with XeF_2 gas with the thermal oxide at the bottom of the cantilevers as the etch stop layer (III (b)). Finally oxide at the bottom of the tip is selectively removed in BOE and polyimide is removed in O_2 plasma (III (c)).

34X34 thermo-piezoelectric Si3N4 cantilever array was successfully transferred on a CMOS wafer by the wafer level transfer-method mentioned above. The outermost two rows and columns of the array are sacrificial cantilevers to guarantee identical fabrication environment for the 32X32 active cantilevers. With these dummy cantilevers, the fabrication yield can be increased.

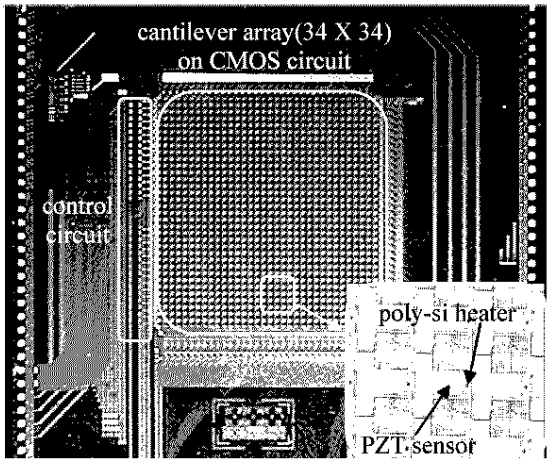
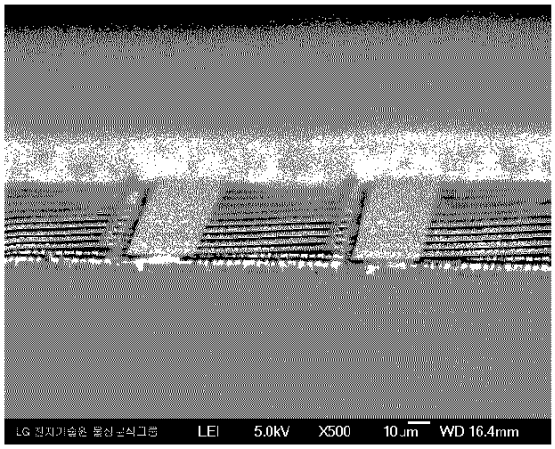


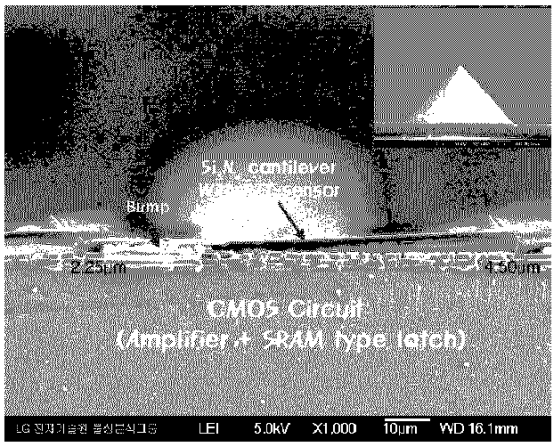
Figure 10. Optical image f the transferred 34 X 34 cantilever array on a CMOS wafer.

Figure 10 shows the transferred cantilever arrays on a CMOS wafer after the bonding and removing of the sacrificial silicon. Each array contains 1024 cantilevers. Integration density is 100 cantilevers/mm^2 and 300 electrical interconnects/mm2 were made within a cantilever array (3.4mm X 3.4mm). The tips are protected until the last step so that they remain sharp through this wafer level bonding process. The electrical contact resistance is well below 0.5 Ohm. Die-shear test has been performed to check the durability of the wafer level bonding. The die shear strength of the bumps was 2-5kgf/mm^2 and this is well above the internationally accepted IC industry's standard of 1kgf/mm^2. The inserted figure is an enlarged view of the free standing cantilevers with PZT sensors for reading and silicon nitride tips with poly-Si heater for writing data bits. The cantilever is typically 70μm long and 45μm wide and 300nm thick.

Figure 11 (a) is a slanted view of the transferred cantilevers in Figure 10. Figure 11 (b) is a closed view of one of the free-standing cantilevers. The cantilevers are bonded to the CMOS wafer with a gap of about 2.25 μm and they are tilted upward by about 1.8 degrees. One side of the pyramidal tip is 5 μm and the tip height is about 3.5 μm. The size of the tips determines the thermal mass of the heater and thus the thermal time constant of the system. To reduce the power consumption and to increase the speed of writing the tips should be as small as possible. When the tip becomes smaller the cantilevers needs to be



(a)



(b)

Figure 11. SEM image of transferred cantilever array.

bent to the direction that keeps the distance between the CMOS wafer and the polymer media to avoid the face to face contact of them during the read and write operation.

The bending of the cantilevers can be controlled mainly by adjusting the deposition condition of LPCVD silicon nitride film. The residual tensile stress of the silicon nitride film can be adjusted from less than 100MPa to 1.2GPa by changing the stoichiometry of the film. The initial bending of the cantilevers as well as the height of the tips should be very uniform and be well under control in order to minimize the variation in loading force of all the cantilevers in an array. This is a crucial factor to the read/write characteristics and the wear of the tip and media. Previous investigations on wear problem suggest that the uniformity of the cantilever bending across a whole chip should be less than 500nm [9],

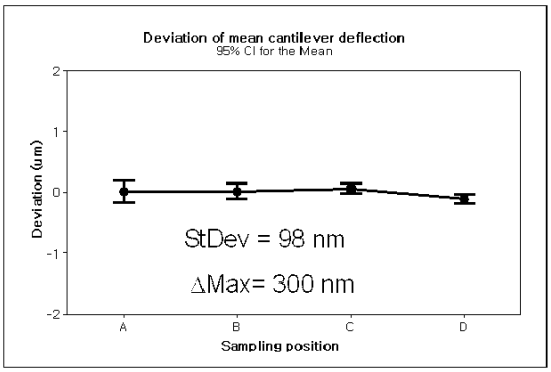


Figure 12. Deviation of initial bending in probe array.

when the spring constant of the cantilever is 1-0.5 N/m.

Figure 12 shows the deviation of deflection of 60 cantilevers from randomly selected areas out of the 34X34 cantilevers array. The standard deviation of the deflection is about 100nm and the maximum deviation is about 300nm. With the spring constant of the cantilever being 1N/m, the deviation of the cantilevers meets the requirements mentioned above. There were some areas where the variation is relatively larger than others. It was observed that in some areas polyimide was not fully removed after the final O_2 plasma ashing. These polyimide residues can contribute the abnormal deflection of cantilevers.

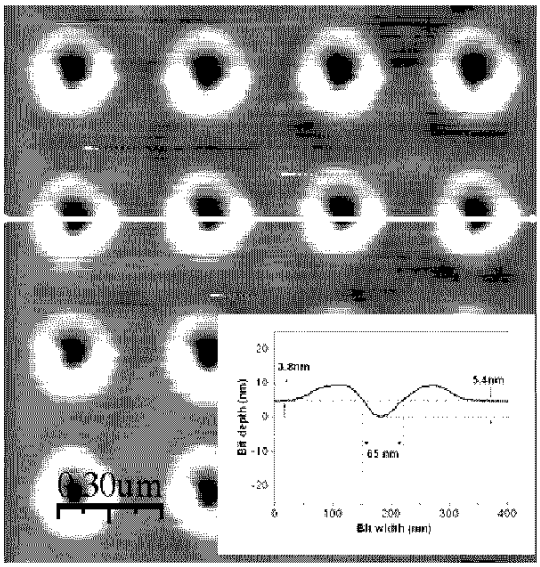


Figure 13. Data bits written by transferred thermo-piezoelectric Si3N4.

A series of data bits were written on a PMMA media with one of the cantilevers transferred by the wafer level bonding method, as shown in Figure 13.

The data bit indentation is about 5.4nm deep and has a diameter of 65nm. The polymer around the indentation has been piled up to about 3.8nm above the initial surface. These topographic pile-ups are regions susceptible to wear during the operation. The presence of pile-ups also limits the writing density. However, this phenomenon of polymer pile-up can be used for erasing of written bits [1]. Now, we are working on read/write test using the arrayed cantilevers.

4 CONCLUSIONS

The thermo-piezoelectric mechanism has been developed using the integrated silicon nitride cantilever with silicon heater and piezoelectric sensor for high density probe-based data storage. Data bits of 40 nm in diameter were recorded on PMMA film. The sensitivity of the piezoelectric sensor was 0.615 fC/nm after poling the PZT layer. And, using simple one-step bonding process, the 34×34 probe array integrated with CMOS circuits has been successfully developed. The process can simplify the process step and reduce tip wear using silicon nitride tip. The initial bending of the cantilevers was very uniform and controllable because the cantilevers were made of silicon nitride film. Further studies are in progress to read and write data bits using this cantilever array with CMOS control circuit and to build the overall system.

ACKNOWLEGEMENT

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