Ferroelectric ultra high-density data storage based on scanning nonlinear dielectric microscopy

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Abstract

Nano-sized inverted domain dots in ferroelectric materials have potential application in ultrahigh-density rewritable data storage systems. Herein, a data storage system is presented based on scanning non-linear dielectric microscopy and a thin film of ferroelectric single-crystal lithium tantalite. Through domain engineering, we succeeded to form an smallest artificial nano-domain single dot of 5.1 nm in diameter and artificial nano-domain dot-array with a memory density of 10.1 Tbit/inch^2 and a bit spacing of 8.0 nm, representing the highest memory density for rewritable data storage reported to date. Sub-nanosecond (500psec) domain switching speed also has been achieved. Next, long term retention characteristic of data with inverted domain dots is investigated by conducting heat treatment test. Obtained life time of inverted dot with the radius of 50nm was 16.9 years at 80°C. Finally, actual information storage with low bit error and high memory density was performed. A bit error ratio of less than 1×10^{-4} was achieved at an areal density of 258 Gbit/inch^2. Moreover, actual information storage is demonstrated at a density of 1 Tbit/inch^2.

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1. Introduction

With the advance of information processing technology, the importance of high-density data storage is increasing. Studies on thermal fluctuation predict that magnetic storage, which plays a major role in this field, will reach a theoretical limit in the near future, and thus a novel high-density storage method is required.

Ferroelectrics can hold bit information in the form of the polarization direction of individual domains. Moreover, the domain wall of typical ferroelectric materials is as thin as the order of a few lattice parameters, which is favorable for high-density data storage. Therefore, we have been studying ferroelectric high-density data storage based on scanning non-linear dielectric microscopy (SNDM) [1] and have previously reported the successful formation of nano-sized inverted domain dot arrays at a data density of 1.50 Tbit/inch^2 in a congruent $LiTaO_3$ (CLT) single crystal thin plate.[2] In addition to a high memory density, recording media in large-capacity memory devices also requires excellent high-speed writing characteristics. In ferroelectrics, the writing time is determined by the speed to reverse the polarization immediately beneath the probe tip. We have demonstrated nano-domain dot formation with application of a 4 ns, 10 V pulse on a 60-nm-thick CLT. [3]

In this paper, we report that considerable progress has been made towards the realization of ferroelectric technology for data storage using SNDM and a CLT thin plate.

At first we performed the fundamental studies on highest memory density and fastest switching speed in ferroelectric data storage and succeeded to form a smallest artificial nano-domain single dot of 5.1 nm in diameter and then to form a nano-domain dot-array with an areal density of 10.1 Tbit/inch^2. A sub-nanosecond (500 psec) domain switching speed was also successfully achieved.

Next, long term retention characteristic of data with inverted domain dots formed on CLT was investigated by conducting heat treatment test. To predict the shrinking speed at lower temperature, we used Arrhenius equation in reaction kinetics with activation energy and frequency factor determined by the test. Calculated life time of inverted dot with the radius of 50 nm was 16.9 years at 80°C.

Finally, actual information storage with low bit error and high memory density was performed. As a result, a bit error ratio (BER) of less than 1×10^{-4} was achieved at an areal density of 258 Gbit/inch^2. Moreover a data bit array of 128×82 was successfully written at an areal data storage density of 1 Tbit/inch^2 with a bit error rate of 1.8×10^{-2}.

2. Experimental Setups

The ferroelectric data storage system has been developed based on SNDM for fundamental read/write experiments. Figure 1 shows the schematic diagram of this system used in this study. The probe is composed of a conductive cantilever and an oscillator. The contact load of the tip is kept constant using AFM technique in order to ensure stable actions of the system and minimize tip damage. (Although the tip dose not have to touch the surface of the recording medium to read/write the domain dot if we use NC-SNDM technique, [4] the gap between the tip and the medium must be small as much as possible to create a small domain dot. Therefore, in this fundamental study, we simply operated the SNDM at the contact mode.) Polarization distinction is performed by detecting the small variation in resonance frequency caused by the capacitance variation due to the nonlinear dielectric response induced by alternating voltage applied to the ferroelectric recording medium, because the sign of the capacitance variation depends on the polarization direction. The probe generates FM signals containing the information of polarization direction. The inner oscillator mounted in the probe is tuned to the

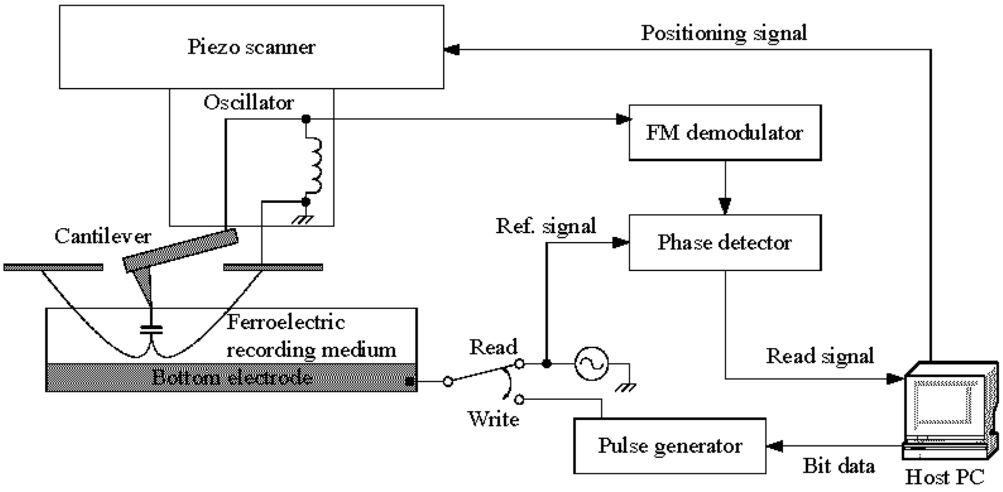


Fig. 1 Ferroelectric data storage system based on SNDM.

resonance frequency determined by the capacitance just under the tip of the cantilever and the inductance embedded in the circuit. By detecting this FM signal using a FM demodulator and a phase detector, a voltage signal proportional to the capacitance variation is obtained. On the other hand, writing is carried out by applying a relatively large voltage pulses to the ferroelectric recording medium and locally switching the polarization direction. The pulse generator is connected to the bottom electrode of the medium, thus the positive domains (which are observed on the surface of the probe side) are written by the positive voltage pulses and the negative domains are the converse. The positive domains are defined as the data bits of `1' in this paper. Piezoelectric scanners with displacement sensors are employed for highly accurate positioning. Two types of cantilevers were used as read/write probes. Conductive-diamond-coated cantilevers with the tip radius of 50 nm were used for the purpose of studying the basic recording technology, because this type of probe has excellent durability, and would be valid for practical use. Metal-coated cantilevers with sharp tip radius of 25 nm were also

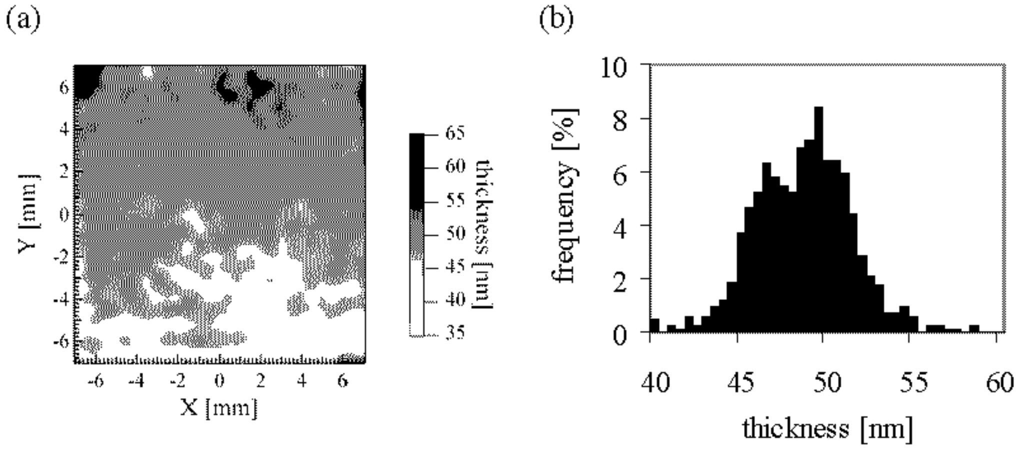


Fig. 2 Thickness distribution in a CLT single-crystal recording medium: (a) two-dimensional mapping image; (b) histogram.

used as probe in order to write the higher-density data. CLT single crystal was selected as a recording medium. When forming a reversed domain by applying a voltage to a specimen using a sharp-pointed tip, the electric field is highly localized immediately beneath the tip. Therefore, the preparation of thin and homogeneous specimens is a matter of the highest priority. In this study, we have succeeded in obtaining very thin and uniform CLT recording media with thicknesses of 10–60 nm—much smaller than those used in a previous report.[1] These specimens were fabricated by mechanically polishing a single-crystal wafer, which was mounted on a metal (chromium)-coated CLT single crystal wafer with a thickness of 400–500 μm, to a thickness of approximately 0.5 μm, followed by electron cyclotron resonance (ECR) dry etching to the desired thickness. The same $LiTaO_3$ material was used for the substrate and the polished thin film to ensure matching of the thermal expansion coefficients. The thickness of the fabricated thin media was measured using a spectrum reflectance thickness monitor (Otshuka Electronic FE-3000) with nanometer scale precision. The area of the sample was 14×14 mm^2, all of which was usable for data storage. As an example, Fig. 2 shows the typical thickness distribution in a recording medium. The average thickness was as thin as 48.5 nm and the variation was only 3.1 nm in standard deviation. Thus, we now have a ferroelectric medium with sufficient homogeneity and space to perform practical information storage on the Tbit/inch^2 density scale.

3. Fundamental studies on highest memory density and fastest switching speed in ferroelectric data storage

Using the above mentioned recording medium, we first examined the effect of a small dc offset voltage on the pulse amplitude and duration needed to switch and stabilize the nano-domains. All of the nano-domain dots obtained in this section were formed using a conductive cantilever tip with a radius of 25 nm. A dc offset voltage is applied to the sample following an initial writing pulse voltage. Figure 3 shows SNDM images of domain dot arrays formed on a 45-nm-thick single crystal CLT plate with dc offset voltages of -0.5, 0, 0.5 and 1.0 V, respectively. An array of 6x6 pulses was applied by varying the offset voltage. From left to right in Fig.2, the pulse amplitude was varied from 10 to 5 V in 1 V steps, and from top to bottom, the pulse duration was varied from 1 msec to 10 nsec in logarithmic steps. Both the pulse amplitude and the application time required to achieve reversal of polarization vary significantly with even small variation in the dc offset voltage following the pulses.

These results indicated that application of a very small dc offset voltage is very effective in accelerating the domain switching speed and in stabilizing the reversed nano-domain dots. In other words, the offset voltage application suppresses the domain backswitching effect known to occur in CLTs (This has been thought to be attributed to the non-stoichiometric Li-deficiency defects which pin domain-wall movement. [3,4]) , and smaller pulse amplitudes and

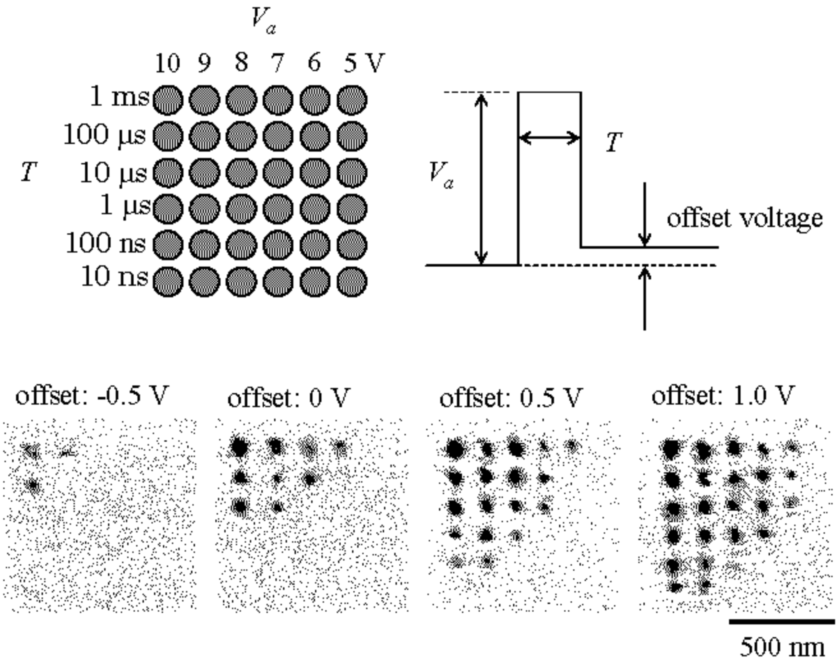
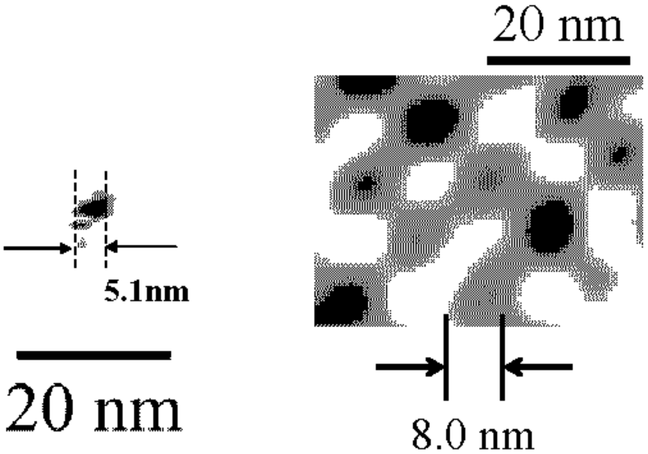


Fig.3 Domain dot arrays written on a 45-nm-thick CLT single crystal using voltage pulses with dc offset.



(a) (b)

Fig. 4 (a) Smallest artificial nano-domain single dot of 5.1 nm in diameter. (b) Artificial nano-domain dot-array with a highest memory density of 10.1 Tbit/inch^2 and a bit spacing of 8.0 nm.

shorter pulse durations are needed to form the nano domain dots under the offset voltage application.

To demonstrate application of this acceleration effect of the offset voltage to high-density data storage, we formed a small artificial nano-domain single dot of 5.1 nm in diameter and also formed an artificial nano-domain dot-array with a memory density of 10.1 Tbit/inch^2 and a bit spacing of 8.0 nm, as shown in Fig.4. The single dot in Fig.4 (a) was formed by a 8.2 V, 100 ns pulse application with a dc offset of 1.0 V on a CLT thin plate with a thickness of 40 nm and the dots in Fig.4(b) were formed by a 7.8 V, 20 ns pulse application with a dc offset of 1.5 V on a CLT thin plate with a thickness of 35 nm. As the dots in the 10.1 Tbit/inch^2 array are sufficiently resolvable for practical data storage, it is fully expected that, with further refinements, this system will be applicable as a storage technology. We have thus demonstrated, using a ferroelectric medium and nano-domain engineering, that rewritable bit storage at a data density of around 10.1 Tbit/inch^2 is achievable. To the best of our knowledge, this is the highest density reported for re-writable data storage, and is expected to stimulate renewed interest in this approach to next-generation ultra-high-density re-writable data storage systems.

We also investigated the high-speed switching of nano-scale domains on the CLT thin plate. In our previous report, the shortest pulse duration for successful polarization switching of the nano-domain was 4 nsec due to limitations in the performance of the pulse generator used in the study.[3] Using a faster pulsar (Picosecond pulse Labs, 10,060A), and a very thin medium with a thickness of 18 nm fabricated using the above-mentioned method, we succeeded in switching the nano-domain at a speed of 500 ps without the dc offset voltage. Fig. 5 shows the dot shape and a cross sectional image of the nano-domain dot formed by a 10 V, 500 ps pulse.

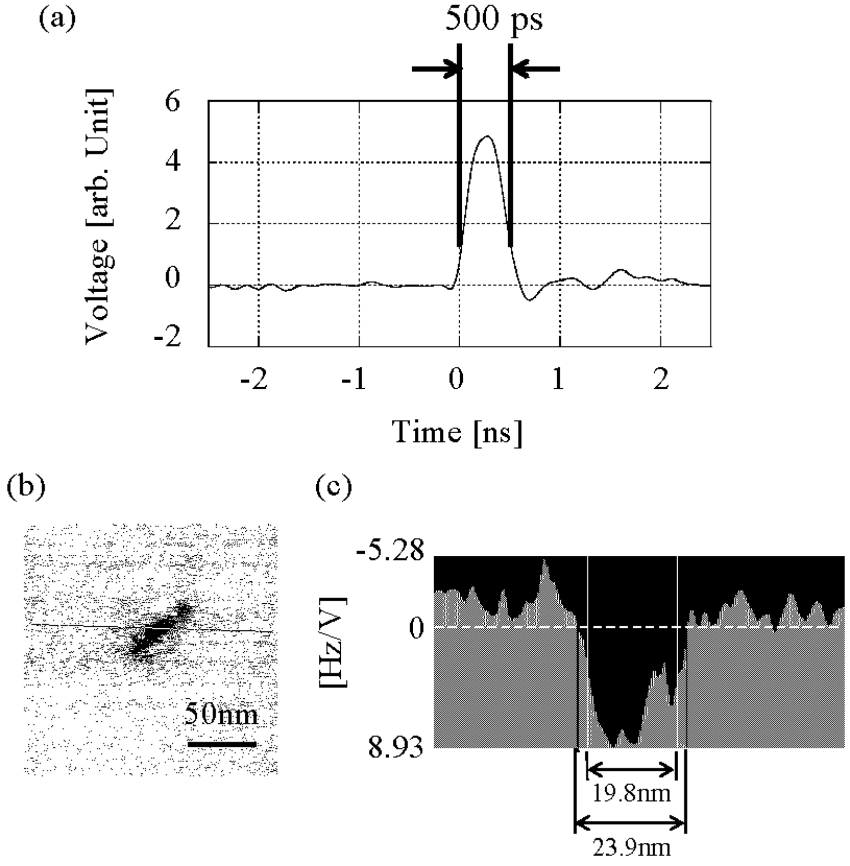


Fig. 5 Nanodomain dot formed on an 18- nm-thick CLT single crystal using 500 ps voltage pulse: (a) wave form of voltage pulse; (b) two-dimensional image; (c) cross-sectional image.

4. Long Term Retention Characteristic of Small Inverted Dots

Another required characteristic for the realization of ferroelectric data storage is long-term-retention characteristic. This means data with inverted domain array on ferroelectric medium must remain for long term. In the actual memory device, much longer term data retention characteristic over 10 years is required. Therefore, in this study, we have investigated retention characteristics of nano-domain dot formed on CLT ferroelectric data storage medium.

To investigate long term retention characteristic of data with inverted domain dots formed on CLT, we conducted heat treatment test. The reason is as follows; the free energy of ferroelectric material has two local minimum points. There is energy barrier between two local minimum points and the system requires high energy enough to surpass the energy barrier when data with inverted domain dots erase by switching back of domain. To accelerate switching back of domain, we left CLT specimen with inverted-domain-dot array in very high temperature atmosphere and compared the shape of the inverted domain dots before and after the heat treatment.

At first, we prepared CLT specimens with thickness of 80nm. Fig.6 A-1, B-1, C-1, and D-1 show the images of inverted domain dot array formed on those CLT specimens, where radius of each dot is approximately 50nm and the distance of each dot is shown if Fig.6E. After that we left these specimens in an electric furnace whose inside temperature was kept at 300 °C, 280 °C, 250 °C and 220 °C for 16hours, 30hours, 42hours and 96hours respectively. The temperature rate of heating and cooling was controlled to be 1 °C /1minute.

Fig.6 A-2, B-2, C-2 and D-2 show the images of inverted domain dot array after heat treatment. In every heat treatment test, each dot shrinked. We can explain this phenomenon from the point of view of stored energy. Total energy W in the system can be written as follows,

$$W=W_{es} + W_{wall} \qquad (1)$$

where W_{es} and W_{wall} denote electrostatic energy and wall energy, respectively. W_{es} is an energy by electric field which makes polarized charge, and W_{wall} is an energy by anti-parallel dipole in domain boundary region. However, polarized charge on surface of ferroelectric medium is compensated. Also pyro-electrical charge which is generated under heating and cooling is compensated because variation rate of temperature is enough slow (1 °C /1minute) in this experimental condition adopted here. For above reason, electrostatic energy W_{es} is constant, and W_{wall} has to get small so that total energy W gets small. Since each dot is away

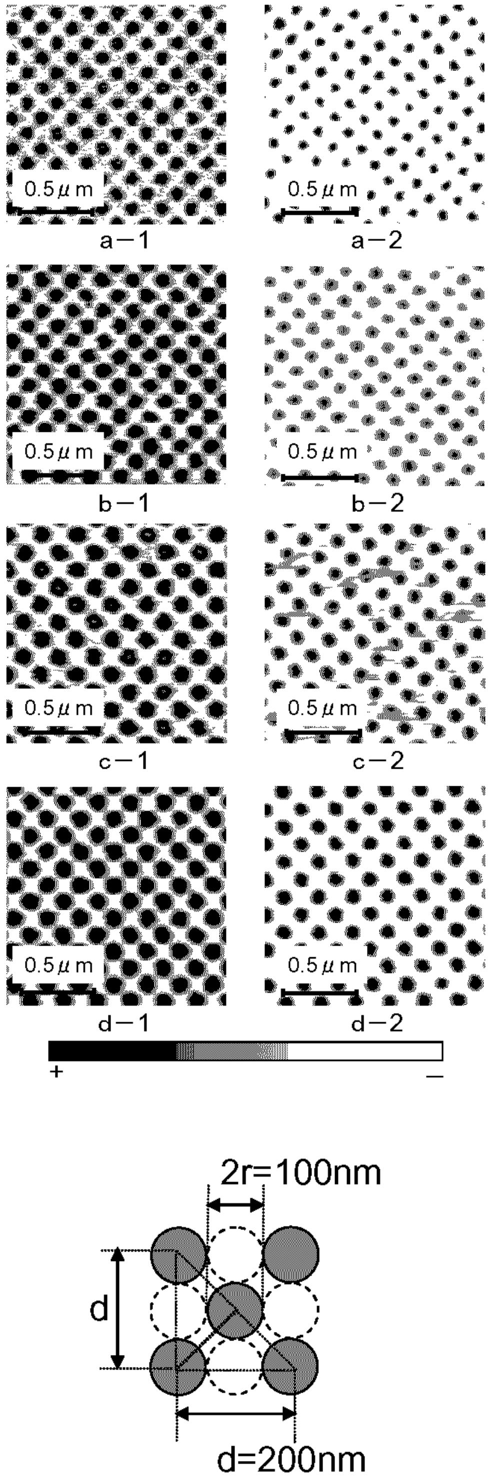


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Fig. 6. Images of inverted domain dot array formed on 80nm thick CLT specimens. a-1, and a-2 : Before and after heat treatment in 300 ℃ for 16hours. b-1, and b-2 : Before and after heat treatment in 280 ℃ for 30hours. c-1, and c-2 : Before and after heat treatment in 250 ℃ for 42hours. d-1, and d-2 : Before and after heat treatment in 220 ℃ for 96hours.e shows the alignment of dots in forming dot array.

from another, the length of domain wall should decrease to make W_{wall} small. (If each dot is close to another, adjacent dots will merge.) Black circles in Fig.7 show the results of these heat treatment test as temperature dependant of shrinking speed of inverted dot radius.

To predict the shrinking speed at lower temperature, we used Arrhenius equation in reaction kinetics. When region of + domain switches to – domain, we can describe the state transition as follows,

$$\mathrm{A} \rightarrow \mathrm{B} \tag{2}$$

where A and B mean a state of + domain and – domain respectively. Reaction velocity $v$of this transition is described as follows,

$$v = -\frac{d[A]}{dt} = k[A] \tag{3}$$

where $[A]$ means area density of + domain and k is reaction rate constant. Integration of equation (3) from $t=0$ to $t=t_1$ is shown as follows,

$$-\log\frac{[A_1]}{[A_0]} = kt_1 \tag{4}$$

where $[A_0]$ and $[A_1]$ mean area density of + domain at $t=0$ and $t=t_1$, respectively. Additionally, Arrhenius equation is shown,

$$k = \alpha \cdot \exp(-E_a / RT) \tag{5}$$

where E_a is activation energy, and α is frequency factor. After we applied the result of heat treatment test in 4 temperatures (300 °C, 280 °C, 250 °C and 220 °C) to the equation (4) and (5), we evaluated that the value of E_a of 0.76±0.025eV and of $2.55\times10^5 \pm 1.27\times10^5$ by using least square method.

Using these parameters, we got shrinking speed of α inverted dot radius as a function of temperature shown by full line in Fig.7. To confirm adequacy of obtained value of E_a and α, we conducted the same heat treatment test in 190 °C. The results shown by white circle shows good agreement with the predicted one shown by the full line in Fig.7. It means the function using E_a and isα appropriate to predict shrinking speed of inverted dot radius at lower temperature.

Calculated shrinking speed of inverted dot radius in 80 °C which is the maximum temperature at use condition in general memory devices is 6.74×10^{-5}nm/h and it means that it takes 16.9 years until inverted dot array with the radius of 50nm loses its radius down to 40nm. This retention characteristic is good enough for comparing with lifetime period 10 years of general memory devices because reading inverted dot array by SNDM is absolutely able even if dot radius of 50nm gets 40nm.

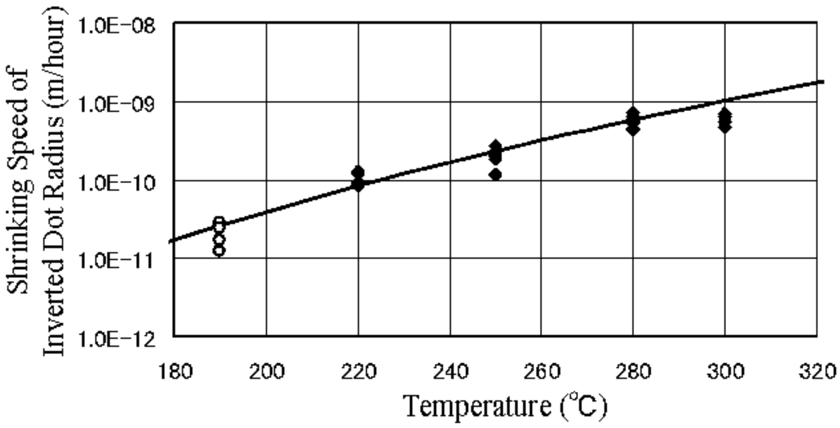

Fig. 7. Shrinking speed of inverted dot radius as a function of temperature. Black circles : The results of heat treatment test in 300 °C, 280 °C, 250 °C and 220 °C. Full line : Shrinking speed of inverted dot radius as a function of temperature using two parameters.White circles : The results of heat treatment test in 190 °C.

5. Actual information storage with low bit error and high memory density

Real information was actually stored. Although we have reported that ferroelectric data storage at a density of 1 Tbit/inch^2 was in principle possible,[1] this does not necessarily mean that actual information storage, requiring an abundance of bits to be packed together at high density, is easy to achieve. To facilitate actual storage, a large medium of sufficient surface quality and homogeneity is needed. Therefore, demonstration of actual data storage at 1 Tbit/inch^2 using ferroelectric materials is important to show whether the technology is really achievable.

At first we considered the usage of diamond-coated cantilevers with much better durability for the storage of actual information data composed of numerous bits. Probes with more sharp tips were required for increasing recording density while keeping BER low. Fine domain structures were obtained to be written successfully using metal-coated cantilevers as read/write probes. The typical tip radius of a metal-coated cantilever was approximately 25 nm, whereas it was 50 nm for the diamond-coated cantilever used in this study. Additionally, the thickness of the recording medium was reduced to 55 nm. Using the improved cantilever, the information data was recorded at 50nm bit spacing (areal density: 258Gbit/inch^2) as shown in Fig.8 .

The pulse amplitude was kept constant at -16 V, and the pulse duration was changed in the range of 5 to 50 μs. BERs were evaluated for each image. A pulse duration of 10 μs resulted in the lowest BER, with a measured BER less than 1×10^{-4}.

Thereafter, the recording density was increased, since the tip abrasion was inhibited by improving the circuit of contacting load control and reducing the spring constant of the cantilevers. 128×82 bit data written without dc offset voltage on a 40-nm-thick CLT plate.

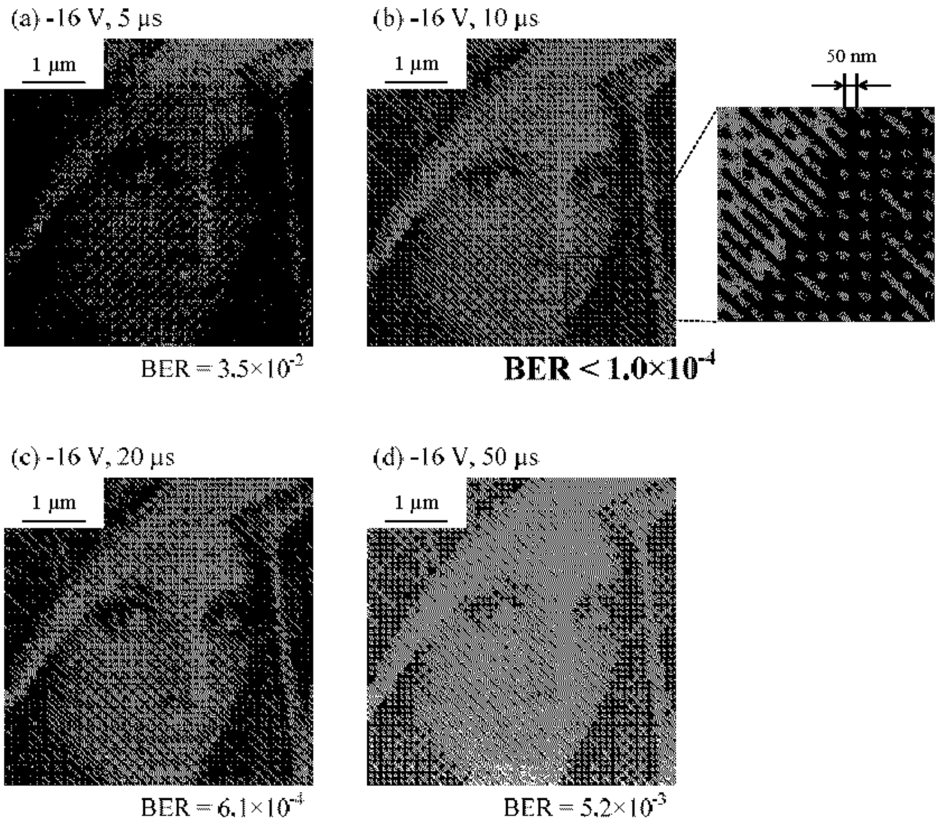

Fig.8 Actual information data recorded on 55-nm-thick $LiTaO_3$ recording medium with bit spacing of 50 nm (areal recording density: 258 Gbit/inch^2). The amplitudes of writing pulses were kept constant at -16V, and pulse widths were changed in the range from 5 μs to 50 μs. BER is indicated below each image.

Figure 9(a) shows the SNDM image of the information data written at the bit spacing of 25.6 nm (areal recording density: 0.98Tbit/inch^2). The writing conditions were as follows: the data bits of `0' were written by -14.1V, 100 ns pulses, whereas the positive voltage pulses were not applied at the positions of `1'. The written data was read out with high S/N ratio, in spite of increasing the recording density. The BER was evaluated to be 7.2×10^{-2} from this image. There were some inhomogeneities of the BER depending on the bit arrangements, similarly to the previous cases, thus the writing parameters were modified. Some different pulse shapes were used for the different bit arrangements, since this way was expected to be a direct way and more effective to reduce the BER than bipolar pulse application. Specifically, the negative pulses for writing the data bits of `0' were the same amplitude as in Fig.9(a) when the just prior bit was `0'and slightly larger when the just prior bit was `1', while the pulse width were set at 100 ns in the both cases. The BER of the information data written in this manner, which is shown in Fig.9(b), was 1.8×10^{-2}. A magnified image of the data bit array is shown in the same figure. The BER was lower by a factor of four compared with the case that all of data bits `0' were written under the fixed conditions. The number of such bit errors that `0' was miss-written as `1' was 124 bit out of 3889 bit, whereas the number of opposite-type errors was 24 bit out of 4251 bit. The bit errors of `0', which was more than five times larger than those of `1', were categorized in more detail according to the surrounding data bits. All of bit errors of `0'

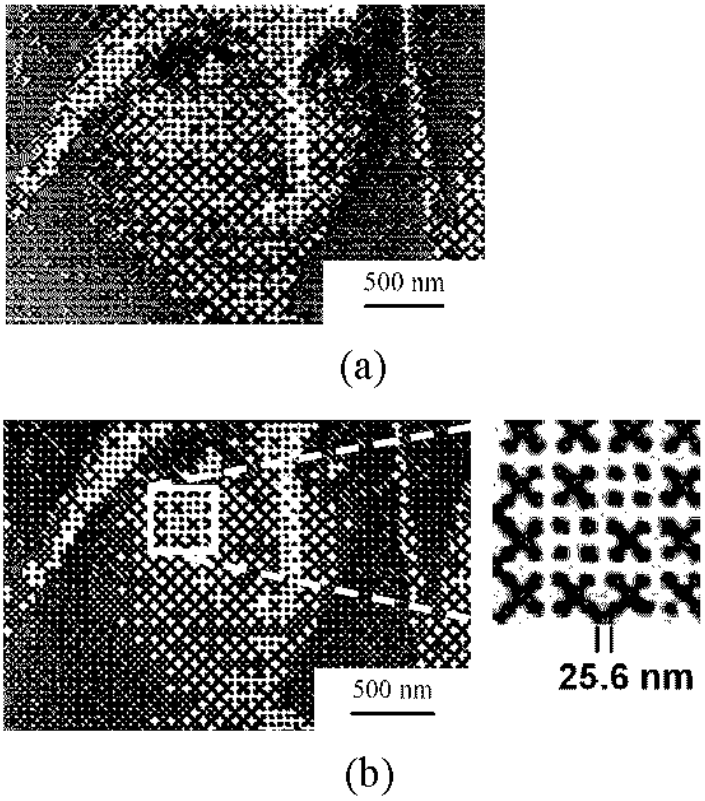

Fig.9 Actual information data recorded at the bit spacing of 25.6 nm (areal recording density: 0.98 Tbit/inch^2). 128×82 bit data written on a CLT single crystal formed by 100 ns pulse application without dc offset voltage on a 40-nm-thick CLT plate. (a) All of negative domains were written under the fixed condition. (The bit error rate was 7.2×10^{-2}.) (b) The duration times of negative voltage were changed according to the bit arrangements.(The bit error rate was 1.8×10^{-2}.)

arose only when three or more bits out of the four nearest bits were `1'. The BER was expected to be reduced by increasing the number of surrounding bits which were referred in the categorization and setting the appropriate pulse voltage for the each case, although it causes some complexities in deciding the pulse parameters such that the estimations by the simulations of domain expansion are required. Thus we succeeded in actual information storage at a density of 1 Tbit/inch^2 in a ferroelectric material.

6. Discussion and Conclusion

In order to obtain fundamental knowledge on high-density ferroelectric data storage, several experiments were conducted on nano-domain formation in CLT single crystals.

Firstly, we studied the relationship between the minimum pulse voltage and duration as a function of dc offset voltage applied to the CLT thin plate. We succeeded to form an smallest artificial nano-domain single dot of 5.1 nm in diameter and also succeeded to form artificial nano-domain dot-array with a memory density of 10.1 Tbit/inch^2 and a bit spacing of 8.0 nm, representing the highest memory density for rewritable data storage reported to date.

Next, we demonstrated nano-domain dot formation by application of a 10 V, 500 ps voltage. The 500 ps switching time is suitable for the development of high-speed ferroelectric data storage systems, potentially supporting writing rates of 2 Gbps per probe with memory densities at 1 Tbit/inch^2

Finally, actual information data were recorded on a CLT single-crystal medium and the method of improving recording density and BER was discussed. For improving recording density and bit error rate simultaneously, the tip of the diamond-coated cantilever was sharpened by the ion milling process, and the thickness of the recording medium was reduced to 55 nm. As a result, a BER of less than 1×10^{-4} was achieved at an areal density of 258 Gbit/inch^2. Moreover a data bit array of 128×82 was successfully written at an areal data storage density of 1 Tbit/inch^2 with a bit error rate of 1.8×10^{-2}. These results confirm the potential of ferroelectric materials in storing information at high densities.

Unfortunately, as long as we use a piezoelectric linear scanner to drive a medium, even in the SNDM technique, the slow data transfer rate of 12 kbps ~ 50 kbps per one probe for reading/writing a succession of bits has been reported due to the slow scanning speed of linear piezoelectric scanner [5] and the narrow bandwidth of SNDM detector. In the some kinds of probe storage system just like millipede developed by IBM, [6] it is essential to employ a multi probe array system to improve the read/write speed. Of course, this multi-probe method might be one possibility to realize SNDM ferroelectric probe memory.

However, as we have confirmed the possibility that the quite high speed data transfer is possible at least for writing with a single probe head in the ferroelectric probe memory, to make the best use of this high speed switching characteristics of ferroelectrics, we will have to investigate the hard disk drive (HDD) type ferroelectric probe memory just like magnetic HDD with a few number of probe heads. Therefore, now, we are developing a new HDD type ferroelectric data storage system with a high speed rotating disk medium and a newly developed wide-band SNDM FM demodulator. The results will be reported in the near future.

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