Design and Implementation of the GHz-Band Wide(2~18 GHz) Linear Equalizer

Sungtek Kahng[1] · Jeongho Ju[1] · Wongyu Moon[2]

Abstract

This paper presents a linear amplitude equalizer developed to secure the linearity of the slope of the amplitude over the frequency band ranging 2~18 GHz. The circuit model is featured by the resistor placed between each pair of a transmission-line and a stub. The design includes finding the values of resistors and stubs to have the optimal linear slope and return loss performances. The measured data show the acceptable performances of the slope variation and return loss over 2~18 GHz.

Key words : Amplitude Linearity, Wide-Band Linear Equalizer, Microstrip Line.

Ⅰ. Introduction

The Radar Warning Receiver(RWR) for a helicopter tends to end up with the increase of overall insertion loss that is attributed to the cascaded placement of dissipative components such as switch, filter, power-divider, coupler and the like in the wide-banded RF channel. In order to reach for the targeted performance, it is necessary to compensate for the insertion loss by flattening in the gain amplitude over the frequency band of interest. This is what is all about the gain(amplitude) equalization techniques which quite often entails the slope linearization.

To date, even though the domestic technical groups have presented that they are mature in implementing the gain equalization for commercial products operating in the relatively narrow frequency bands, they do not seem to meet the challenge of the equalization in broader bands for military applications.

As an attempt to meet the rising demands and boost the competitiveness of our technology, we have developed the linear gain equalizer working in the band as wide as over 10 GHz for the RWRs.

With a look into the current techniques of the gain equalization, it is found they can be classified to the followings : Linear and non-linear gain equalization methodologies[1]~[4]. The non-linear scheme is exploited to the narrow-banded sub-bands of one given broad-band, This is relatively easy to build up in the design, but it requires multitude of different stages corresponding to the sub-bands, which leads to cumbersome extra insertion losses, when the stages are electrically combined for its physical implementation. On the contrary, the linear equalizer necessitates one module, though its design seems tougher than the non-linear case. Besides, the linear equalization is advantageous in that it aims at the operation in one broad-band.

Making a noteworthy progress from what has been done previously as in [1]~[4], we present the linear gain equalizer working over 2~18 GHz by transmission lines with coupling elements.

Ⅱ. Theoretical Work

The gain equalizer plays a role of flattening the amplitude of the resultant insertion loss of the equalizer following the former component over the specified band[1]~[4].

As shown in the result, the balance marked number 3 is made by the ascending amplitude(marked number 1) added to the descending one(number 2). Particularly

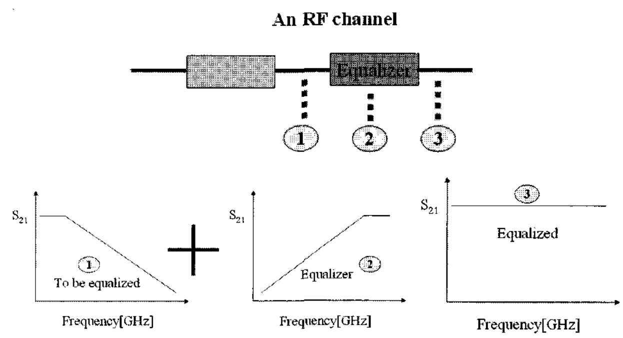

Fig. 1. Role of the linear gain equalizer.

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with Fig. 1, the equalizer shows the minimum loss at the high end of the band[5]. Depending on cases, the slope of the equalizer's amplitude should be negative with the maximum loss at the upper end of the band. As a matter of course, the minimum loss of the equalizer is designed the lowest possible.

To begin, a low-ordered bandpass filter(BPF) is considered. In detail, the center frequency of the BPF is set at the end of the band(18 GHz or 20 GHz here), which is called the cut-off frequency in the gain equalizer design, with the ripple level of 0.1 dB and the fractional bandwidth of 1. That is to say the Chebyshev filter of 1st order. Using this, it is effective to get the idea of how we get started, but falls short of satisfactory levels on return loss and linear slope. So it is inevitable to expand to a higher order circuit.

Regarding the fundamentals of the operation, the transmission line with the serial resistor is let go open at the cut-off frequency that is equivalent to the resonance frequency of series inductor and capacitor. At this point, the insertion loss becomes ideally zero. The rest of the band is designed to undergo the attenuation due to the T-network of three resistors, which determines the slope.

The design flow can be simply described as follows (Fig. 3).

In the first place, we set the cut-off frequency of the gain equalizer at the center frequency of the nominal filter. Simultaneously, the attenuation band is defined. In the second place, the order of the filter is decided to have the slope of the amplitude as close as possible to the wanted value. And then, varying the resistors, the slope is adjusted to meet the spec. over the entire frequency band. If it is not satisfactory, return to the step where the order of the filter is determined and change to the immediate higher order.

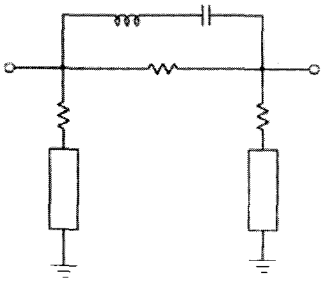


Fig. 2. Basic circuit of the linear equalizer.

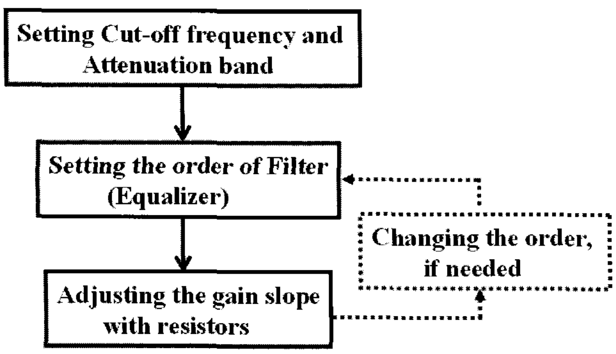


Fig. 3. Steps for the design of the linear equalizer.

Ⅲ. Design and Implementation

Here comes the summary of the design specifications (Table 1).

Among the items, the slope is set the top priority. Maintaining the slope, the return and insertion losses are considered.

Firstly, let us start the design by changing the order of the basic circuit from 1 to 2.

The reactive elements are found by having their resonance at the cut-off frequency given in the specs. The resistors are computed, assumed that the T-networks are symmetric, to secure the gradient of the amplitude curve parallel to the given slope. Increasing the order of the equalizer, the slope performance has improved from Fig. 4(b) to Fig. 4(d).

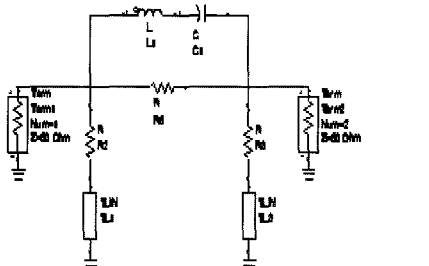
Taking into account the fabrication based upon the microstrip line, the reactive elements are replaced by the lossy transmission line(better for considering dispersion). The order of the entire circuit should be increased.

In order to compute the design parameters such as the lengths of the transmission lines for the cut-off frequency and the resistors for the gain slope meeting the specifications, an iterative scheme results in the values of the components as in the following Table 2.

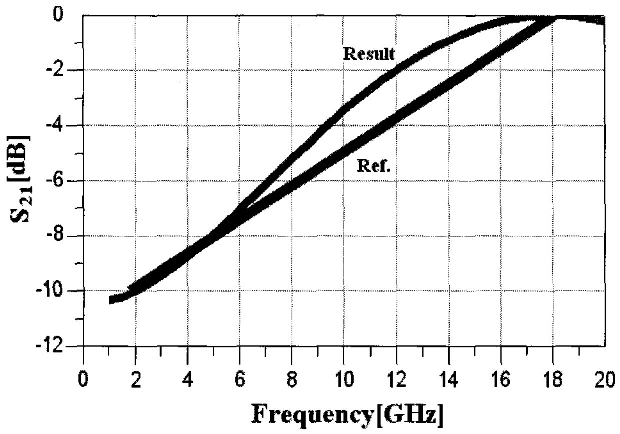
It is assumed that the 15th ordered circuit takes the symmetry with regard to the 8th shunt element, for convenience. Resistors are 800, 700, 300, 180, 150, 20, 170, 150 Ω in order from the first shunt element through the 8th shunt element, And the characteristic impedance values of the first(14th), and second(13th) series lines are 35 Ω and 31 Ω, respectively. The rest of the series lines have 30 Ω. Besides, Zc of the first and last shunt lines is 60 Ω. 120 Ω is given to the other shunt lines. Here the capacitance is negligible.

Table 1. Specifications.

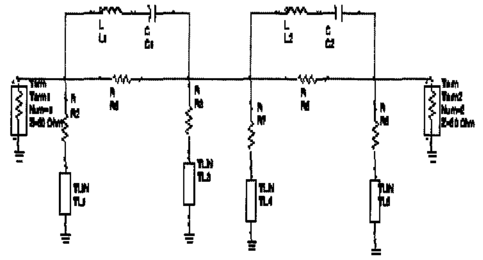
Item	Specs
Band	2~18 GHz
Slope	10 dB over the BW
Insertion loss	< 3 dB at 18 GHz
VSWR	< 2.0:1



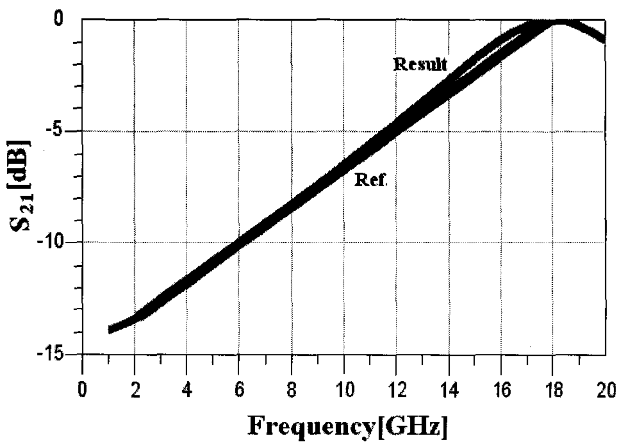
(a) Circuit of the 1st order linear equalizer(before improvement)



(b) Performance of the 1st order linear equalizer(before improvement)



(c) Circuit of the 2nd order linear equalizer(an improvement)



(d) Performance of the 2nd order linear equalizer(an improvement)

Fig. 4. Experiment on the improvement of the performance.

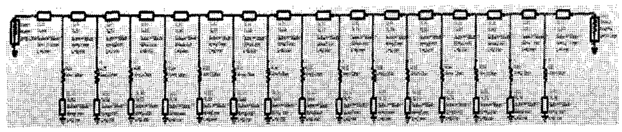
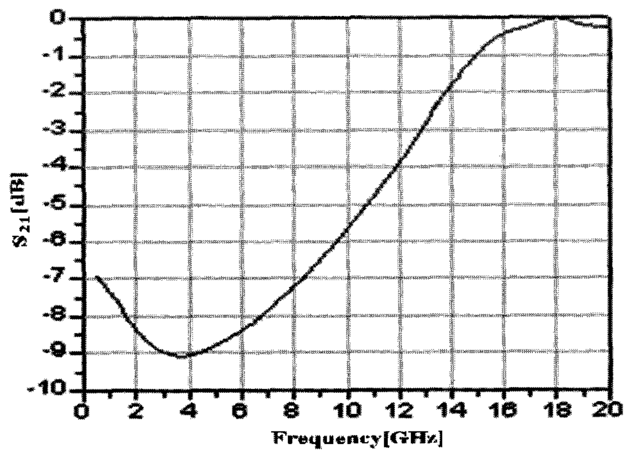


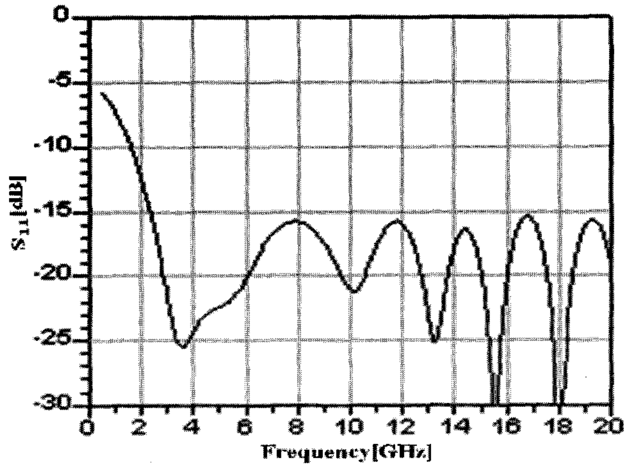
Fig. 5. Increased order of the linear equalizer.

Table 2. Design parameters in use.

Item	Value
Series line	8.25 mm with Z_c=30～35 Ω
Shunt line	4.13 mm with Z_c=60～120 Ω
Relative dielectric constant	9.6
Line width	9.9 mil
Substrate height	0.25 mm
Resistors	20～800 Ω



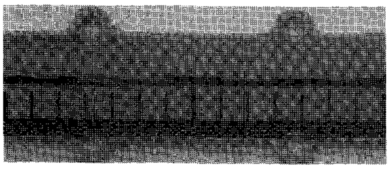
(a) Insertion loss of the linear equalizer



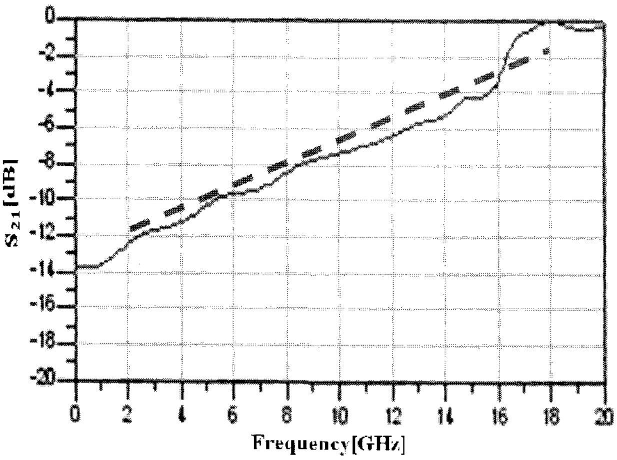
(b) Return loss of the linear equalizer

Fig. 6. Simulated insertion and return loss performances of the linear equalizer.

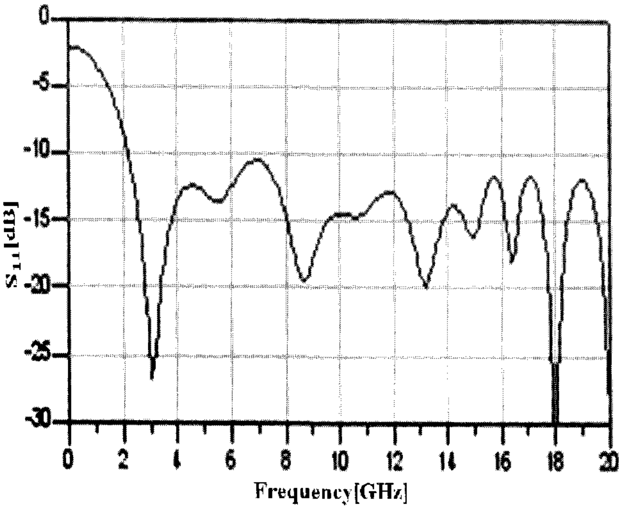
Using the circuit components above, the following



(a) Picture of the manufactured linear gain equalizer



(b) Insertion loss of the linear equalizer



(c) Return loss of the linear equalizer

Fig. 7. Measured insertion and return loss performances of the linear equalizer.

results have been obtained as the insertion and return loss performances.

Concerning the results, the cut-off frequency and the average slope of the design are compliant to the specs. However, the slope's discrepancies occurring near the lower and upper ends of the band are presumed to result from the scheme that the design resonance frequencies of all the units are set at one cut-off frequency. This can be improved by assigning the units to slightly different frequencies. The performance of the designed return loss is good enough, less than －15 dB, which also shows compliance to the specified value. Next, the design has been reflected on the fabrication with the microstrip line and the substrate of relative dielectric constant 2.2, we conducted the measurements of the equalizer.

Going through the tuning and trimming on the fabricated equalizer, the measured return and insertion losses amount to less than －10 dB and roughly 9 dB throughout the band(2～18 GHz), respectively. Actually, the slightly non-linear behavior happens in the vicinity of 18 GHz and it is believed to stem from the design ignorant of the capacitance parasitic to the resistors and transmission lines.

Ⅳ. Conclusion

In this paper, the design of a gain equalizer has been conceptualized to achieve the linear slope over the very wide band 2～18 GHz and good return loss performance. Besides, it has been implemented by fabrication with the microstrip transmission lines and SMT resistors. The measured data prove the realized equalizer outputs the acceptable linearity in the slope and return and insertion losses.

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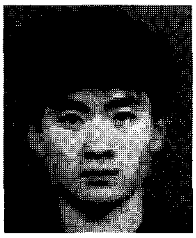

was with Hanyang University in Seoul, Korea and there he earned the Ph.D. degree in Electronics and Communication Engineering in 2000, with the specialty in radio science and engineering. From year 2000 to early 2004, he worked for the Electronics and Telecommunication Research Institute, where he worked as a senior research staff on numerical electromagnetic characterization of and developed the RF passive components for satellites. Since March 2004, he has joined the department of Information and Telecommunication Engineering at University of Incheon that he has continued studying analysis and advanced design methods of microwave components and antennas. Along with the above, he is accredited to be in the Science & Engineering of Marquis Who's Who in the World and holds several patents concerning EMC solutions and microwave components as well.

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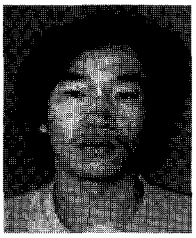

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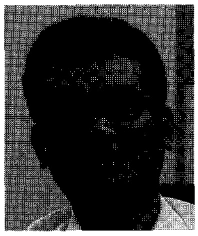

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