칩 및 코아간 연결선의 지연 고장 테스트
(Delay Fault Test for Interconnection on Boards and SoCs)

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요 약 본 논문은, IEEE 1149.1 및 IEEE P1500 기반의 보드 및 SoC의 연결선 지연 고장 테스트를 위한 회로 및 테스트 방법을 제안한다. IDFT 모드 시, 출력 셀의 Update와 입력 셀의 Capture가 한 시스템 클럭 간격 내에 이루어지도록 하는 시스템 클럭 상승 모서리 발생기를 구현한다. 이 회로를 이용함으로써, 단일 시스템 클럭 뿐만 아니라 다중 시스템 클럭을 사용하는 보드 및 SoC의 여러 연결선의 지연 고장 테스트를 쉽게 할 수 있다. 기존의 방식에 비해 면적 오버헤드가 적고 경계 셀 및 TAP의 수정이 필요 없으며, 테스트 절차도 간단하다는 장점을 가진다.
키워드 : 연결선 지연 고장, 시스템 온 칩, IEEE 1149.1, IEEE 1500, 다중 클럭

Abstract This paper proposes an interconnect delay fault test (IDFT) solution on boards and SoCs based on IEEE 1149.1 and IEEE P1500. A new IDFT system clock rising edge generator which forces output boundary scan cells to update test data at the rising edge of system clock and input boundary scan cells to capture the test data at the next rising edge of the system clock is introduced. Using this proposed circuit, IDFT for interconnects synchronized to different system clocks in frequency can be achieved efficiently. Moreover, the proposed IDFT technique does not require any modification of the boundary scan cells or the standard TAP controller and simplifies the test procedure and reduces the area overhead.
Key words : Interconnect Delay Fault, SoC, IEEE 1149.1, IEEE 1500, Multiple Clocks

1. 서 론

As the integration density of boards and System on Chips (SoCs) and the speed of system clocks become increasingly high and fast, it is crucial to test delay as well as conventional static faults on interconnect wires. Boundary scan design is a design for testability technique to simplify the application of test patterns for the detection and diagnosis of different faults at levels of packages (e.g. chips, modules, boards and backplanes). Both IEEE 1149.1 standard for board and IEEE 1500 for embedded core testing have become increasingly prevalent as industrial standards [1,2]. Inherently IEEE 1149.1 has a deficiency in testing delay defects on interconnect wires due to the 2.5 test clock interval required from launching to capturing the test patterns. Boundary scan was used to test delay defects on I/O pads at wafer or package levels [3], however at-speed testing by multiple system clocks was not properly addressed. Early Capture latch is added to each input boundary scan cell (BSC) to sample the test responses [4], and an Early Capture Control Register (ECCR) composed of flip-flops and inverters is additionally required to test interconnect operated by different system clocks [5]. Similar to the ECCR, programmable delay logic was introduced to capture the responses early and to update the stimuli later [6]. To adopt the above techniques of [4-6], extra hardware for each boundary scan cell is required. Without modifying the BSC, late update and system clock multiplexing technique was proposed, but multiple system clocks and IEEE 1500 wrappers were not

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addressed [7]. Multi-frequency core wrappers were presented in [8], which does not handle interconnects among cores but describes at-speed testing using the core's internal scan chains.

This paper presents IDFT solutions on boards and SoCs operating with multiple system clocks. The problem of testing interconnect delay faults with IEEE 1149.1 is introduced in section 2, and section 3 describes IDFT circuits and test procedure with IEEE 1149.1. In Section 4 the IDFT for an SoC with IEEE 1500 wrappers is presented. Comparative analysis from design experiments shows the superiority of our approach in Section 5 followed by the conclusion in Section 6.

2. IEEE Boundary Scan and Interconnect Testing

IEEE boundary scan architecture consists of Test Access Ports (TAP), TAP controller, and instruction and data registers. Test Data Input (TDI), Test Data Output (TDO), Test Clock (TCK), and Test Reset (TRST) constitute the TAP and TRST can be used optionally. All of the input and output pins of a chip are connected to input and output boundary scan cells, respectively. IEEE boundary scan instructions can be classified into compulsory ones such as BYPASS, EXTEST, and SAMPLE/PRELOAD and optional ones such as CLAMP, HIGHZ, and RUNBIST. The TAP controller is a finite state machine with 16 states, which mainly enable the application of patterns to data and instruction registers as well as the observation of test responses. The interconnect faults on a board can be summarized as follows:

1. S-at-1 and S-at-0: The conventional stuck at fault model.
2. S-open: The fault model for CMOS implementations which models any open net fault as either a pull-up or pull-down circuit. Initialization and transition patterns, that is, a two pattern test is required to detect a stuck-open fault.
3. Shorted Nets Faults: AND, OR, OPEN, DOMINATOR: The fault model for shorted nets faults can be classified into AND, OR, OPEN and DOMINATOR type faults. Suppose two nets: (A, B) are shorted and let the logic values at each net be V(A) and V(B) respectively then:
   A. An AND type short results in logic 0 if either net is logic 0.
   B. Conversely an OR type short results in logic 1 if either net is logic 1.
   C. We say A DOMINATES B if V(A) appears at both nets regardless of V(B). Similarly B DOMINATES A if V(B) always appears at both nets regardless of V(A).
4. Delay fault: '0_ 1' or '1_ 0' transition can not reach the receiver within a specified amount of time.

This paper introduces a new technique which makes it possible to test delay defects in addition to the static interconnect faults with the EXTEST instruction. The method to apply and observe interconnect test patterns and state transitions of the Test Mode Selector can be summarized as follows:

1. EXTEST instruction is read and decoded. The state transition is: RESET_ IDLE_ Scan-DR_ Scan-IR_ Capture-IR_ Shift-IR_ …_ EXIT1-IR_ Update-IR_
2. Interconnect test patterns are serially applied through the boundary scan register. The corresponding state transitions are: Scan-DR_ Capture-DR_ Shift-DR_…_ EXIT1- DR_
3. Test patterns read are applied to the Update latch and the signals are propagated to input Boundary Scan Cells (BSC) in parallel. The corresponding state transitions are: Update-DR_ Scan-DR_ Capture-DR_
4. Test responses captured are shifted out through BSCs to TDO. The corresponding state transitions: Capture-DR_ Shift-DR_…_ EXIT1-DR _

Update-DR and Update-IR states are active on the falling edge of the TCK while all the others are active on the rising edge. The timing diagram of the above step 3) can be drawn as in Fig. 1. Update-DR is active on the dotted line, and Capture-DR is active on the bold line, thus 2.5 TCKs are required from Update-DR to Capture-DR. That is, it takes 2.5 TCKs from the application of interconnect test patterns through output BSCs to the observation of test responses to input BSCs.

Although the number of TCK cycles has no relevance to the detection of static interconnect faults, the test responses must be observed in a system clock cycle to detect delay defects. Since the delay defects can not be tested with IEEE boundary scan design, either the state diagram of the TAP controller or boundary scan cells must be changed to capture the responses, especially if multiple system clocks are involved, within associated system clock intervals. A highly efficient test control technique for capturing interconnect delay defects operated by multiple system clocks will be described in the following section.

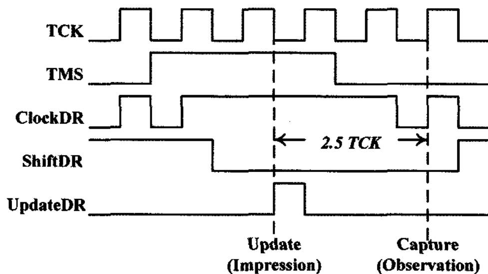

Figure 1 Problem in testing interconnect delay with IEEE 1149.1 boundary scan

3. IDFT in Boards with IEEE 1149.1

The key feature of our IDFT is to design an edge generator corresponding to each system clock. To describe the basic concept of our IDFT, one board with two chips (Chip 1 and Chip 2) operating with the same system clock is introduced in Fig. 2. *The IDFT Edge Generator transforms the signals from a standard TAP controller to late update UpDR and early capture CapDR with the Delay_EXTEST instruction.* The output BSCs launch test stimuli at the rising edge of UpDR and the input BSCs capture the test responses exactly one system clock later by the CapDR signal. Most boards use several different system clocks with varied frequencies to optimize the overall system performance [5]. To test delay defects on inter-connects operated by different system clocks, it must be ensured that the associated test data are updated and captured only once according to the corresponding system clocks. We adopt the stretched Update-DR state [4] to capture the responses early, but instead of changing each BSC, for each system clock simple edge generator is attached to the TAP controller to provide modified Update and Capture control signals to the BSCs.

An IDFT Edge Generator described as a synchronous finite state machine in Fig. 3 has to perform Update and Capture operations during the Update-DR state and perform a Shift operation during the Shift-DR state. Fig. 4 shows the detailed architecture of the IDFT Edge Generator and all the signals are precisely described in Table 1. In normal mode, the M1 and M2 choose UpdateDR and ClockDR by the IDFT_Mode value of 0. In Delay_EXTEST mode, the stretched IDFT_UpDR and IDFT_CapDR generated by the system clock, IDFT_Mode, and UpdateDR signals are chosen by the multiplexors. It is noted that the

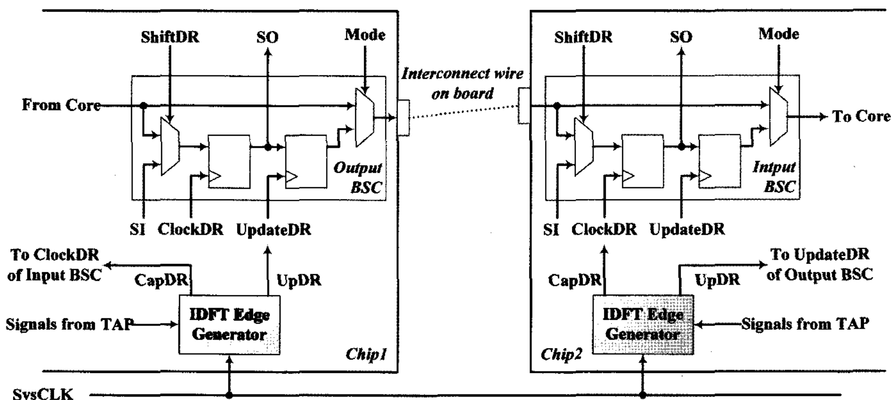

Figure 2 IDFT Using System Clock Edge Generator

key flip-flops are not active during normal mode by degating the SysCLK.

The operation procedure of our IDFT controller can be described as follows.

Step 1. Shift in Delay_EXTEST instruction and IDFT_Mode control signal is set to 1 after decoding.

Step 2: Shift in test stimuli.

Step 3: Update-DR state is stretched to generate IDFT_UpDR and IDFT_CapDR from the UpdateDR, IDFT_Mode, and SysCLK.

Step 4: Shift out test responses.

By applying the above procedures, the timing diagram of Fig. 5 is obtained. TCK, TMS, UpdateDR, ClockDR and ShiftDR are the standard signals from the IEEE 1149.1 TAP controller. During the Update-DR state prolonged by TCK and TMS, UpDR and CapDR are transited from 0 to 1 only once in a SysCLK interval. When the Update-DR state is over, UpDR and CapDR are transited from 1 to 0 at the rising edge of the system clock, and CapDR resumes the test signal of ClockDR during the Shift-DR state.

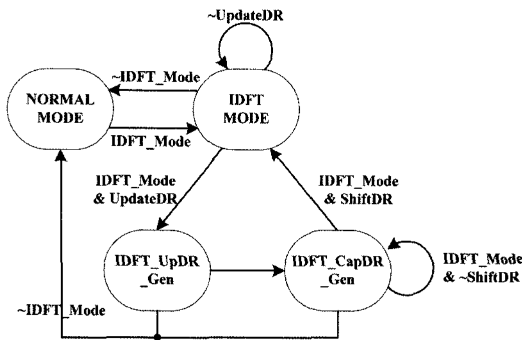

Figure 3 IDFT Edge Generator State Diagram

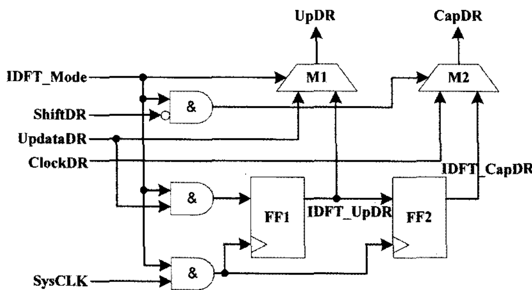

Figure 4 IDFT Edge Generator

Table 1 Signal Description of IDFT Edge Generator

Signal Name	Description
SysCLK	System Clock
IDFT_Mode	0 = Normal mode, 1 = IDFT mode.
UpdateDR	UpdateDR from TAP controller
ClockDR	ClockDR from TAP controller
IDFT_UpDR	Internal signal to generate a rising edge from the FF1 synchronized at system clock when IDFT_Mode = 1. This signal forces UpDR to transit from 0 to 1 and output BSCs update test stimuli.
IDFT_CapDR	Internal signal to generate a rising edge from the FF2 synchronized at system clock when IDFT_Mode = 1. This signal forces CapDR to transit from 0 to 1 and input BSCs to capture test responses.
UpDR	Output of M1. If IDFT_Mode = 1, UpDR <= IDFT_UpDR. Otherwise, UpDR <= UpdateDR.
CapDR	Output of M2. If IDFT_Mode = 1 and UpdateDR = 1, CapDR <= IDFT_CapDR. Otherwise, CapDR <= ClockDR.

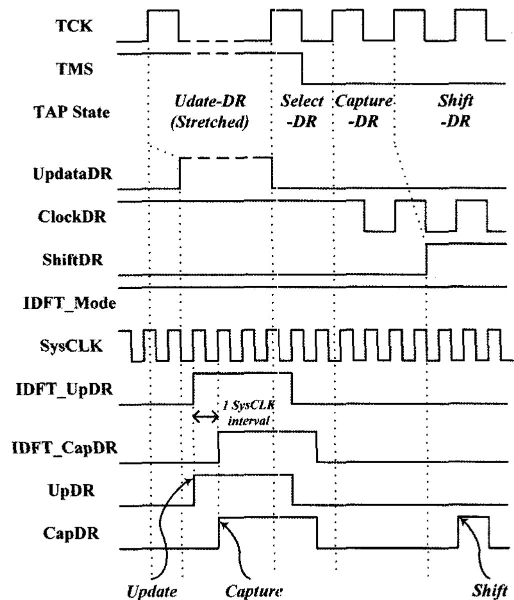

Figure 5 Timing Diagram of IDFT Edge Generator

To test delay defects on interconnects operated by multiple system clocks, only this simple IDFT edge generator is needed for each system clock. The UpDR and CapDR signals from each IDFT edge generator are connected to the set of output

and input BSCs operated by the corresponding system clock. Fig. 6 shows a timing diagram example for IDFT with multiple system clocks. Signals UpDR1 and CapDR1 are the outputs of one IDFT Edge Generator operated by SysCLK1, and the signals UpDR2 and CapDR2 are the outputs of the other IDFT Edge Generator operated by SysCLK2. During the stretched Update-DR, the UpDR1 and CapDR1 are transited from 0 to 1 only once in a SysCLK1 interval, and UpDR2 and CapDR2 are also transited from 0 to 1 once in a SysCLK2 interval. When the Update-DR state is over, signals UpDR1 and UpDR2 are transited from 1 to 0 at the rising edge of each system clock, and CapDR1 and CapDR2 resume the test signal of ClockDR during the Shift-DR state.

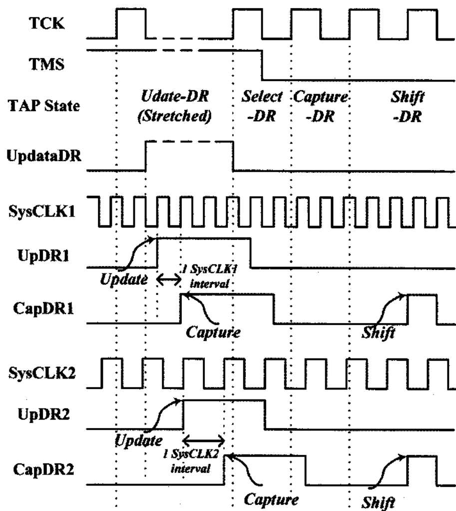

Figure 6 IDFT Timing Diagram with Multiple System Clocks

4. IDFT in SoCs with IEEE 1500

4.1 IEEE 1149.1 to IEEE 1500 Interface

The IEEE 1500 is the standard for testing embedded cores while preserving scalability for hierarchical test access. IEEE 1500 provides a flexible hardware interface between an embedded core and its environment so that the predefined test patterns can be efficiently delivered to and from the embedded core. The core test wrapper standardized by IEEE 1500 has the following features [2].

- Provides the core test, interconnect test and bypass mode which are subset of IEEE 1149.1 modes.
- May connect the core boundary chain (wrapper) to any internal scan chain to perform internal testing of the cores.
- The various modes of the core test wrapper are operated by several control signals in general generated through an SoC TAP controller.

The IEEE 1500 architecture consists of the IEEE 1500 wrapper register, TAM connection, instruction register, and control signals provided externally. The wrapper boundary cell (WBC), wrapper serial input (WSI), wrapper serial output (WSO), and wrapper serial control (WSC) are shown in Fig. 7.

In general, control signals to access the WSP are provided by an existing IEEE 1149.1 TAP controller with an interface glue logic as shown in Fig. 8, where some mechanisms are required to select cores or chip, and to set up, release, and change serial scan paths [2,9-12]. WRCK is directly connected to TCK and, SelectWIR, whose value of '1' indicates the selection of WIR and '0' the selection of WBR, is connected to the Select signal of the TAP controller. From the wrapper serial control (WSC) signals, the control signals for each wrapper boundary cell (WBC) are generated by the simple logic of Fig. 9. When WBCs are selected (SelectWIR = 0), this logic enables each WBC to perform

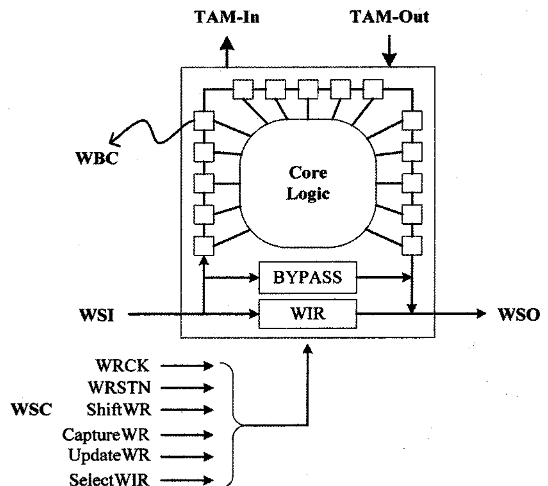

Figure 7 IEEE 1500 Wrapper & WSP (Wrapper Serial Port)

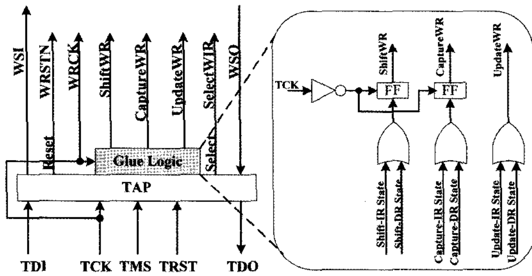

Figure 8 TAP to WSP interface logic

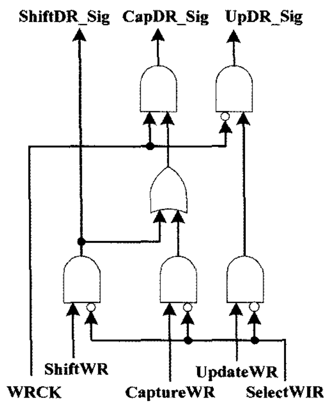

Figure 9 A Simple WSC to WBC logic

the update, shift and capture by passing ShiftWR to ShiftDR_Sig and WRCK to CapDR_Sig and UpDR_Sig, respectively [2,13].

4.2 IDFT among IEEE 1500 Wrapped Cores

IEEE 1500 defines various types of WBCs including a standard cell shown in Fig. 1, a single flip-flop type without update storage, multiple flip-flops with a number of shift-path storages, and so on [2]. Only when an IEEE 1500 wrapped core includes the WBCs with update storages, can the delay defects on interconnects among IEEE 1500 wrapped cores be easily tested by implementing our IDFT edge generator and applying the test procedures described in Section 3. Fig. 10 shows the detailed connections of the IDFT edge generator to an IEEE 1500 wrapped core, and the timing diagram of TAP to WSP interface logic, WSC to WBC logic and IDFT edge generator is precisely described in Fig. 11. If multiple system clocks are involved, the IDFT edge generator for each system clock is needed. In summary, interconnects on any SoC with 1149.1 and IEEE 1500 cores operated by

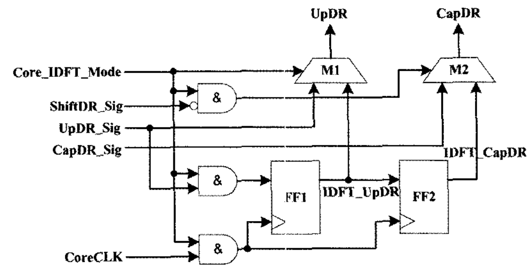

Figure 10 IDFT Edge Generator for IEEE 1500 core

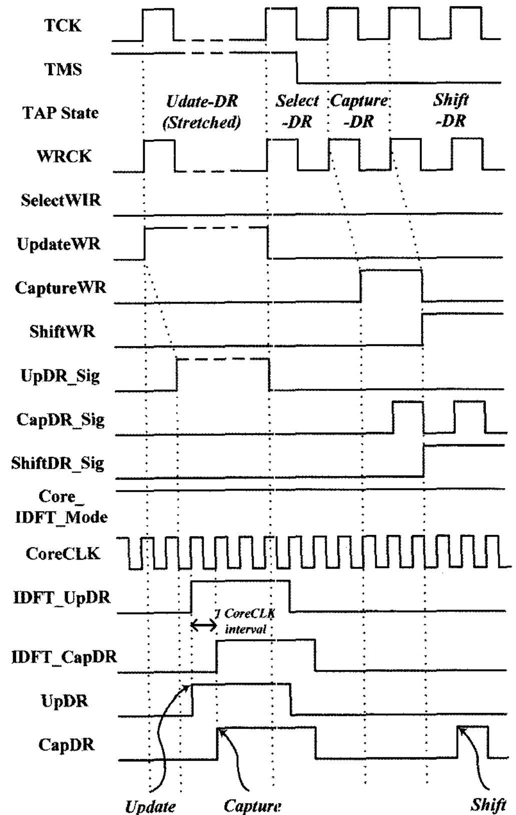

Figure 11 Timing Diagram of IDFT Edge Generator

multiple system clocks can be effectively tested with our technique.

5. Design Experiment and Comparative Analysis

An SoC with IEEE 1500 wrapped cores was designed to verify the operation of IDFT. The block diagram is shown in Fig. 12. Three IEEE 1500 wrapped cores are controlled by an SoC TAP, and two system clocks, CLK1 and CLK2 are

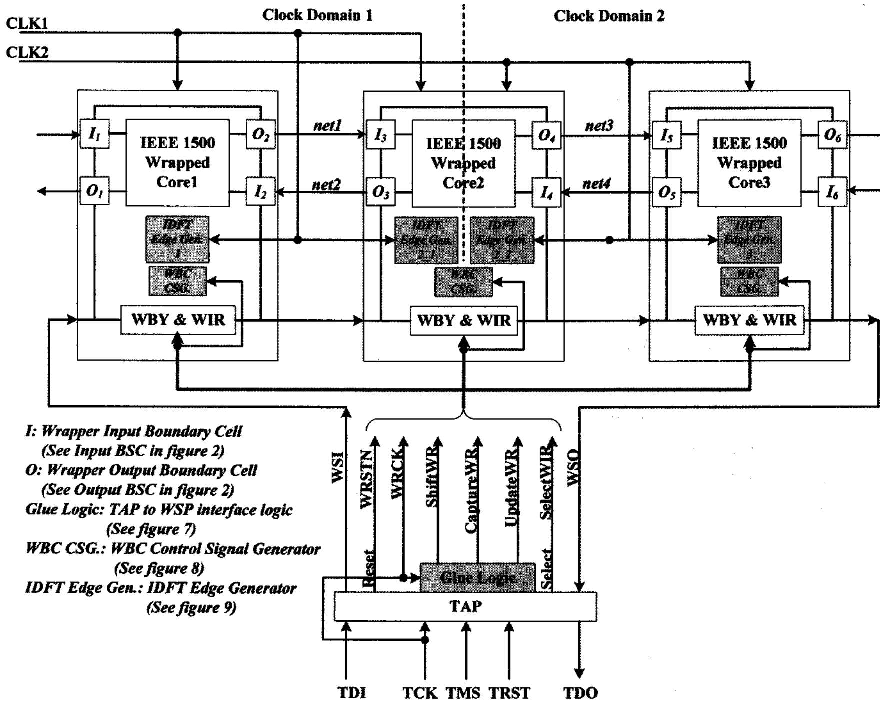

Figure 12 Example of an SoC with multiple clock domains

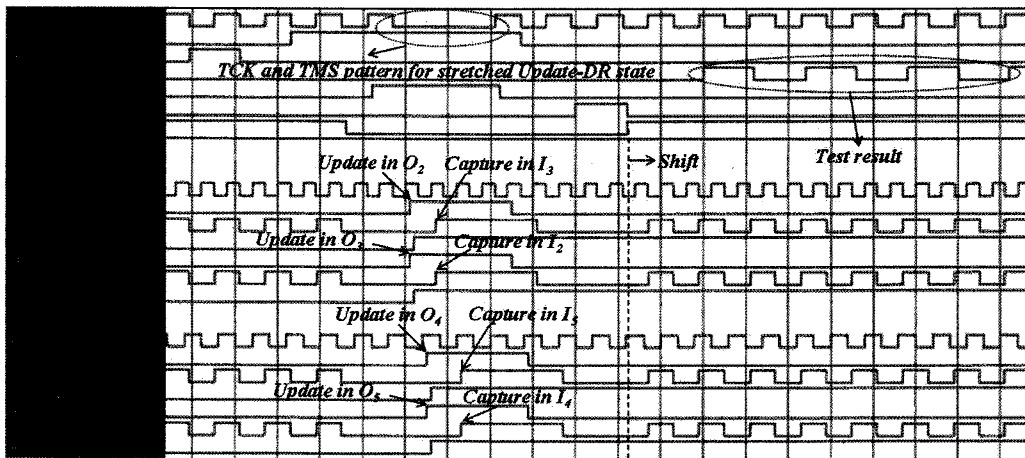

Figure 13 IDFT simulation results between IEEE 1500 wrapped cores

adopted, where the CLK1 interfaces between Core1 and Core2, and CLK2 between Core3 and Core1. Both Core1 and Core3 have one IDFT edge Generator each. Since Core2 includes two separate parts, one operating at CLK1 and another at CLK2, two IDFT Edge Generators are needed. A benchmark SoC is described as Verilog-HDL and synthesized through Synopsys with Samsung 0.18 Omtechnology library, and the clocks for TCK, CLK1 and CLK2 are adopted as 100 MHz, 200 MHz and 125 MHz, respectively. In Fig. 13, the simulation result shows that the patterns for net1, net 2, net3, and net4 among different cores are successfully captured within one system clock cycle.

Compared with previous research, our IDFT

controller fully complies with IEEE standards, and supports an SoC with IEEE 1149.1 and IEEE 1500 wrapped cores. Normal operation is not affected by our technique and no additional power is required by activating the IDFT edge generator only during the update stage of Delay_EXTEST. Table 2, where the IDFTC shows our IDFT controller, precisely compares various aspects with other techniques, and it is noted that our technique generally outperforms other techniques.

Minimizing area overhead on the chip is completed by simply providing update and capture signals through the IDFT edge generator. The number of boundary scan cells, additional gates with other techniques which change boundary scan cells, and the gate count of our IDFT edge generator are compared in Table 3. Drastic area reduction is shown to be achievable with our technique.

Table 2 Comparisons with Existing Techniques

	BSC Modifica-tion	TAP Modifica-tion	Effect on Normal Mode	Support Multiple Clocks	Support IEEE 1500	Low Power
[4]	O	X	O	X	X	X
[5]	O	X	O	O	O	X
[6]	X	O	X	X	O	X
[7]	X	X	X	X	O	X
IDFTC	X	X	X	O	O	O

Table 3 Comparisons of Gate Counts by BSC Modification

	Xeon Processor (INTEL)	TMS320 DM642 (TI)	TMS320 C6713 (TI)	Pentium Ⅲ 0672 (INTEL)
BSC #	304	363	363	457
BSC changed	1824	2178	2178	2742
IDFTC	96	72	72	96

6. Conclusions

An efficient interconnect delay fault test (IDFT) controller is introduced for boards or SoCs operated by multiple system clocks. The simple IDFT controller enables the test stimuli launched to be captured by input cells within one system clock cycle, and for multiple system clocks only the simple IDFT controller is needed for each system clock. Compared with other techniques, our IDFT controller fully complies with IEEE 1149.1 and IEEE 1500 standards, and system speed and power are not affected.

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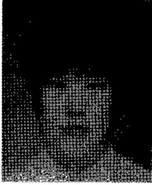

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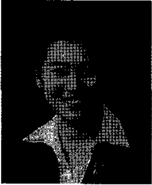

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