Fast Charging Photoflash Capacitor Charger with Wide Range Current Limiter

Won Ho Choi, Woo Kwan Lee, Soo-Won Kim

Abstract

The fast charging photoflash capacitor charger with wide range current limiter is presented. By using proposed control logic block and wide range current limiter, the photoflash capacitor charger can reduce charging time and control life of battery for user convenience. The proposed photoflash capacitor charger has 3s charging time at 3.3V battery voltage, 1.2A current limit condition. It is well-suited for portable device application like digital camera, digital video camera, and mobile phone with camera.

Key words: DC-DC converter, Flyback converter, Photoflash capacitor charger, Fast charging time

1. Introduction

It requires high voltage over 300V for flashing the Xenon bulb commonly used in digital camera and mobile phone. For that reason, it requires large photoflash capacitor and charging circuit. Nowadays, the photoflash capacitor charger of micro-controlled flyback converter type is the most popular charging circuit because of its low power and small area characteristic [1]. The most important aspects of this structure are charging time and efficiency. Fast charging time is an advantage that user can have short latency time. And control logic block is the most important block to decide the charging time of the photoflash capacitor charger. To address this issue, various design techniques have been developed to fast transient response and to have high efficiency for flyback converter [2]-[4]. This paper proposes the architecture that the control logic block approaches for fast charging with high efficiency of photoflash capacitor charger. However, for faster charging time, the photoflash capacitor charger must select large peak current of transformer primary side current which gives a bad effect of battery life [5]. So, for user convenience, it can control widely current limiting by using proposed wide range of current limiter.

In this paper, section 2 reviews operation of photoflash capacitor charger. Section 3 describes conventional and proposed control logic block. The simulation and the experimental results are shown in section 4. At last, conclusion is shown in section 5 respectively.

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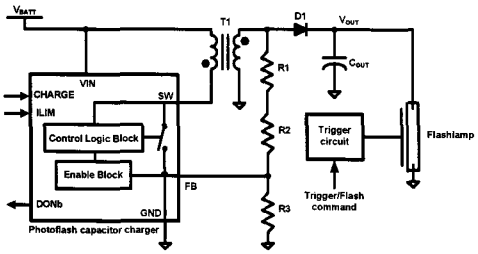
2. Operation of Photoflash Capacitor Charger

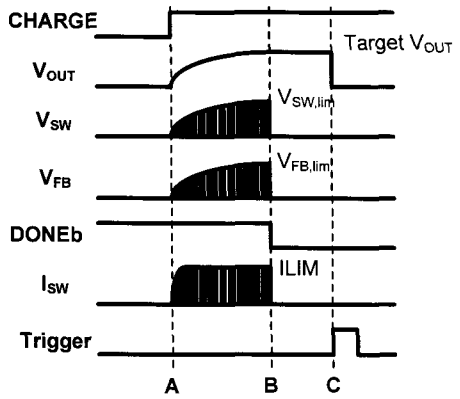
Fig. 1(a) shows the flashlamp circuitry using the photoflash capacitor charger of micro-controlled flyback converter type. This structure consists of transformer, photoflash capacitor, power switch (Power transistor) for primary current control of transformer, control logic block for switching of power switch, enable block for enable and disable of control logic block [6]. Fig. 1(b) shows timing diagram of the photoflash capacitor charger of micro-controlled flyback converter type. The charging operation of the photoflash capacitor charger of micro-controlled flyback converter type is started by a low-to-high signal on the CHARGE pin (A point in timing diagram). When a charging cycle is initiated, the transformer primary side current, $I_{Primary}$, ramps up linearly at a rate determined by the combined effect of the battery voltage, V_{BATT}, and the SW node voltage, V_{SW}, and the power switch

on-time, t, and the primary side inductance, $L_{Primary}$, as shown in equation (1).

When $I_{Primary}$ reaches the current limit, I_{LIM}, set by configuring the ILIM pin, the internal power switch is turned off immediately, allowing the energy to be pushed into the photoflash capacitor, C_{OUT}, from the secondary winding. The output voltage, V_{OUT}, rises by this repetitious process.



(a) Block diagram



(b) Timing diagram

Fig. 1. Flashlamp circuitry using micro-controlled flyback converter type photoflash capacitor charger.

$$I_{primary} = \frac{1}{L_{primary}} \cdot (V_{BATT} - V_{SW}) \cdot t \qquad (1)$$

While the internal power switch is turned off, V_{OUT} is sensed by a resistor string, R1 through R3, connected between the anode of the output diode, D1, and ground. This resistor string forms a voltage divider that feeds back to the FB pin.

$$V_{OUT} = \frac{R1+R2+R3}{R3} \cdot V_{FB} \qquad (2)$$

Where V_{FB} is FB node voltage. The resistors must be sized to achieve a desired output voltage. When V_{OUT} reaches the desired value, the charging process is terminated. And DONEb signal goes low to indicate the completion of the charging process (B point in timing diagram). After then, trigger circuit that operates by flash command discharges V_{OUT} to the flashlamp (C point in timing diagram). As a result, the flashlamp flashes the light.

3. Control Logic Block of Photoflash Capacitor Charger

3.1 Conventional Control Logic Block

Fig. 2 shows the control logic block of the conventional photoflash capacitor charger [6].

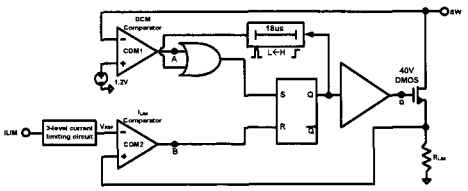


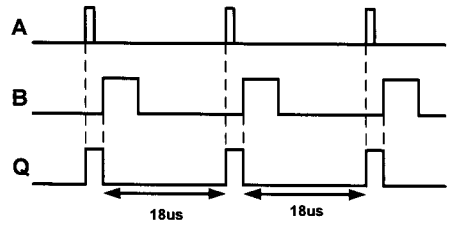
Fig. 2. Conventional control logic block

The feature of the conventional control logic block is as follows. At first, ILIM can be set to 3-level (1.0A, 1.2A, 1.4A) by configuring the ILIM pin (ground, float, Vdd). Lower input current offers the advantage of a longer battery lifetime. In the mean time, the highest current limit is required for faster charging time.

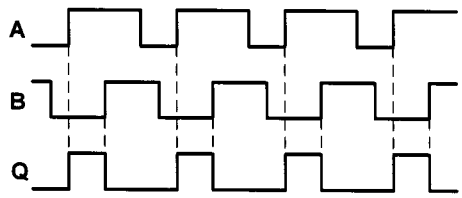
Second, the conventional architecture has two modes (timer mode and fast charging mode) by using ILIM comparator and DCM comparator. Fig. 3 shows the timing diagram of conventional control logic block.

The conventional architecture operates in the timer mode when it begins to charger a completely discharged photoflash capacitor, usually when V_{OUT} is less than 10 to 20V. Timer mode is fixed to 18μs off-time control. It can be recognized by

lowering initial input charging current as a result of a lower duty cycle, like soft start [7]. As V_{OUT} rises to more than 10 to 20V, converter operates near the discontinuous boundary, and sensing circuit tracks the fly-back voltage at SW node. As soon as this voltage swings below determined voltage, the internal power switch turns on again, starting the next charging cycle. The process is repeated like this and boosts the voltage to a goal voltage. The conventional architecture has a defect that charging time comes slow by long off-time duration (18μs) in the timer mode.



(a) Timer mode

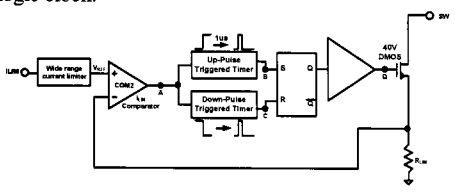


(b) Fast charging mode

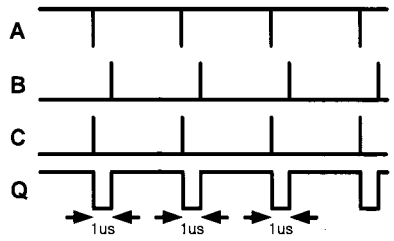
Fig. 3. Timing diagram of conventional control logic block.

3.2 Proposed Control Logic Block

Fig. 4 shows block and timing diagram of proposed control logic clock.



(a) Block diagram



(b) Timing diagram

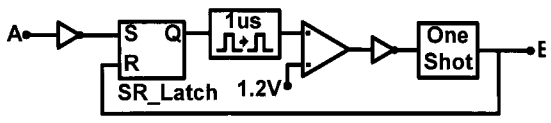
Fig. 4. Proposed control logic block.

Proposed control logic block operates one mode (fast charging mode) unlike the conventional architecture by taking off DCM comparator. And the proposed architecture puts the up-pulse triggered timer path with down-pulse triggered timer path and adjusted on-off time duration. Fig. 5 shows block diagram of proposed up-pulse and down-pulse triggered timer.

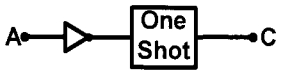
In the proposed architecture, the power switch on-time is decided by V_{BATT}, $L_{Primary}$, and I_{LIM}. And the power off-time is decided by delay cell in the up-pulse triggered timer. Equation (3) indicates minimum off-time, t_{OFF}, for full-discharge of transformer [5].

$$I_{LIM} = \frac{V_{OUT}}{n \cdot L_{primary}} \cdot t_{OFF} \tag{3}$$

Where n are transformer turns ratio. If n is 10 and I_{LIM} is 1.2A and V_{OUT} is 300V and $L_{Primary}$ is 14μH, t_{OFF} is 560ns of the calculation. So, up-pulse triggered timer is designed by using 1μs delay cell as it is enough time for the photoflash capacitor to charge delivering voltage from secondary side of transformer. As the result, it can respect fast charging time characteristic of photoflash capacitor charger by faster switching of power switch than conventional architecture.



(a) Up-pulse triggered timer



(b) Down-pulse triggered timer

Fig. 5. Proposed up-pulse & down-pulse triggered timer block diagram.

As the importance of the lower power characteristic for digital cameras and mobile phones is being increased day by day, low power photoflash capacitor charger is required. So wide range current limiter is proposed for adjusting low power application. Fig. 6 shows the block diagram of the proposed wide range current limiter.

The operation of the wide range current limiter is as follows. The inner comparators decide upper and lower side of current limiting point. And, 2.5R and R are used for preventing the ILIM node noise voltage [8]-[9]. If ILIM node voltage, V_{ILIM}, is less than 0.7V, the output voltage, V_{out}, is 0.2V. On the other hand, if V_{ILIM} is over 2.8V, V_{out} is 0.8V. If V_{ILIM} is from 0.7V to 2.8V, V_{out} has proportional value from 0.2V to 0.8V. Designed R_{LIM} is 0.5Ω in figure 4(a). According to Ohm's law, the proposed wide range current limiter can control I_{LIM} range from 0.4A to 1.6A. Fig. 7 shows V_{out} and I_{LIM} as V_{ILIM} of the proposed wide range current limiter.

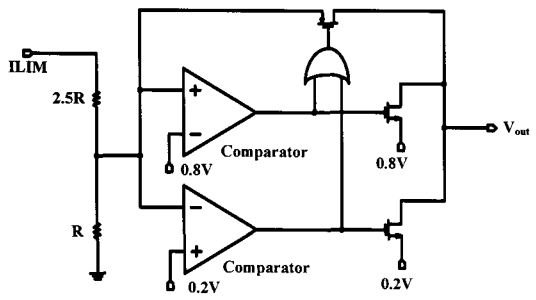
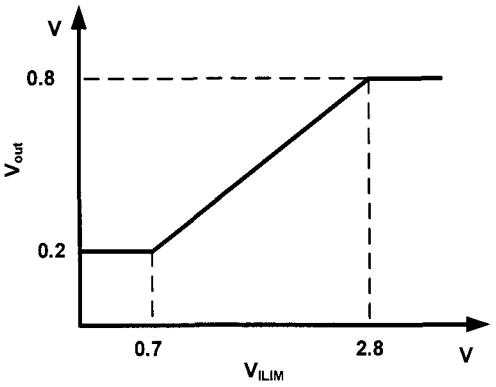
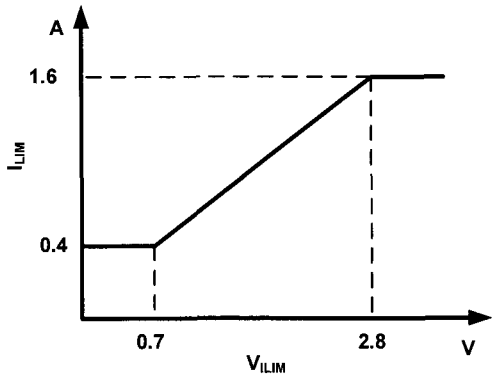


Fig. 6. Proposed wide range current limiter block diagram.



(a) V_{out} vs. V_{ILIM}



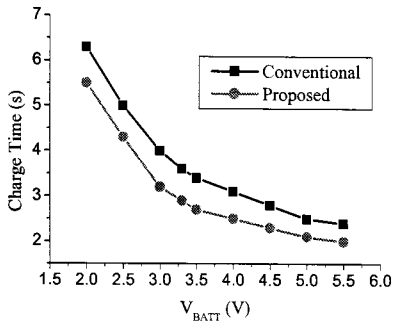
(b) I_{LIM} vs. V_{ILIM}

Fig. 7. Proposed wide range current limiter V_{out} and I_{LIM} as V_{ILIM}.

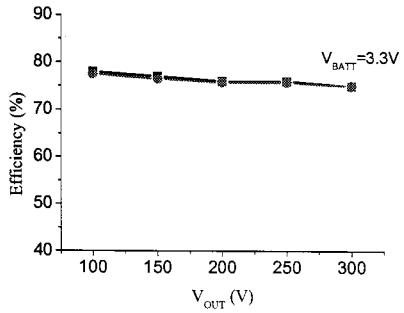
4. Simulation and Experimental Results

To verify the performance of the photoflash capacitor charger using proposed control logic block and wide range current limiter, the simulation is conducted charging time, efficiency and current limiting range. For comparison, the same simulation is also conducted with the conventional architecture. Fig. 8(a), (b) shows the results of the simulation for charging time and efficiency. The proposed photoflash capacitor charger has faster charging time as similar to conventional structure efficiency.

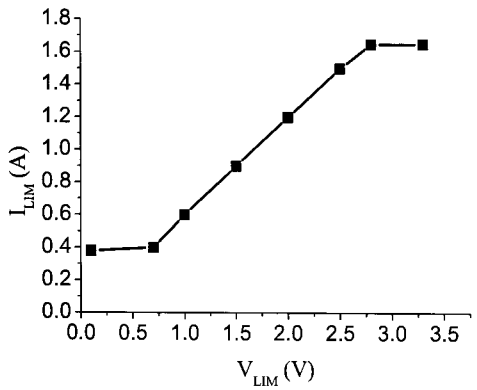
Figure 8(c) shows the result of the simulation for proposed photoflash capacitor charger current limiting range as V_{LIM}.



(a) Charging time



(b) Efficiency



(c) Current limiting range

Fig. 8. Simulation results.

The chip is fabricated in a 1-poly 4-metal 0.35-μm high voltage CMOS process. Fig. 9 shows the chip microphotograph. The DMOS (Double-diffused Metal Oxide Semiconductor) is used for the power switch, and a protection circuit is designed. And it is integrated IGBT driver to drive of an IGBT for ramp trigger circuit. Fig. 10 shows the experimental circuit for testing the proposed architecture. And Fig. 11 shows the implemented test board. A TTRN-060S-015 transformer made by Tokyo Coil Engineering Company is used. This transformer turns ratio is 10 and $L_{Primary}$ is 14μH. Fig. 12 is the Experimental results of V_{OUT} at 3.3V V_{BATT}, 1.2A I_{LIM} by the Tektronix TDS2024 analog oscilloscope. The vertical axis is 50V per division and the horizontal axis is 1s per division. Table 1 shows the performance of the proposed photoflash capacitor charger.

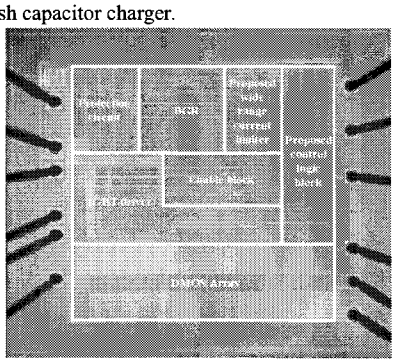


Fig. 9. Microphotograph of proposed photoflash capacitor charger.

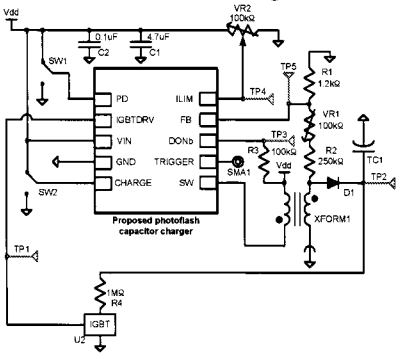


Fig. 10. Experimental circuit for testing proposed architecture

Fig. 11. Proposed photoflash capacitor charger test board

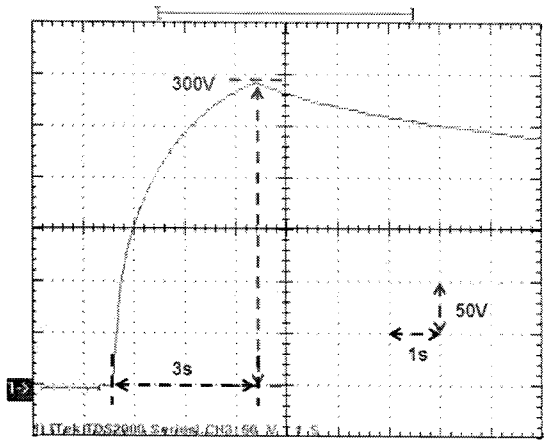


Fig. 12. Experimental results of V_{OUT} @ 3.3V V_{BATT}, 1.2A I_{LIM}

Table 1. Performance summary

		Conventional [6]	Proposed	Units
Supply voltage (V_{BATT})		3.0 ~ 5.5	3.0~ 5.5	V
Supply current	Charging	5	4.8	mA
	Charging done	1	1	μA
	Shutdown	0.01	0.01	μA
SW Maximum Off-time		18	1	μs
SW Maximum On-time		18	4	μs
I_{LIM}		1.0, 1.2, 1.4	0.4 ~ 1.6	A
Charging time to 300V @ 3.3V Vdd, 1.2A I_{LIM}		3.8	3	s
Efficiency		> 75	> 75	%
Area		2.23 x 1.64	1.6 x 1.3	mm

5. Conclusion

In this paper, the photoflash capacitor charger that has faster charging time with high efficiency by proposed control logic block is designed, simulated, and fabricated. And the proposed wide range current limiter has an advantage that user can adjust current limiting value for user convenience between charging time and battery life. The proposed photoflash capacitor charger has 3s charging time at 3.3V battery voltage, 1.2A current limit condition. It is well-suited for portable device application such as digital camera, digital video camera, and mobile phone with camera.

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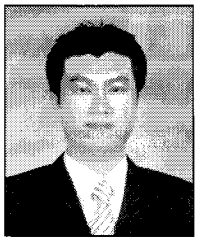

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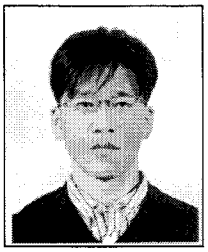

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