

# Gray Scale Plasma Display Panel with a New High-Speed Drive

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## Abstract

The objective of this study is to evaluate the characteristics of a newly proposed high-speed drive method for the gray scale display for high-resolution plasma display panels (PDP). In the experiment it was found that the characteristics of gray scale display are not closely affected by a priming period below 50[ $\mu$ s], the width of the priming period, and that it can be driven stably from the brightest sub-field to the darkest sub-field even though a priming discharge is applied to the 1 TV-field only once. Moreover, from the experimental result, the gray scale pattern of 8-bit and 9 sub-fields was stably displayed in the experimental PDP with scan pulses having the pulse width of 0.7[ $\mu$ s]. An address voltage margin of about 25[V] and a sustain voltage margin of about 10[V] was obtained.

Key Words : HDTV, plasma display panel, drive method, gray scale, discharge

## 1. Introduction

Demand for large-screen flat panel displays is expanding explosively due to the popularization of digital TV broadcasting. The plasma display panel (PDP) is the display that is the most suitable for large-screen, high-definition (HD) TV because it is easy to convert to the large-screen style and because of the digitized display mode for image information. The trend of HDTV is shifting to FHD with its 1080 horizontal scanning lines

(=scan line). PDP is relatively difficult to convert to a high-quality image on account of the large-screen conversion of the liquid crystal display (LCD), which has already achieved high-quality, FHD level images. Therefore there is a close market competition between the two.

In PDP, the brightness decreases on the principle of drive when the number of scan lines and the gray scale increases. For single scanning HD PDP scanning sequentially all scan lines, when considering the brightness, image quality, or reliability, around 768 scan lines are the limit of the drive. The commercialized FHD PDP overcomes this limit using either a dual scanning mode that scans horizontally and simultaneously by dividing the panel in half or an interlaced scanning mode such as cathode ray tube (CRT) [1-2]. In the former case, since number of driver

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IC on the data side increases by two, the circuit cost increases. This also has a lowered picture quality for stationary images.

This drive limit is caused mainly by the ADS (address display separated) drive technology [3] that is applied in the commercialized PDP. The AWD (address while display) drive technology is being studied for improvement [4]. However, since high-voltage pulses for the priming discharge [5] should be applied on a different timing for each scan line, there is the drawback of an increased number of high-voltage drive circuits. Moreover, this drive technology is not yet ready for the market since the scan lines cannot be scanned sequentially and, accordingly, the commercial driver IC cannot be used.

In a previous study, a new drive mode was proposed that has overcome the limits of the high-speed drive via the ADS drive mode while improving the drawback of the AWD drive mode. A test was conducted to ensure its validity [6]. In this study, an experiment was made on gray scale displays using the test PDP to review the commercial possibilities of the proposed high-speed drive technology. Drive conditions for displaying gray scale stably were derived through this experiment.

## 2. Experiments

As shown in Fig. 1, the proposed PDP high-speed drive mode has a structure in which the current field (Nth) and the previous field (N-1th) are blended within 1 TV-field. The 1 TV-field consists of sub-fields arranged time-sequentially along the address line as shown in the figure. Each sub-field consists of an address period and sustain period [6]. The priming period is also installed in the front face of the panel overlapping with this sustain period. One priming

period was set in 1 TV-field.

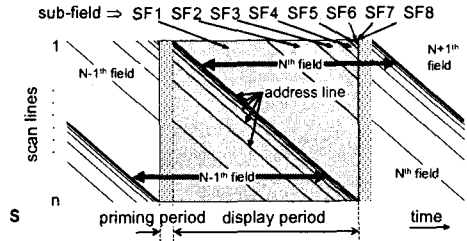


Fig. 1. TV-field structure of the proposed drive method

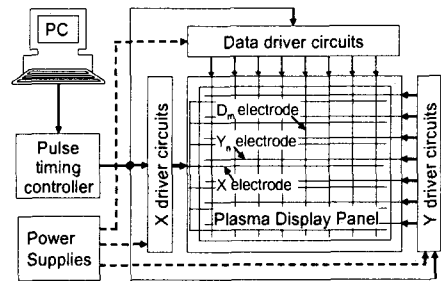


Fig. 2. Schematic block diagram of the PDP drive system

Fig. 2 shows a block diagram of the test PDP drive system used in the experiment. This equipment is constructed of the driver circuits that supply high-voltage pulses to each electrode of the test PDP, the pulse timing controller that controls the pulse timing of these driver circuits, and the power supply [6]. The electrode structure of the test PDP is the same as the electrode structure of the commercial 3-electrode surface discharge AC PDP. The electrodes of one pair installed horizontally in the panel are the X and Y electrodes, and the electrode pair installed vertically is the D electrode. The diagonal size of the test PDP is 6 inches, the pixel pitch is 220[μm], and total number of pixels is 80×80×3. The measurement of discharge was conducted with an oscilloscope, an IR-ray semiconductor sensor with a maximum strength of 828nm, and the C6386 amplifier of the Hamamatsu Photonics Company.

Fig. 3 shows the detailed timing diagram of the drive pulses used in this study. After two sustain pulses are applied continuously to the X and Y electrodes, one rest period is installed. The address period is inserted during this rest period. The address discharge occurs due to the sum of the scan pulse voltage and the data pulse voltage applied respectively to the Y and D electrodes. In the data pulse, the pulse width and applied timing coincided with the scan pulse. The priming period expands and installs one rest period, and also applies a ramp-shape priming pulse simultaneously to all the X electrodes of the priming pulse.

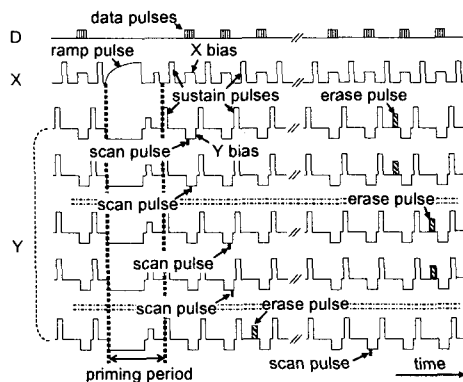


Fig. 3. Timing chart of drive pulses for the proposed drive method

### 3. Results and Discussion

Fig. 4 shows the gray scale display image of the 8-bit and 9 sub-fields having driven the test PDP at a high speed with a scan pulse having a pulse width of  $0.7\mu\text{s}$ . From the figure it can be seen that images are stably displayed from the darkest gray level to the brightest gray level with this drive technology.

Fig. 5 shows the light output of the drive pulses measured with an oscilloscope. This shows that a priming discharge by priming pulse occurs only in (a) of the sub-field where the sustain discharge

did not occur, and the address and sustain discharges occur stably.

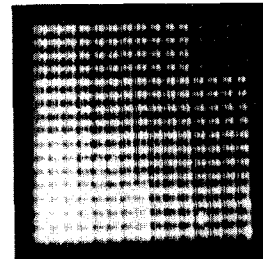
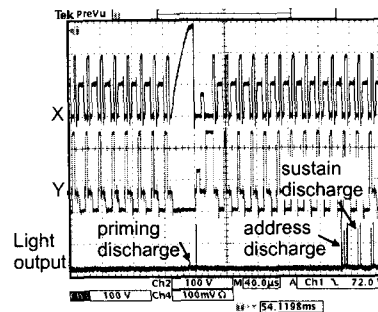
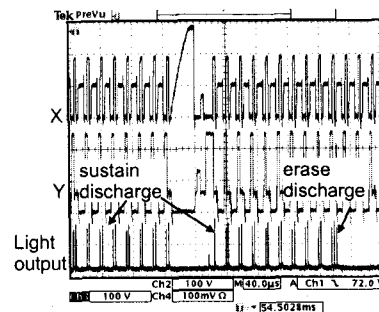


Fig. 4. Gray scale display image of an actual panel driving with a scan pulse width of  $0.7\mu\text{s}$



(a) Where the sustain discharges are not generated

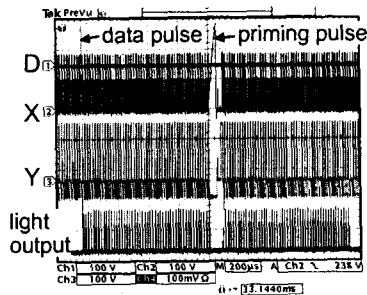


(b) Where the sustain discharges are generated

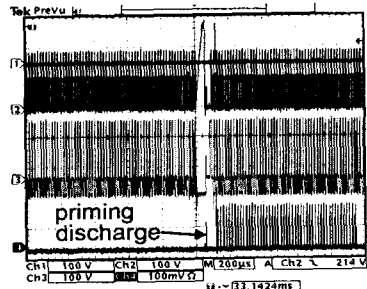
Fig. 5. Light output of priming, sustain, address and erase discharges

Fig. 6 shows the light output of the sustain discharge measured in the sub-field of (a) and (b), which has the most sustain pulse, and the sub-field of (c) and (d), which has the fewest sustain pulses. Priming discharge occurs only

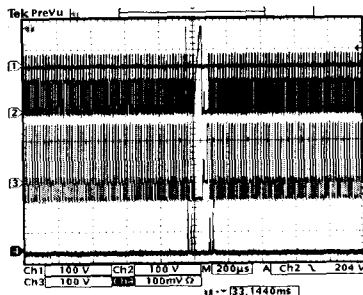
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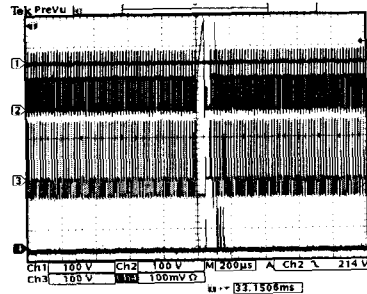
(a) Sub-field with maximum sustain pulses, with priming pulse inserted during the sustain discharges



(b) Sub-field with maximum sustain pulses, with priming and sustain discharges generated



(c) Sub-field with minimum sustain pulses, with priming pulse inserted during the sustain discharges



(d) Sub-field with minimum sustain pulses, with priming and sustain discharges generated

Fig. 6. Light output of discharges in each sub-field during 1 TV-field

when there is no sustain discharge even when the number of sustain pulse is few similarly to when there are many sustain pulses. This indicates that the gray scale can be stably displayed using the proposed drive mode.

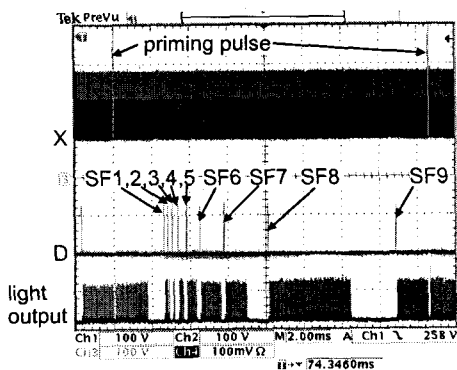


Fig. 7. Light output of sustain discharges in all sub-fields during 1 TV-field.

Fig. 7 shows the light output of discharges at all the sub-fields applied during 1 TV-field. Regarding the number of sustain pulses applied to each sub-field, the sub-field having the fewest number of pulse has 2 pulses respectively in the X and Y electrodes, and the sub-field having the greatest number of pulse has 256 pulses. From the figure it can be seen that sustain discharges occur stably in sub-fields representing each gray scale.

Fig. 8 shows the operating margin of the address discharge voltage and sustain discharge voltage upon display of the gray scale, which is measured while varying the width of the priming period. From the experiment it was found that the address and sustain discharge voltage is not affected by the width of the priming period although it was widened to 50[ $\mu$ s]. An address voltage margin of about 25[V] and a sustain

voltage margin of about 10[V] was obtained.

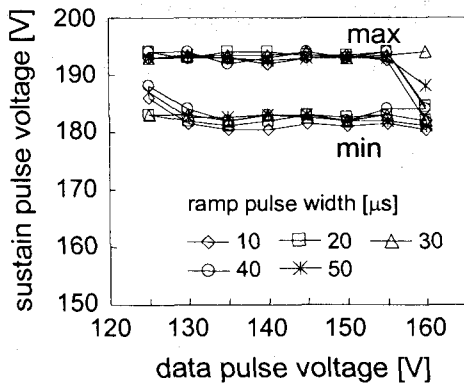


Fig. 8. Relationship between address and sustain discharge voltage with varying width of priming periods

#### 4. Conclusion

In this study, the gray scale display characteristics of a newly-proposed high-speed drive method for high-resolution plasma display panels (PDP) were evaluated. The results indicated that, in displaying gray scale, the width of the priming period is not closely affected by the drive characteristics of this drive technology although the width of the priming period was widened to 50[ $\mu$ s]. Also, it can be stably driven from the brightest sub-field to the darkest sub-field even though a priming discharge is applied only once to a 1 TV-field. This drive mode displayed a gray scale of 8-bit and 9 sub-fields with scan pulses having a pulse width of 0.7[ $\mu$ s], and at the same time, an address voltage margin of about 25[V] and a sustain voltage margin of about 10[V] was obtained. The address voltage margin decreased by 15[V], compared to existing study results that did not consider the display of gray scale [6]. Therefore, in order to apply the newly proposed drive mode to an actual large-scale PDP, a study of the optimization of large-scale drive charac-

teristics is required with consideration for the panel features.

#### Acknowledgements

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#### Biography

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Received B.S., M.S. and Ph.D. degrees in electrical engineering from Seoul National University in 1987, 1989 and 1992, respectively. From 1992-1995, he worked for LG Electronics Co. Ltd. in Korea to study information display systems and plasma displays. From 1996-1999, he worked for Samsung SDI Co. Ltd. in Korea to study drive technology for plasma displays. From 2000-2005, he was with Kyeongju University in Korea. He is now with the Department of Electrical Engineering, Soongsil University, in Korea.