SIPAC

2006년 1월부터 2월까지 32개의 IP가 SIPAC에 새로 등록되었습니다. 지면관계상 20개의 IP의 정보를 제공해 드리며, SIPAC 홈페이지(http://www.sipac.org)를 방문하시면 그 외 IP에 대한 보다 다양하고 자세한 정보를 보실 수 있습니다. (Total: 1931 개)

No.	IP Name (Type/Format)	Seller	Category	Description
1	AMBA AHB compatible 4X5 partial crossbar switch(Soft IP / VHDL)	Seoul National University(www.snu.ac.kr)	Bus Interface 〉 AMBA	This IP is an AMBA AHB compatible partial crossbar switch. Four masters and five slaves can be attached. One master can access all slaves and the others can access two slaves.
2	HelloCellular(Soft IP, Hard IP / Verilog, GDS II)	HelloSoft Inc.(www.hellosoft.com)	Wireline Communication	HelloCellular solutions (GSM/GPRS/EDGE) include L1/L2/L3 layers which support Class B, C, Multi-Slot Classes 1-14 and Multiband. The solution is flexible and customizable for various architectures.
3	HelloVoice(Soft IP / Verilog)	HelloSoft Inc.(www.hellosoft.com)	Wireline Communication	HelloVoice™ Industry's most optimized and comprehensive software solution for implementing Voice over Packet terminals like IP Phones, VoWLAN (Voice Over Wireless LAN) handsets, Dual mode cellular handsets, ATAs (Analog Telephone Adaptor), SOHO gateways and other CPE devices on RISC processor architectures like ARM, MIPS, XScale and OMAP.
4	ECC security processor(Soft IP / Verilog)	HelloSoft Inc.(www.hellosoft.com)	Others	This ip can operate scalar multiplication of ECC(Elliptic Curve Cryptographic). This ip is used Radix-4 modified booth algorithm. This algorithm's amount of operation is smaller then Double-and-add algorithm, therefore this ip have small area and fast speed.
5	DRPIC166X - High Performance Configurable 8-bit RISC Microcontroller(Soft IP, Firm IP / VHDL, Verilog, EDIF)	Digital Core Design(www.dcd.pl)	General Processor & Microcontroller	The DRPIC166X is a low-cost, high performance, 8-bit, fully static soft IP Core, dedicated for operation with fast (typically on-chip) dual ported memory. The core has been designed with a special concern about low power consumption assuring the best power consumption, price and performance combination on the IP market.
6	DR80390 - High Performance 8-bit Microcontroller(Soft IP, Firm IP / VHDL, Verilog, EDIF)	Digital Core Design(www.dcd.pl)	General Processor & Microcontroller	DR80390 is a high performance, area optimized soft core of a single-chip 8-bit embedded controller dedicated for operation with fast (typically on-chip) and slow (off-chip) memories. The core has been designed with a special concern about low power consumption.
7	DR80390CPU - High Performance 8-bit Microcontroller(Soft IP, Firm IP / VHDL, Verilog, EDIF)	Digital Core Design(www.dcd.pl)	General Processor & Microcontroller	DR80390CPU is a high performance, area optimized soft core of a single-chip 8-bit embedded controller dedicated for operation with fast (typically on-chip) and slow (off-chip) memories. The core has been designed with a special concern about low power consumption.
8	Line based 2-D lifting DWT processor(Soft IP / VHDL)	Chonnam National University(www.chonnam.ac.kr)	Digital Signal Processing	This processor conducts 2-D lifting based DWT(discrete wavelet transform) for bi-orthogonal (9,7) filter. It produces 4-level wavelet coefficients in an interleaved fashion by RPA(Recursive Pyramid Algorithm) scheduling for 128x128 input image.

No.	IP Name (Type/Format)	Seller	Category	Description
9	VPP Generator for FLASH Memory using Magnachip 0.25um CMOS Process(Hard IP / GDS II)	Changwon National University(www.changwon. ac.kr)	Memory Element 〉 Flash Memory	Block diagram of VPP Generator for Flash Memory is composed of Reference Voltage Generator, Voltage-Up Converter, VPP Level Detector, Ring Oscillator, VPP Control Logic and Charge Pump
10	Charge Pump for FLASH Memory using DongbuAnam 0.13um CMOS Process(Hard IP / GDS II)	Changwon National University(www.changwon. ac.kr)	Memory Element 〉 Flash Memory	Block Diagram of VPP Generator is composed of VPP BIAS, VPP Level Detector, Ring Oscillator, VPP Control Logic and charge Pump.
11	RFID-Sensor(Soft IP / GDS II, Spice)	KAIST(www.kaist.ac.kr)	Wireless Communication 〉 Others	UHF(900MHz) RFID Tag Chip It integrates temperature and photo sensors for environmental monitoring. It has the UHF band RF interface with the base station, and its forward and down link has the data rate of 20kbps.
12	RamP-Lite : A 3D graphics rendering core(Soft IP / Verilog)	KAIST(www.kaist.ac.kr)	Graphic 〉 Rendering Engine	A 3D graphics rendering core for handheld systems. It supports OpenGL simple lighting, triangle setup, Gouraud shading, texture mapping/blending, depth test and alpha blending.
13	LAU – The Arithmetic Unit for 3D Graphics System(Soft IP / Verilog)	KAIST(www.kaist.ac.kr)	Arithmetic & Logic Function 〉 Arithmetic & Logic Unit	The arithmetic Unit for 3D graphics system. It calculates the complex functions such as division and reciprocal by logarithmic number system. It consists of 2-stage pipelined architecture. It calculates the complex functions in 2-cycle.
14	DA-1 : User-programmable Mobile Graphics Processor(Soft IP / Verilog)	KAIST(www.kaist.ac.kr)	Graphic 〉 Processor	DA-1 is a 155mW, 50Mvertices/s, 50Mpixels/s user-programmable mobile graphics processor with ARM10 compatible RISC processor, reconfigurable streaming SIMD vertex shader, low power rendering engine and programmable frequency synthesizer for 2D/3D mobile multimedia applications
15	DP80390CPU – Pipelined High Performance Microcontroller(Soft IP, Firm IP / VHDL, Verilog, EDIF)	Digital Core Design(www.dcd.pl)	General Processor & Microcontroller	The core has been designed with a special concern about performance to power consumption ratio. This ratio is extended by an advanced power management unit PMU.
16	DR8051XP – High Performance Configurable 8-bit Microcontroller(Soft IP, Firm IP / VHDL, Verilog, EDIF)	Digital Core Design(www.dcd.pl)	General Processor & Microcontroller	Advanced power management unit makes DR8051XP core perfect for portable equipment where low power consumption is mandatory.
17	A CMOS 0.18um 3.2~3.7GHz Frequency Synthesizer with Programmable Dual Modulus Divider(Hard IP / GDS II)	Chonbuk National University(www.chonbuk.a c.kr)	Analog & Mixed Signal 〉 RF Circuit 〉 Others	3.2 ~ 3.7GHz frequency synthesizer with programmable dual modulus divider is designed. The simulated results are as followings – Locking time : 35us in 40KHz loop bandwidth – Power dissipation : 15mW – Phase noise in VCO : –118dBc/Hz at 1MHz offset
18	Design of two stage power amplifier with on-chip matching for IEEE 802.11a WLANs applications(Hard IP / GDS II)	Chonbuk National University(www.chonbuk.a c.kr)	Analog & Mixed Signal 〉 RF Circuit 〉 RF Power Amplifier	The designed power amplifier operates in 5.15~5.35GHz – gain = 8.74dB – output power = 20.6dBm – drain current = 177mA – supply voltage = 1.8V
19	Current Reused Complementary VCO with Differential Outputs(Hard IP / GDS II)	ICU(www.icu.ac.kr)	Analog & Mixed Signal	Complementary VCO with Current Reused scheme Low phase noise –120@ 1M offset Low power dissipation : 0.8mA @ 1.8V supply Differential Outputs with single ended structure
20	A 3rd Order Complex Filter for Low IF zigbee Receiver(Hard IP / GDS II)	ICU(www.icu.ac.kr)	Analog & Mixed Signal	Complex –BPF for Low IF Receiver at 2.4GHz Zigbee Application – Low power – Controllable Center Frequency 4MHz – Image rejection at IF frequency