: IP Catalog

SIPAC

2005년 10월부터 12월까지 90개의 IP가 SIPAC에 새로 등록되었습니다. 지면관계상 25개의 IP의 정보를 제공해 드리며, SIPAC 홈페이지(http://www.sipac.org)를 방문하시면 그 외 IP에 대한 보다 다양하고 자세한 정보를 보실 수 있습니다. (Total: 1899 개)

No.	IP Name (Type/Format)	Seller	Category	Description
1	META multi-threaded RISC/DSP(Soft IP / VHDL)	Imagination Technologies (www.imgtec.com)	General Processor & Microcontroller	META is a multi-threaded RISC/DSP processor.
2	On-Chip Synchronous SSRAM Controller(Soft IP, Hard IP / VHDL)	Seoul National University(www.snu.ac.kr)	Peripheral Core 〉 Controller 〉 Memory Controller	On-Chip Synchronous SSRAM Controller는 SoC에 내장되는 Synchronous SSRAM을 AHB 버스에 연결해 주는 컴포넌트이다.
3	External Asynchronous SRAM Controller(Soft IP, Hard IP / VHDL)	Seoul National University(www.snu.ac.kr)	Peripheral Core 〉 Controller 〉 Memory Controller	External Asynchronous SRAM Controller는 Asynchronous SRAM 타입의 메모리를 연결할 수 있는 컴포넌트이다. 이 컴포넌트는 하나의 NOR/NAND 플래시 메모리와 세개의 SRAM/ROM을 연결할 수 있으며, 타이밍을 프로그래밍할 수 있다.
4	UART(Soft IP, Hard IP / VHDL)	Seoul National University(www.snu.ac.kr)	Bus Interface 〉 UART	UART Controller는 16 depth의 Receiver/Transmitter FIFO를 내장하고 있으며, Parity bit 생성, Hardware flow control, Programmable baud rate등의 기능을 지원한다.
5	TFT LCD Controller(Soft IP, Hard IP / VHDL)	Seoul National University(www.snu.ac.kr)	Peripheral Core 〉 Controller 〉 LCD Controller	TFT-LCD Controller는 Memory의 RGB 영상 데이터 또는 YUV 영상 데이터를 자체적으로 내장한 DMA를 이용해 순차적으로 읽어온 후, TFT-LCD 패널에 타이밍을 맞춰 전송한다.
6	AHB2AHB Bridge(Soft IP, Hard IP / VHDL)	Seoul National University(www.snu.ac.kr)	Bus Interface 〉 AMBA	AHB2AHB Bridge는 두개의 AHB 버스를 중계한다. 한개의 AHB Bus는 Master Bus로서 읽기 혹은 쓰기 요청을 발생하고, 다른 하나는 Slave Bus로서 Master Bus부터의 데이터 전송 요청을 받아 처리한다.
7	AHB Bus Matrix(Soft IP, Hard IP / VHDL)	Seoul National University(www.snu.ac.kr)	Bus Interface 〉 AMBA	AHB Bus Matrix는 AHB Bus Arbiter와 Muliplexer를 통합한 것이다. AHB Bus Matrix는 Arbitration 방식과 제공하는 AHB Master 인터페이스, AHB Slave 인터페이스에 따라 다양한 모델이 제공된다.
8	Reset Generator(Soft IP, Hard IP / VHDL)	Seoul National University(www.snu.ac.kr)	Others	Reset Generator는 프로세서의 지시에 따라 일정 시간 동안 주변 장치 Reset 신호를 발생시킬 수 있다. 이 Peripheral Reset Generator는 FPGA 프로토타입을 위해 구현되었으며, AHB 인터페이스를 통해 제어할 수 있다.
9	D8255 – Programmable Peripheral Interface(Soft IP/ VHDL, Verilog, EDIF)	Digital Core Design(www.dcd.pl)	Peripheral Core 〉 Peripheral Interface	The D8255 is a programmable I/O device which is designed for use with all Intel and most other microprocessors. It provides 24 I/O pins which may be indi-vidually programmed in 2 groups of 12 and used in 3 major modes of operation
10	8259 – Programmable Interrupt Controller(Soft IP/ VHDL, Verilog, EDIF)	Digital Core Design(www.dcd.pl)	Peripheral Core 〉 Controller 〉 Interrupt Controller	The D8259 is a soft Core of Programma-ble Interrupt Controller. It is fully compatible with the 82C59A device. The D8259 Core manages up to 8-vectored priority interrupts for processor.
11	DI2CM – I2C Bus Interface – Master(Soft IP/ VHDL, Verilog, EDIF)	Digital Core Design(www.dcd.pl)	Bus Interface 〉 I2C (Inter Integrated Circuit)	I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data transmission over a short distance between many devices. The DI2CM core provides an interface between a microprocessor / microcontroller and an I2C bus.
12	DFP2INT – Floating Point To Integer Pipelined Converter(Soft IP/ VHDL, Verilog, EDIF)	Digital Core Design(www.dcd.pl)	Arithmetic & Logic Function	The DFP2INT is the pipelined floating point to integer converter. The input and output numbers format is according to IEEE-754 standard. DFP2INT supports single precision real numbers and double word integers (4 Bytes).

No.	IP Name (Type/Format)	Seller	Category	Description
13	USB 2.0 Function Controller OVA Checker AIP(Soft IP / Vera)	Silicon Interfaces(www.siliconinterfaces.com)	Test Core	USB 2.0 Function Controller OVA Checker AIP is fully documented off the shelf component for the Developers of the USB 2.0 compliant function controller.
14	Sigma-Delta Modulators for Radio Frequency Applications(Soft IP, Hard IP / VHDL, Verilog, GDS II, Available as RTL & GDSII as well as Verilog-A or S)	Intrinsix Corp.(www.intrinsix.com)	Wireless Communication	The Intrinsix Sigma-Delta Modulators for Radio Frequency Applications (Sigma-Delta-M-RF™) are part of the larger offering of Sigma-Delta IP available from Intrinsix.
15	AES Core(Soft IP/ VHDL)	Algotronix Ltd.(www.algotronix.com)	Data Transmission 〉 Encryption 〉 AES	Complete implementation of AES algorithm – all key lengths (128, 192, 256 bits), Encrypt, Decrypt or Encrypt/Decrypt function, all standardised modes (ECB, CBC, OFB, CFB1, CFB8, CFB128, CTR).
16	DFPSQRT – Floating Point Pipelined Square Root Unit(Soft IP / VHDL, Verilog, EDIF)	Digital Core Design(www.dcd.pl)	Arithmetic & Logic Function 〉 Square Root	The DFPSQRT uses the pipelined mathematics algorithm to compute square root function. The input number format is according to IEEE-754 standard. DFPSQRT supports single precision real numbers.
17	Intrinsix Sigma-Delta ADCs for Precision Data Conversion(Soft IP, Hard IP / VHDL, Verilog, GDS II, Available as RTL and GDSII as well as RTL and Beha)	Intrinsix Corp.(www.intrinsix.com)	Analog & Mixed Signal 〉 Data Converter	A design methodology that is geared towards a digital CMOS process helps reduce cost, die size and power consumption. A high Signal to Noise Ratio (SNR) is achieved by pushing the frequency of the quantization noise outside the band of interest.
18	DF6811 – 8-bit FAST Microcontrollers Family(Soft IP / VHDL, Verilog, EDIF)	Digital Core Design(www.dcd.pl)	General Processor & Microcontroller 〉 Microcontroller	The DF6811 is a advanced 8-bit MCU IP Core with highly sophisticated, on chip peripheral capabilities. DF6811 soft core is binary-compatible with the industry standard 68HC11 8-bit microcontroller and can achieve a performance 45-100 million instructions per second.
19	USB On-The-Go(Soft IP / Verilog)	Silicon Interfaces(www.siliconinterfaces.com)	Data Transmission	Peripheral mode / Host mode. When acting as a peripheral, SI22USBOTG10 provides all the encoding, decoding and checking needed in sending and receiving USB packets
20	Ittiam MP3 Decode on ARM9(Software IP)	Ittiam Systems (www.ittiam.com)	Video / Image / Audio	MPEG-1/2 Layer 1,2,3 Decoder optimized for ARM9
21	Ittiam AEC for ARM9E(Software IP)	Ittiam Systems(www.ittiam.com)	Video / Image / Audio	Acoustic Echo Canceller on ARM9E
22	Ittiam 802.11a PHY(Soft IP / Verilog)	Ittiam Systems(www.ittiam.com)	Wireless Communication 〉 802.11	Ittiam 802.11a PHY IP Core is a licensable and synthesizable HDL implementation of IEEE Standard 802.11a 1999 Edition in Verilog/VHDL. The IEEE 802.11a specification is the high speed Physical Layer in the 5 GHz band designated for U-NII applications.
23	Ittiam 802.11 MAC(Soft IP / Verilog, C/C++)	Ittiam Systems(www.ittiam.com)	Wireless Communication 〉 802.11	Ittiam 802.11 MAC is IEEE standards PICS compliant and is real time tested on Ittiam WLAN Validation Platform. It is also internally verified for Wi-Fi compliance.
24	UART eVC(Soft IP / e Language)	Silicon Interfaces(www.siliconinterfaces.com)	Test Core	Silicon Interfaces' UART eVC is a fully documented, off the shelf component for Verisity's Specman EliteTM functional verification environment.
25	DFPIC165X – High Performance 8-bit RISC Microcontroller(Soft IP / VHDL, Verilog, EDIF)	Digital Core Design(www.dcd.pl)	General Processor & Microcontroller	The DFPIC165X is a low-cost, high performance, 8-bit, fully static soft IP Core, dedicated for operation with fast memory (typically on-chip). The core has been designed with a special concern about low power consumption.