Realization of Two-bit Operation by Bulk-biased Programming Technique in SONOS NOR Array with Common Source Lines

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We report for the first time two-bit operational characteristics of a high-density NOR-type polysilicon-oxide-nitride-oxide-silicon (SONOS) array with common source line (CSL). An undesired disturbance, especially drain disturbance, in the NOR array with CSL comes from the two-bit-per-cell operation. To solve this problem, we propose an efficient bulk-biased programming technique. In this technique, a bulk bias is additionally applied to the substrate of memory cell for decreasing the electric field between nitride layer and drain region. The proposed programming technique shows free of drain disturbance characteristics. As a result, we have accomplished reliable two-bit SONOS array by employing the proposed programming technique.

Keywords : SONOS NOR array, Two-bit operation, Disturbance, Common source lines, Bulk-biased programming technique

1. INTRODUCTION

There have been great amounts of demands on the ultra-high-density flash memory devices for the mobile communication and electronic devices[1]. One of the most important issues for the ultra-high-density flash memory is scalability of memory cell. Polysilicon-oxide-nitride-oxide-silicon (SONOS) memory has been considered as the most promising candidate in commercial products because of its possible scalability, simple fabrication process, and full compatibility with the poly-gate complementary metal-oxide-semiconductor (CMOS) process[2,3].

NROM™ with the SONOS structure has been recently introduced by B. Eitan et al.[4,5]. The NROM™ reduced the area per bit by achieving the two-bit-per-cell operation. The NROM™ cell is programmed by channel hot electron injection, and typically by applying 9 V to the gate and 5 V to the drain. However, program disturbance in the NROM™ cell array may come from an unselected cell sharing the same bit line and word line as cell being programmed due to high gate and drain voltage[6].

In this study, we report for the first time two-bit operational characteristics of a high-density NOR-type SONOS array with common source line (CSL). An undesired disturbance, especially drain disturbance, in the NOR array with CSL comes from the two-bit-per-cell operation by applying a conventional CHE programming method. To solve this problem, we propose an efficient bulk-biased programming technique.

2. EXPERIMENTAL DETAILS

The SONOS NOR arrays with common source lines

are fabricated by employing conventional CMOS process technology. The processing sequence is identical to standard CMOS technology, except for the formation of the oxide-nitride-oxide (ONO) dielectric stack. The process for the ONO gate dielectric is as follows: The bottom oxide is thermally grown at 900 °C in nitrogen diluted with oxygen (5 % O_2 in N). The nitride is deposited using low-pressure chemical-vapor deposition (LPCVD) at a low chamber pressure of 0.5 Torr and 770 °C by reacting of dichlorosilane (SiH_2Cl_2):ammonia (NH_3)= 30:330 sccm. The blocking oxide is grown by wet oxidation at 950 °C with a gas flow ratio of hydrogen (H_2):oxygen (O_2)= 5:10 ℓ/min. The thicknesses of the ONO stack measured by transmission electron microscopy (TEM) are 34 Å for the bottom oxide, 73 Å for the nitride, and 34 Å for the top oxide. The n-type impurity is ion implanted in order to form n+ diffusion layers, after the field oxide is etched by self-align source (SAS). Diffusion layers of the n+ type are used for the common source lines, and the salicide process is implemented in order to reduce the resistance of n+ diffusion layers. A source contact is formed for every 128 memory cells. As a result, the area of the SONOS memory cell is greatly reduced. Electrical characterizations of the NOR-type SONOS array are measured by *HP4155B* semiconductor parameter analyzer connected with high accuracy probe station.

3. RESULTS AND DISCUSSION

A two-bit SONOS NOR architecture with common source line is shown schematically in Fig. 1.

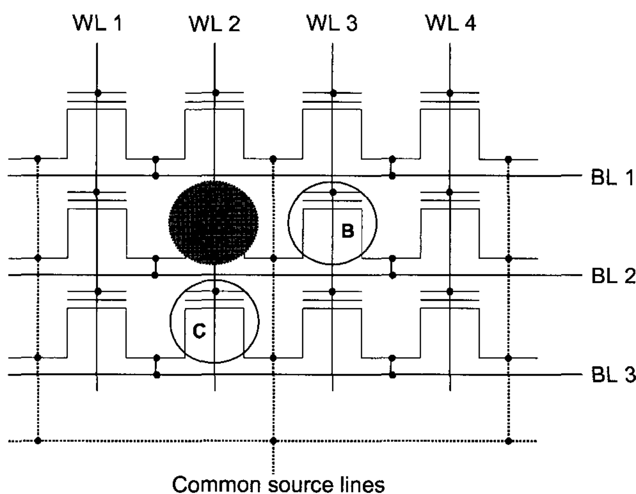

Fig. 1. Equivalent circuit of two-bit SONOS NOR array with common source line.

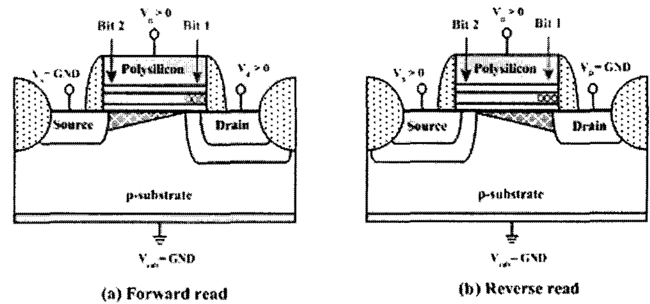

Fig. 2. SONOS cell cross-sections illustrating the two bit operation. Electrons are stored locally in the nitride above drain junction edge by channel hot electron injection: (a) Forward read shows that a read voltage is applied to the same electrode as bit 1, (b) Reverse read shows that a read voltage is applied to bit 2 where electrons are absent.

In this configuration, all sources of the memory cell are connected in common to reduce the memory cell area. In the proposed injection method, 5 V, 3 V, and -2 V bias is applied to the word line 2 (WL 2), the bit line 2 (BL 2), and the substrate of a selected memory cell A, respectively for 500 μs, and the common source is grounded. For the conventional CHE injection, 5 V bias for 500 μs is applied to the both the WL 2 and the BL 2 of the selected cell A, and the common source and the substrate are grounded in the selected cell A.

Figure 2 explains concept of two-bit operation in the SONOS memory cell.

Two read methods are performed for reading change of threshold voltage due to locally stored electrons in bit 1. Those are the forward read and the reverse read. The forward read means that a read voltage is applied to the same electrode as junction stored by electrons as shown in Fig. 2(a). While, the reverse read is performed by interchanging the source and drain terminals. That is, a read voltage is applied to electrode of the converse side where electrons are absent for the reverse read as shown in Fig. 2(b).

Figure 3 illustrates threshold voltage measured by the forward and reverse read as a function of read voltage for comparing the proposed injection method with the conventional injection method.

Threshold voltage of the programmed cell A is nearly constant in the reverse read, while threshold voltage of the programmed cell A is decreased in the forward read with increasing the read voltage as shown in Fig. 3. This data also show that the reverse reading process requires higher threshold voltage than the forward reading process. The reason is that the channel under the trapped charge region can not be inverted due to reverse read voltage.

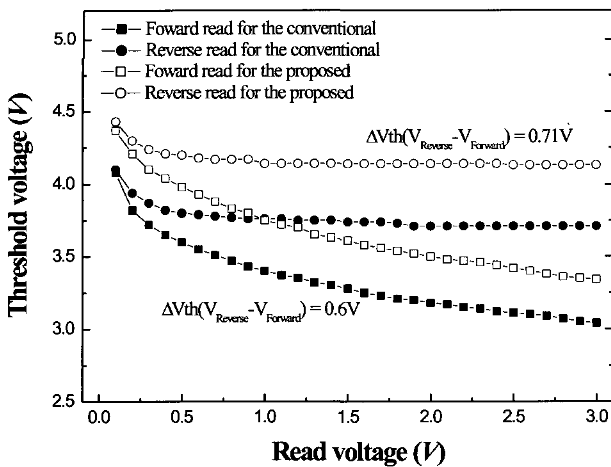

Fig. 3. Threshold voltage measured by the forward and reverse read as a function of read voltage for comparing the proposed injection method with the conventional injection method.

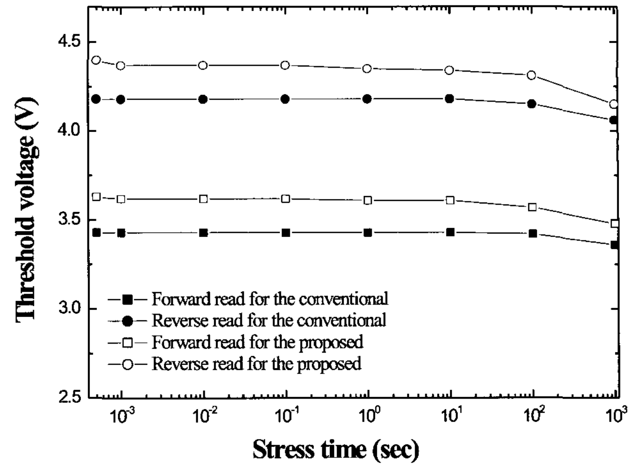

Fig. 5. Gate disturbance characteristics of the unselected cell C with a programmed state that is connected to the same WL 2 as the cell A being programmed.

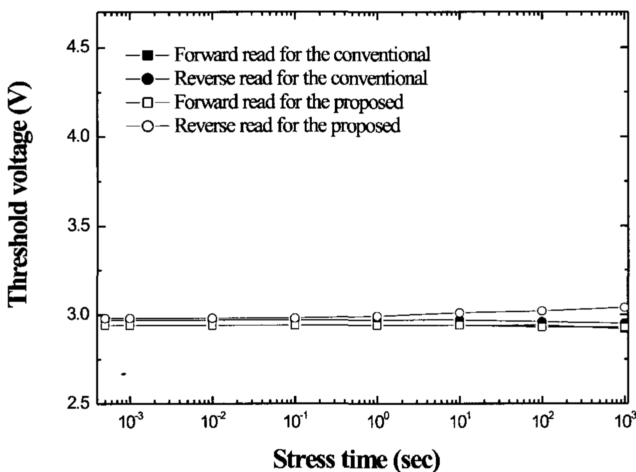

Fig. 4. Gate disturbance characteristics of the unselected cell C with an erased state that is connected to the same WL 2 as the cell A being programmed.

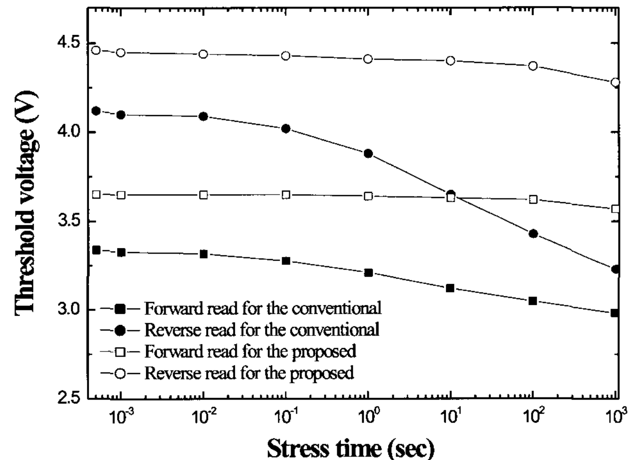

Fig. 6. Drain disturbance characteristics of the unselected programmed cell B.

In Fig. 3, the threshold voltage due to localized trapped charge shows significant difference when applying read voltages larger than 2.5 V. The difference of the threshold voltage is 0.71 V for the proposed programming method, and is 0.6 V for the conventional programming method when read voltage of 2.5 V is applied. The bigger margin of threshold voltage between forward and reverse read is observed in the proposed injection method than the conventional injection method.

Figure 4 shows the gate disturbance characteristics of the unselected cell C with an erased state that is connected to the same WL 2 as the cell A being programmed.

The gate disturbance by the proposed programming method is compared with that by the conventional programming method as a function of stress time applied to the unselected erased cell C. In order to investigate gate disturbance of the unselected erased cell C by both the conventional programming method and the proposed method, program-inhibit voltage of 0 V is applied to the BL 3 of the unselected erased cell C. As Fig. 4 shows, the threshold voltage of the unselected erased cell C is nearly constant for both the forward read and the reverse read even though stress time is increased. It shows the gate disturbance in the unselected erased cell C doesn't occur regardless of the proposed programming method or the conventional method.

Figure 5 shows the gate disturbance characteristics of the unselected cell C with a programmed state that is connected to the same WL 2 as the cell A being programmed.

The same stress as the condition used in Fig. 4 is applied in order to compare the gate disturbance of the unselected programmed cell C by the two programming methods. As Fig. 5 shows, the threshold voltage of the unselected programmed cell C is nearly constant up to stress time of 100 sec for both the forward read and the reverse read even though stress time is increased. It shows the gate disturbance in the unselected programmed cell C doesn't occur regardless of the proposed programming method or the conventional method.

Figure 6 shows drain disturbance characteristics of the unselected cell B with a programmed state.

The drain disturbance comes from the unselected cell B that is on the same BL 2 as the cell A being programmed. The drain disturbance by the proposed programming method is compared with that by the conventional programming method as a function of stress time applied to the unselected cell B. For applying the conventional programming method, program-inhibit voltage of 0 V is applied to the WL 3 of the unselected cell B. The result of Fig. 6 shows that threshold voltage of the unselected cell B with a programmed state is drastically decreased for both the forward read and the reverse read in the conventional programming method. It illustrates that holes at the interface of the drain junction region are created by high drain voltage of 5 V, and then compensate a programmed state of the unselected cell B. It concludes that drain disturbance of the unselected cell B is serious in the conventional method. Program-inhibit voltage of 0 V is applied to the WL 3 of the unselected cell B for using the proposed programming method. As Fig. 6 shows, the threshold voltage of the unselected cell B with a programmed state is nearly constant up to stress time of 100 sec for both the forward read and the reverse read in the proposed programming method. It means that generation of hot hole is drastically decreased at the surface of drain junction region by this method because the electric field between nitride layer and drain region is reduced by decreasing the drain bias. It concludes that the unselected cell B sharing the same BL 2 with the cell A being programmed is free of drain disturbance in the proposed method.

4. CONCLUSION

We have accomplished reliable two-bit SONOS array by employing the efficient bulk-biased programming technique. A bulk bias is additionally applied to the substrate of memory cell for decreasing the electric field between nitride layer and drain region. The SONOS memory cell has shown free of drain disturbance characteristics as the generation of hot hole is drastically decreased at the surface of drain junction region by this proposed programming technique.

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