Integratable Micro-Doherty Transmitter

Jaeho Lee*, Dohyung Kim*, Jinwook Burm*, and Jin Soo Park**

Abstract—**We propose Doherty power amplifier structure which can be integrated in Silicon RF ICs. Doherty power amplifiers are widely used in RF transmitters, because of their high Power Added Efficiency (PAE) and good linearity. In this paper, it is proposed that a method to replace the quarter wavelength coupler with IQ up-conversion mixers to achieve 90 degree phase shift, which allows on-chip Doherty amplifier. This idea is implemented and manufactured in CMOS 5 GHz band direct-conversion RF transmitter. We measured a 3dB improvement output RF power and linearity.**

Index Terms—**RFIC, Power Amplifier, Doherty Amplifier, RF Transmitter**

I. INTRODUCTION

Recently RF applications require a small and low power Si RF ICs. The scaling-down of CMOS makes the power IC design more difficult, because of the large output conductance and low power supply voltage. The low power supply voltage makes the use of a cascode configuration difficult. In addition, it does not allow enough voltage headroom for high power output. This problem would become more serious in RF CMOS front-end stages.

The power amplifier (PA) which delivers a high RF output to antenna is the critical block in RF transmitter front-end. It needs to emit a huge power. But in low power supply voltage system, PA output level is limited. Therefore the high power output technique is needed for low-power supply RF front-end system.

In this paper, we demonstrate a new structure for high P_{1dB} in a transmitter PA. Section 2 addresses the motivation and idea for this structure. Section 3 introduces the constructed schematics. Section 4 and 5 show the simulation and measurement data of the proposed structure. Then conclusions are provided in section 6.

II. MOTIVATION AND IDEA

The Doherty amplifier architecture is a popular topology in RF PAs. It is an enhancement technique for high linearity and good efficiency. Its primary advantages are its: 1) simple circuitry, 2) ease of configuration, and 3) wide bandwidth when compared with other conventional efficiency enhancement techniques such as EER and LINC [1]. Linearity is one of the most important Fig.s of merit for power amplifiers of communication systems [2]. P1dB is a parameter of linearity, which is presented the point that gain is reduced by 1 dB from the linear gain. Recently, CMOS process has been developed by sub-micron technology under 90 nm. The supply voltage level has been reduced simultaneously.

The scale-down of CMOS makes a low P1dB which is dependant on the system supply voltage level. To improve the linearity, output power and the efficiency, a Doherty amplifier will be a good approach. However, generally a Doherty amplifier is implemented on a PCB board rather than on a Si wafer because it needs two 90° ($\lambda/4$) phase shifters for dividing amplification path between a main (or carrier) amplifier and a peaking (or auxiliary) amplifier (Fig. 1). For IC implementation, there are many limits to implement Doherty amplifiers. Above all, the quarter wave length couplers are the most

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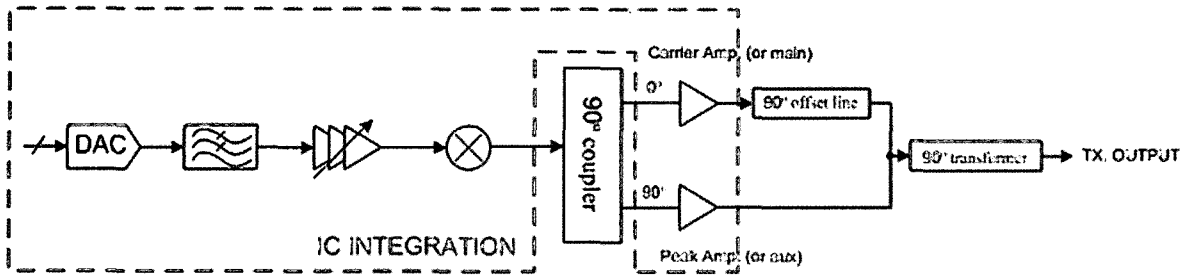


Fig. 1. Conventional transmitter system with Doherty power amplifier.

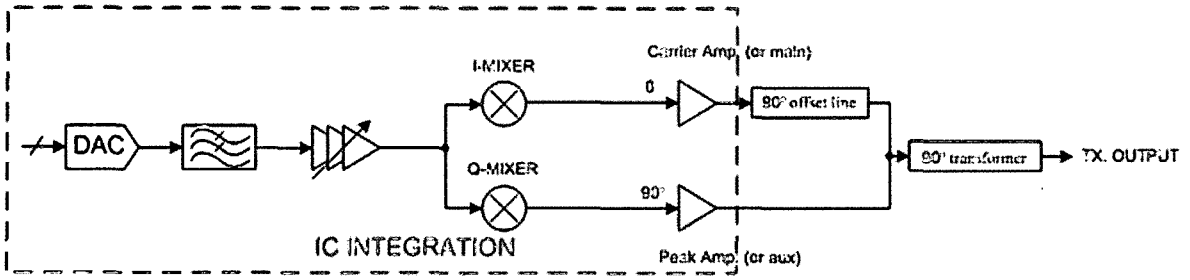
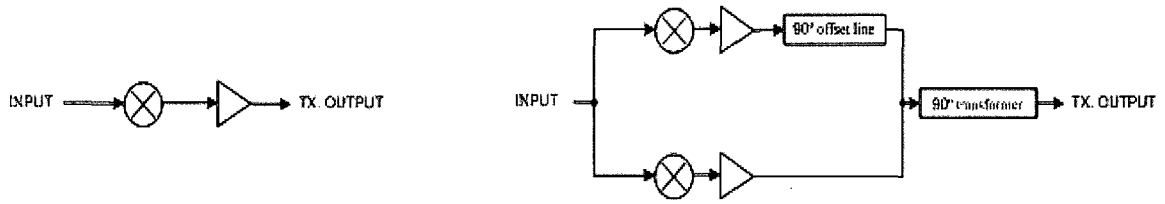


Fig. 2. The proposed transmitter system with Doherty power amplifier architecture.



(a) Single channel (b) Double channel

Fig. 3. (a) Single and (b) Double channel transmitters.

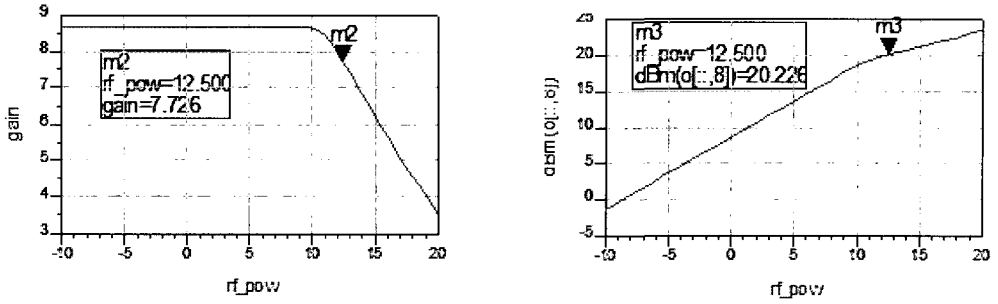
critical problem for an implementation. Usually the quarter wave length coupler is made of transmission lines. The transmission line requires a large space for an RF system under 10 GHz. We propose a new structure to realize a Doherty amplifier on Si wafer.

For a conventional Doherty amplifier two 90° phase shifts are required. In a transmitter circuit, a 90° phase shift can be obtained by mixing with I and Q LO signals. I/Q mixer has 90° phase shift characteristic due to I/Q LO signal. These allow us to eliminate one quarter wave length coupler in the middle of the signal pass. By using this characteristic, the RF direct-conversion transmitter with Doherty power amplifier architecture is able to be implemented as power amplifier. Fig. 2 is the proposed structure for on-chip integration.

The proposed idea still requires an additional quarter wave length coupler at the output. However as it is the last stage of the RF transmitter connected to an antenna, a passive quarter wave length coupler can be easily implemented. In a direct-conversion transmitter system, all blocks are implemented in on-chip so that no off-chip components such as surface acoustic wave (SAW) filter are required.

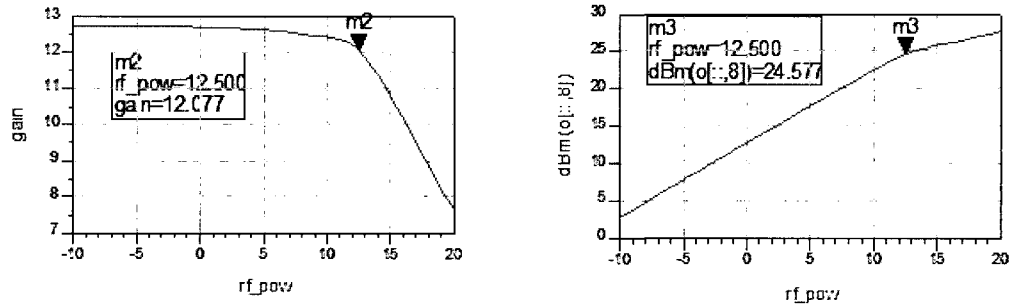
The proposed Doherty power amplifier for on-chip implementation is still greatly beneficial as it eliminated quarter wave length coupler in the middle of the signal pass. Any external component in the middle of the signal pass would bring many drawbacks such as extra power consumption and gain degradation from 50 Ω matching. The proposed method allows making Doherty power amplifiers without external component except at the last stage.

The proposed structure has an additional advantage that enhances output power level inheriting from Doherty structure. If each amplifier of I/Q mixer have same amplifier, total system's input-P1dB is equal. But



(a) Gain versus input power (power in dBm) (b) P1dB of single channel (power in dBm)

Fig. 4. ADS simulation results of single channel (a) gain curve (b) P1dB.



(a) Gain versus input power (power in dBm) (b) P_{1dB} of double channel (power in dBm)

Fig. 5. ADS simulation results of double channel (a) gain curve (b) P1dB.

OP1dB is increased by the power combine.

We certified the theory of Doherty architecture transmitter by ADS circuit simulation using the model of commercially available power amplifiers.

Fig. 3 shows block diagram of each channel for comparison. Fig. 4 and 5 are ADS simulation results of single channel and Doherty structure (double channel). The Doherty structure with double channel has higher gain and OP1dB, but IP1dB is about the same, 12.5 dBm.

III. CONSTRUCTED BLOCKS

I/Q mixer

The proposed structure uses I/Q up-conversion mixers. Mixer structure is independent for proposed structure. It just needs I/Q up-conversion mixing by any topology. Local oscillation (LO) signal also needs a quadrature signal for I/Q mixing.

Amplifiers (Carrier and Peak Amplifiers)

The Doherty amplifier has two separate amplifiers that are the carrier (or main) and peaking (or auxiliary) amplifiers. The carrier amplifier and peaking amplifier operate at different modes. The carrier amplifier operates at class AB mode and the peaking amplifier operates at class C mode.

Extra amplifier enhances total power consumption. However class C amplifier has lower power consumption than other class amplifiers such as class A or class AB. Moreover the peaking amplifier turns on when the input power approaches the main amplifier P_{1dB} level. It makes that total system is able to be affected low by extra amplifier.

Off-chip phase shifter and balun transformer

For power combining each channel signal, balun transformer for differential output of each amplifier and an off-chip phase shifter are required which can be either commercially available products or home-made ones.

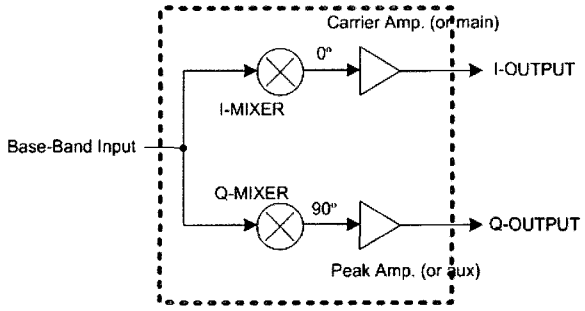


Fig. 6. The implemented I-channel block in IC.

IV. Simulation Results

The proposed transmitter was simulated by Spectre RF by using UMC 0.18 μm RF CMOS process. We try to confirm the difference of 1 dB compression point (P_{1dB}) between single channel and double channel. Fig. 7 and Fig. 8 are single and double channel P_{1dB} result. Double channel (Doherty amplifier) output has same input-referred 1 dB compression point (IP_{1dB}), about 0 dBm, which is about 2.7 dB better output-referred 1 dB compression point (OP_{1dB}) than that of the single channel.

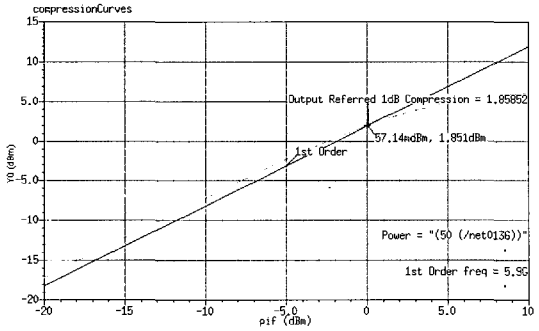


Fig. 7. Single-channel P1dB simulation result.

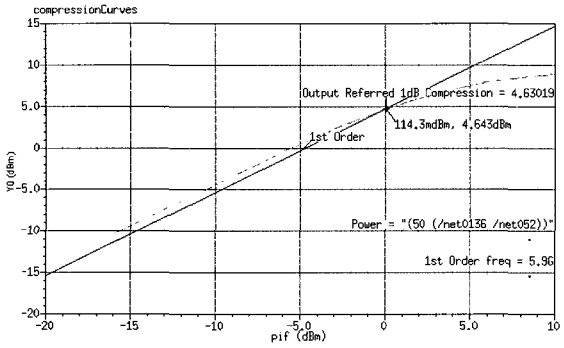


Fig. 8. Double-channel P1dB simulation result.

V. Implementation

This proposed transmitter was fabricated in UMC 0.18 μm RF CMOS 6 metal process. It was implemented with fractional-N Phase Locked Loop (PLL) and sub-harmonic mixer.

Fig. 9 demonstrates the single channel P_{1dB} plot. IP_{1dB} is -1 dBm and OP_{1dB} is -0.15 dBm. Conversion gain is 1.85 dB. Output impedance matching is lower than about -5 dB. The chip-die picture is shown at Fig. 10. And Fig. 11 is the package chip test board. It is 4 layered PCB fabricated by RO4003.

The measurement results which of P_{1dB} and gain are slightly lower than the simulation results about 1 dB. It is due to parasitic component and model mismatch.

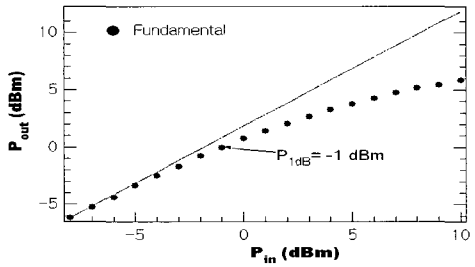


Fig. 9. Single channel P1dB measurement.

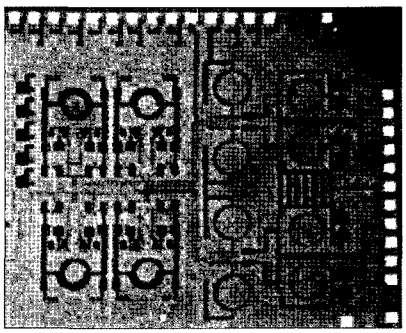


Fig. 10. Chip-die picture.

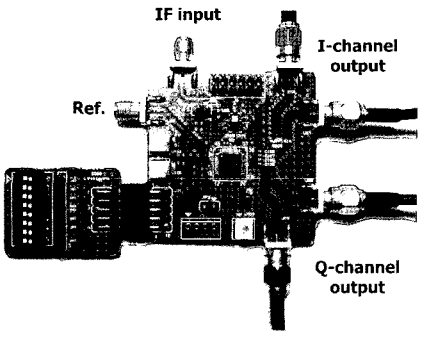


Fig. 11. Test board.

Table 1. The comparison of measurement results between single and double channel.

Property	Single channel results	Double channel results
$OP_{1\text{-}dB}$	-0.15 dBm	2.21 dBm
$IP_{1\text{-}dB}$	-1 dBm	-1.1 dBm
Conversion gain	1.85 dB	4.31 dB
S_{22}	< -5 dB	

VI. CONCLUSIONS

In this paper, the new method to integrate the Doherty amplifier architecture in RF transmitter IC is proposed by using CMOS technology. The Doherty amplifier needs the 90° coupler for using peaking amplifier and combining signals. This difficulty makes hard to integrate in ICs though it has many advantages. By using I/Q mixer, the coupler in front of amplifiers was implemented in IC. This is able to make RF transmitter IC in low price, small size, good linearity and good efficiency. For testing the proposed structure, it is fabricated in UMC 0.18 μm RF CMOS process and measured. The fabricated transmitter consists of I/Q mixer and main/aux. amplifiers.

However this implantation consists of the I-channel stage for simple idea test. Full full stage implementation of Doherty amplifier architecture is perfromed to certify proposed structure for ICs.

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REFERENCES

[1] S. C. Cripps, "RF Power Amplifier for Wireless Communications. Norwood, MA" Artech House, 1999.

[2] Daekyu Yu, "Fully integrated Doherty power amplifiers for 5 GHz Wireless-LANs." *2006 IEEE RFIC symp., Dig.*, pp. 177 – 180, June 2006.

[3] P.B. Kenington, "High-Linearity RF Amplifier Design." Artech House Inc., 2000.

[4] F.H. Raab, "Efficiency of Doherty RF Power Amplifier System," *IEEE Transactions of Broadcasting*, vol. BC-33, no. 3, pp. 77-83, Sep. 1987.

[5] Andrei Grebennikov, "RF and Microwave Power Amplifier Design" McGraw Hill, 2005.

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