Partially-insulated MOSFET (PiFET) and Its Application to DRAM Cell Transistor

Chang Woo Oh, Sung Hwan Kim, Kyoung Hwan Yeo, Sung Min Kim, Min Sang Kim, Jeong-Dong Choe, Dong-Won Kim, and Donggun Park

Abstract—In this article, we evaluated the structural merits and the validity of a partially insulated MOSFET (PiFET) through the fabrication of prototype transistors and an 80 nm 512M DDR DRAM with partially-insulated cell array transistors (PiCATs). The PiFETs showed the outstanding short channel effect immunity and off-current characteristics over the conventional MOSFET, resulting from self-induced halo region, self-limiting S/D shallow junction, and reduced junction area due to PiOX layer formation. The DRAM with PiCATs also showed excellent data retention time. Thus, the PiFET can be a promising alternative for ultimate scaling of planar MOSFET.

***Index Terms*—PiFET, PiCAT, PiOX, DRAM, partial SOI, self-induced halo region, self-limiting shallow junction**

I. INTRODUCTION

In the ultimate scaling region of planar MOSFET, short channel effects (SCEs) seems more and more difficult to be controlled on bulk silicon[1]. As one of alternatives, silicon-on-insulator (SOI) based MOSFETs have emerged as a promising technology to meet these requirements. Despite the merits of SOI devices such as self-limited shallow junction, process simplicity, low power consumption, and fast speed owing to buried oxide (BOX) layer, SOI devices still suffer from low threshold voltage (V_{TH}), floating body, heat dissipation, and back gate interface problems[2-4]. Most of all, the poor V_{TH} controllability should be overcome to implement CMOS logic devices.

As one of the approaches to solve these problems of bulk and SOI MOSFET and to combine their merits, we proposed a modified structure, a partially insulated MOSFET (PiFET) structure having partially insulating oxide (PiOX) layers under source/drain regions. This structure has its own structural advantages such as self-limited shallow source/drain (S/D) junctions and self-induced halo regions. And also, it can give the good SCE immunity comparable to SOI MOSFET and the good V_{TH} controllability comparable to bulk MOSFET without floating body, heat dissipation, and back-gate interface problems.

In consideration of DRAM, as the design rule shrinks, it becomes very difficult to obtain sufficient data retention time. It is basically due to the high channel doping concentration to prevent SCEs with shrinking the feature size. Increased channel doping results in the increase of electric field and leakage current at the junction[5, 6]. Thus, using the PiFETs as DRAM cell transistors, we can achieve good SCE immunity due to self-limited shallow junction, small leakage current due to reduced channel doping, and reduced bit-line/word-line capacitance owing to its structural benefits.

In this work, we evaluate the structural advantages of the PiFET through the 2-D simulation and demonstrate its outstanding performance through the fabrication. As one of PiFET applications, we introduce a partially-insulated cell array transistor (PiCAT) for high-density DRAM products and demonstrate the improved data retention time characteristics.

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II. SIMULATION STUDIES

Transistor schematics in Figure 1 show a PiFET in comparison with the conventional MOSFETs on bulk silicon and SOI. As shown in the figures, the PiFET has self-limited S/D junctions owing to PiOXs and body-tied channel region. For those three types of structures, several simulations using TSUPREM4 and MEDICI were performed in order to investigate the scalability of PiFET and the role of PiOX.

Firstly, the role of PiOX layer was simulated for a bulk MOSFET and PiFETs. After thermal annealing, the PiFET structures showed the self-induced halo region with higher doping concentration near the edges of PiOX layers in Figure 2. It was reasoned that the PiOXs act as diffusion barriers causing the self-limited S/D junctions and the higher channel doping profiles near the edges of PiOX layers. The larger the overlapping between gate and PiOX layers, the higher the doping level near the edges of PiOX layers.

Secondly, the simulations for scalability were performed for transistors with the gate oxide thickness (T_{ox}) of 1.1 nm and the Si body thickness (T_{si}) of 17 nm. From the V_{TH} roll-off characteristics in Figure 3, it was confirmed that the PiFET has better scalability over the bulk MOSFET and much higher V_{TH} over the SOI MOSFET due to its structural merits.

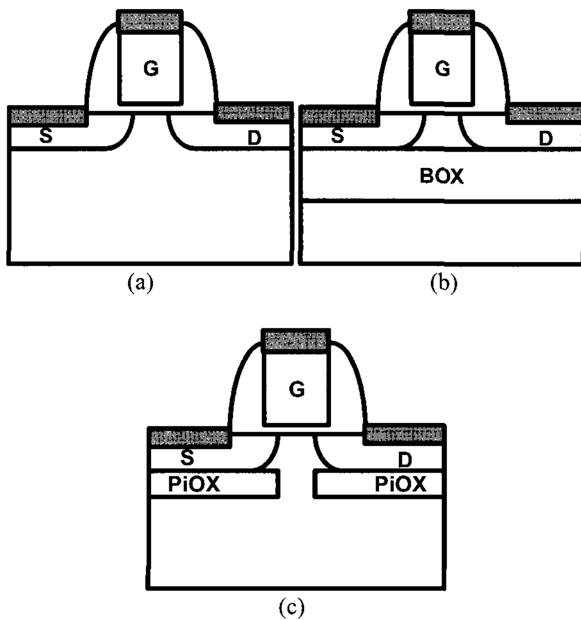


Fig. 1. Transistor schematics; (a) a bulk MOSFET, (b) an SOI MOSFET, and (c) a newly proposed PiFET.

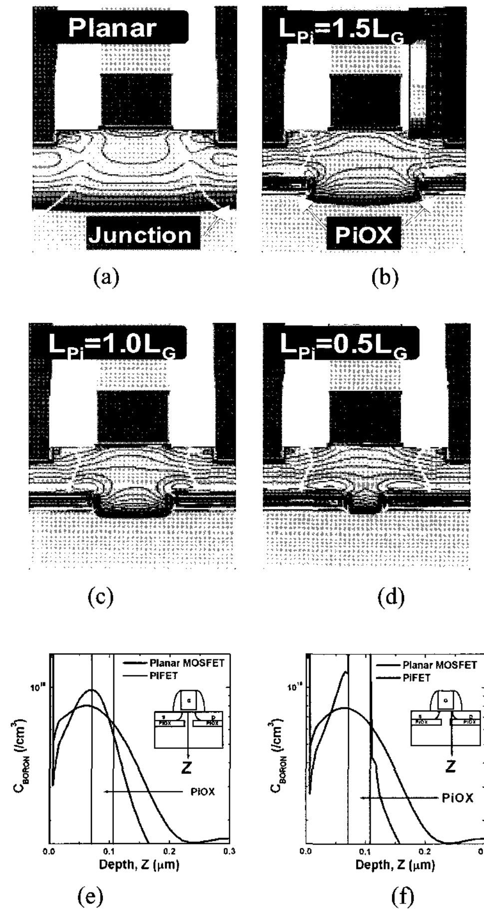


Fig. 2. Simulation results for self-induced halo regions near the edges of PiOX layers; (a) a planar MOSFET and PiFETs with (b) L_{Pi}=1.5L_G, (c) L_{Pi}=L_G (doping profiles in (e), (f)), and (d) L_{Pi}=0.5L_G. The LPi is defined as the spacing between the PiOX layers. From the results, it was confirmed that PiOX layers make self-limited shallow S/D junctions and self-induced halo regions near the edges of PiOX layers during thermal process.

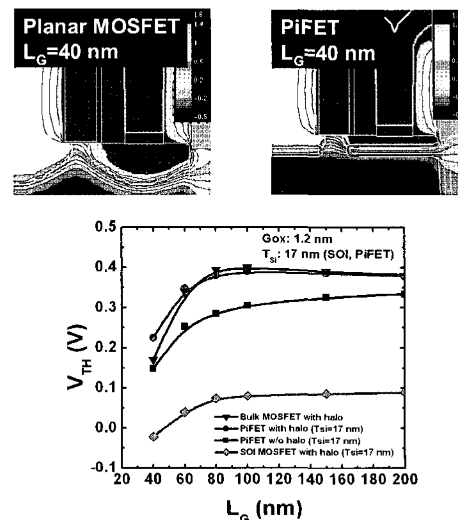


Fig. 3. Simulation results for V_{TH} roll-off characteristics of a bulk MOSFET, an SOI MOSFET, and PiFETs.

III. Device Fabrication

The fabrication process of PiFET is shown in Figure 4 and its process flow is as follows. The epitaxial growth of SiGe and Si layers on Si substrate and the hard mask deposition of SiO_2 and Si_3N_4 layers were firstly performed before the patterning of partially insulating (Pi) layer. The Si/SiGe epitaxial layers were etched out so that the surface of the Si substrate was exposed (Figure 4 (a)). Then, the masking layers were removed by wet etch, followed by the Si epitaxial growth (Figure 4 (b)). For the device isolation and the PiOX layer formation, the conventional shallow trench isolation (STI) process including pad oxide/SiN mask deposition and trench etch was carried out. The SiGe layers were selectively removed using a specially formulated etchant[7]. As a result, the Si epi-layer sustained by epitaxially-grown Si layer on substrate was made on the center of active area (Figure 4 (c)). After the selective removal of SiGe, oxidation and gap-fill process were followed to form the PiOX layers under the S/D region. Finally, the PiFET fabrication was completed by applying the conventional CMOS process (Figure 4 (d)).

The cross-sectional TEM images of the fabricated PiFET are shown in Figure 5. The PiOX layers were formed under source and drain region and the gate was formed on the body-tied region, where no defects were observed owing to the well-optimized pre-cleaning process before the epitaxial growth.

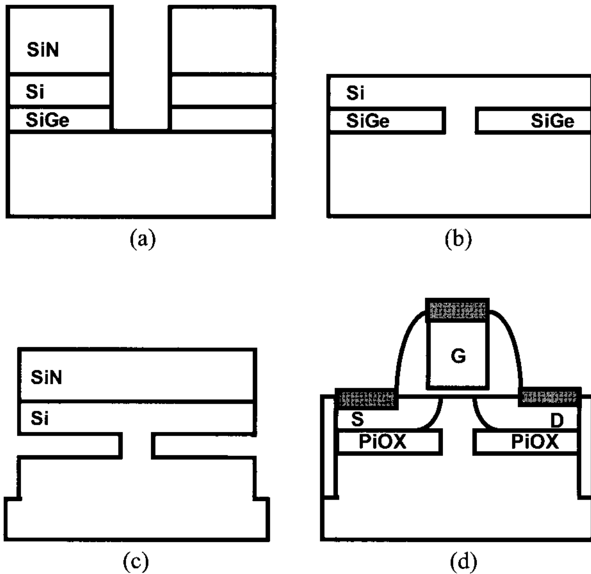


Fig. 4. Process flow of a PiFET; (a) partially insulating (Pi) layer patterning and etch with mask layers, (b) epitaxial growth of Si layer after stripping masking layers, (c) trench etch with active mask layers and SiGe removal, and (d) a completed PiFET after the conventional CMOS process including STI process.

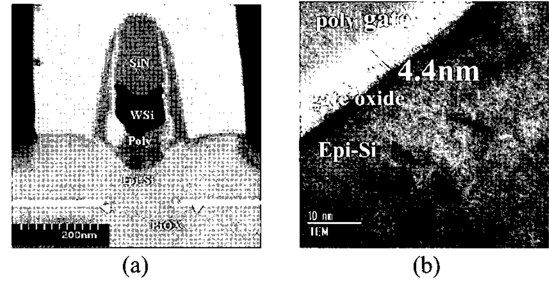


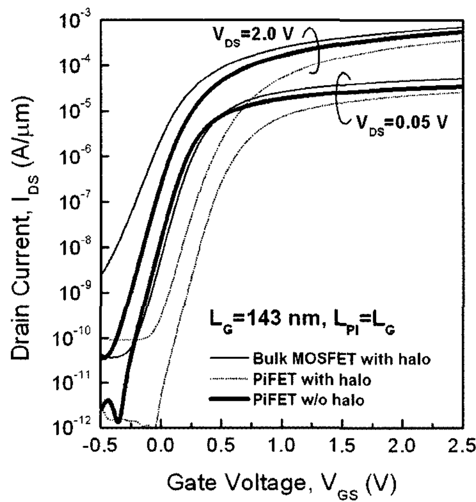
Fig. 5. Cross-sectional views of a newly fabricated PiFET. (a) The PiOX layers were formed under the source and drain region, while gate was formed on the body-tied region. (b) Lattice image shows epitaxially grown Si under the 4.4 nm-thick gate oxide.

IV. Electrical Characteristics

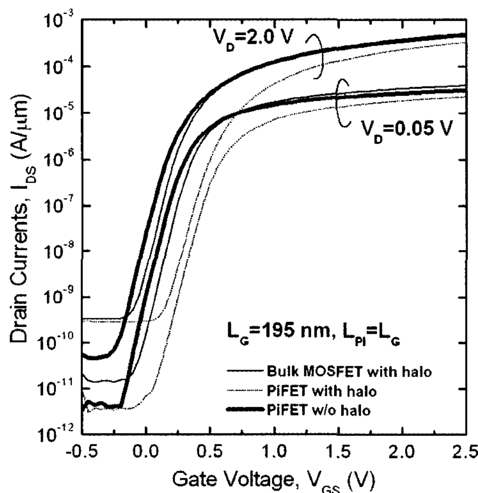
To evaluate the V_{TH} controllability and the scalability of the fabricated PiFETs, the electrical characteristics of the bulk MOSFETs and the PiFETs for various gate lengths and L_{Pi}, the spacing between the PiOXs, were measured by using parameter analyzer, HP4156. The I_{DS}-V_{GS} characteristics of the fabricated bulk MOSFETs and PiFETs with L_G =143 nm and L_{Pi}=L_G, L_G =195 nm and L_{Pi}=L_G, and L_G =152 nm and L_{Pi}=0.5L_G are shown in Figure 6 and their key parameters are summarized in Table 1. According to the results, as the gate length is smaller and the L_{Pi} is narrower, short channel effects are effectively suppressed and threshold voltages are dramatically increased in PiFETs with halo. And also, the PiFETs even without halo scheme have better SCE immunity than the bulk MOSFET and the lowest junction leakage currents among them. But, considering the V_{TH} decrease due to the buried oxide layer in SOI MOSFET, these results may appear to be strange. Even though the V_{TH} controllability of the PiFETs comparable to that of bulk MOSFET is considered, much higher V_{TH} cannot be explained. However, if higher doping concentration near PiOX layers as shown in simulation results is considered, these phenomena can be well explained as the effects of self-induced halo regions generated during PiOX layer formation and subsequent thermal process, as well as self-limited shallow S/D

Table 1. The key electrical parameters of bulk MOSFETs and PiFETs for gate length and L_{Pi}.

		Bulk MOSFET	PiFET with halo	PiFET w/o halo
L_G=143 nm L_{Pi}=L_G	V_{TH}	0.26	0.62	0.22
	DIBL (mV/V)	174	72	69
	Swing (mV/dec.)	104	97	97
L_G=195 nm L_{Pi}=L_G	V_{TH}	0.36	0.58	0.31
	DIBL (mV/V)	61	31	65
	Swing (mV/dec.)	84	88	86
L_G=252 nm L_{Pi}=0.5L_G	V_{TH}	0.29	0.65	0.45
	DIBL (mV/V)	26	16	29
	Swing (mV/dec.)	77	96	84



(a)



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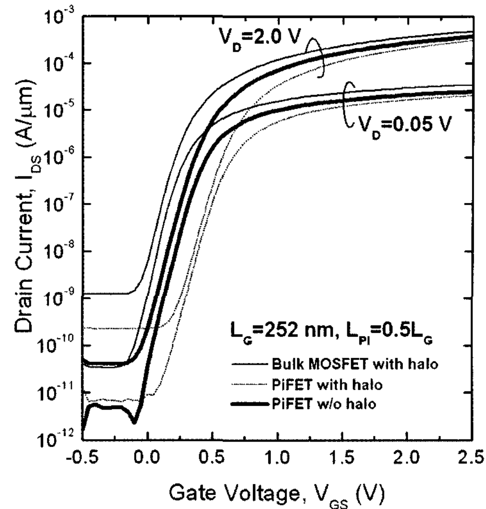

(c)

Fig. 6. I_{DS}-V_{GS} characteristics of bulk MOSFETs and PiFETs with (a) L_G=143 nm and L_{Pi}=L_G, (b) L_G=195 nm and L_{Pi}=L_G, and (c) L_G=252 nm and L_{Pi}=0.5L_G. As the gate length decreases and the L_{Pi} decreases, short channel effect is effectively suppressed and V_{TH} is largely increased. These phenomena can be well explained as the effects of self-induced halo regions due to PiOX layers.

junction. For better understanding, body-bias effects were measured for the bulk MOSFET and the PiFETs with L_G=195 nm and L_{Pi}=L_G. The PiFETs, sustaining low off-currents, have large body bias dependency resulting from increased channel doping due to PiOXs in comparison with the bulk MOSFET. This result can become another proof for self-induced halo regions due to PiOX layers. Figure 8 shows V_{TH} roll-off characteristics of the bulk MOSFET and the PiFETs with L_{Pi}=L_G. The PiFET without halo implantation shows good roll-off characteristics comparable to that of bulk MOSFET with halo implantation. In the I_{DS}-V_{DS} charac-teristics in Figure 9, the PiFET shows the slightly low saturation current of 554 μA/μm, while the bulk MOSFET, having lower threshold voltage, shows the slightly high saturation current of 720 μA/μm. However, the PiFET has much more stable on-currents in saturation regions, giving higher output impedances. Therefore, these superior short channel effect (SCE) immunity and off-current characteristics of the PiFETs mainly resulted from its own structural advantages such as self-induced halo region, the self-limiting S/D shallow junction, and the reduced junction area due to PiOX layer formation.

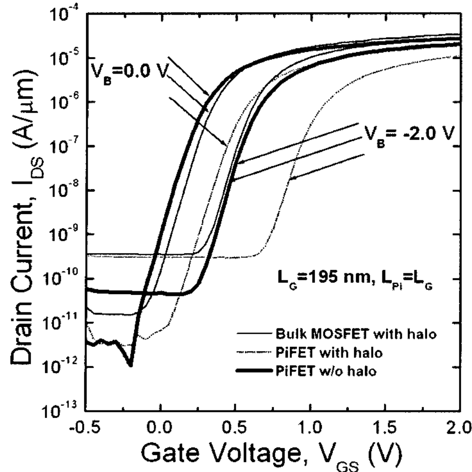

Fig. 7. Body-bias effects of bulk MOSFET and PiFETs with L_G =195 nm and L_{Pi}=L_G. The PiFETs have large body bias dependency. This result can be another proof of self-induced halo regions due to PiOX layers.

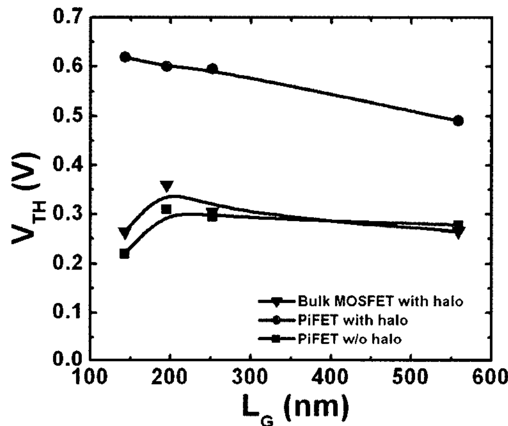

Fig. 8. V_{TH} roll-off characteristics of a bulk MOSFET and PiFETs with L_{Pi}=L_G. The PiFET without halo implantation scheme show good roll-off characteristics comparable to that of bulk MOSFET with halo implantation.

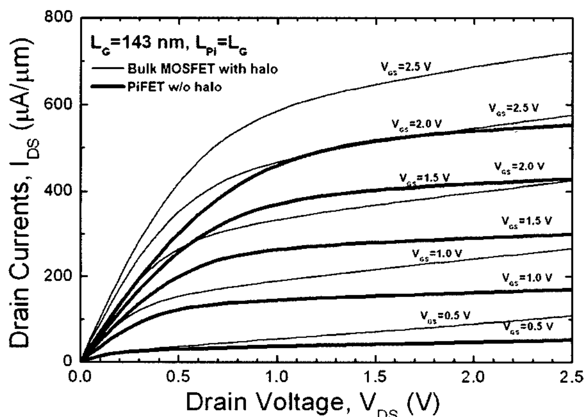

Fig. 9. I_{DS}-V_{DS} characteristics of a bulk MOSFET and a PiFET with L_G =143 nm and L_{Pi}=L_G. The PiFET shows more stable currents in saturation regions, meaning higher output impedances.

V. Partially-insulated Cell Array Transistor (PiCAT) For Dram Application

To show the merit of PiFET, low junction leakage current, we fabricated a 512M DDR DRAM with partially-insulated cell array transistors (PiCAT). Cell array transistors are made on the partially insulated structure, while peripheral and core transistors are made on epi-Si. Therefore, the peripheral circuit operation is maintained as the conventional DRAM.

The cross-sectional SEM picture of fully integrated 512M DRAM is shown in Figure 10. The close views of the PiCAT with 80 nm technology are shown in Figure 11. The channel regions were flattened by optimizing 2nd epi-Si growth process. The PiCAT is formed on the 50 nm-thick Si and 46 nm-thick PiOX. The silicon body thickness is controllable by epi-Si growth process.

The I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics of PiCAT are shown in Figure 12. In spite of using low channel doping, PiCAT shows the lower DIBL characteristic than the conventional cell transistor. This improved SCE immunity is due to the retardation of dopant diffusion in the channel and the self-limited shallow junction in the source/drain by PiOX. The evaluation of cell junction leakage current using defect array test pattern shows that the cell junction leakage current of PiCAT is 30 % lower than that of the conventional cell array transistor (Figure 13). Low junction leakage current results from the self-limiting shallow junction and reduced junction area. Owing to these excellent cell array transistor characteristics of PiCAT, the data retention time is enhanced, compared to the DRAM with the conventional cell array transistor (Figure 14). The distributions of bit line/word line capacitances are compared in Figure 15. Because of the PiOX layers under B/L contact, smaller bit-line/word-line capacitances could be obtained than the conventional cell array transistor by 14 % and 7 %, respectively.

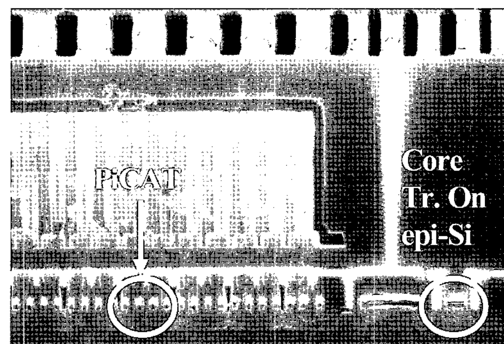

Fig. 10. Vertical structure of a fully integrated 512M DRAM with PiCAT using 80 nm process technology.

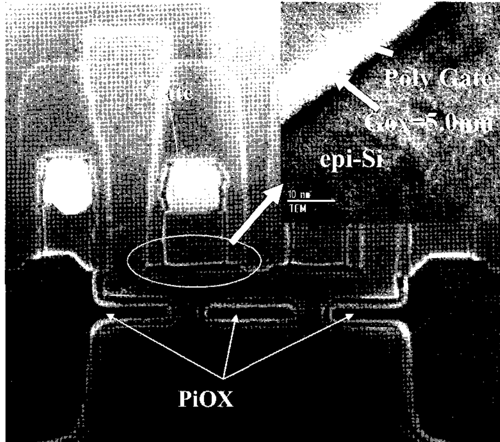

Fig. 11. SEM and TEM images of Pi cell transistor after full process. PiOXs are located under source and drain. The thickness of gate oxide is 5.0 nm.

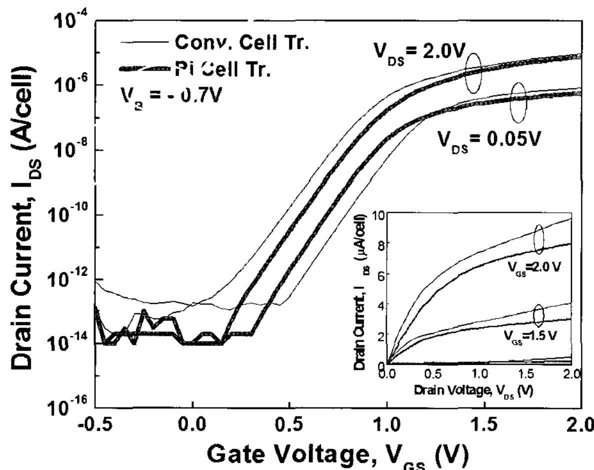

Fig. 12. I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics of cell transistor. PiCAT with low dose implantation shows smaller DIBL and lower junction leakage current than the conventional cell array transistor. PiCAT shows slightly lower cell current due to high threshold voltage with smaller DIBL.

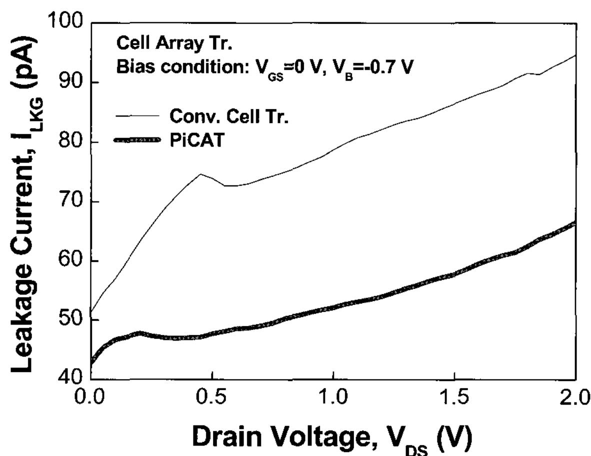

Fig. 13. Junction leakage current of PiCAT is reduced by 30 %.

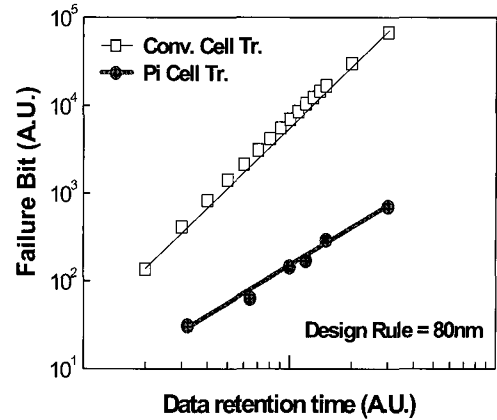

Fig. 14. Data retention time of 80 nm 512M DRAM with PiCAT comparing with conventional cell array transistor. The newly fabricated DRAM shows superior data retention time to the conventional one due to low junction leakage.

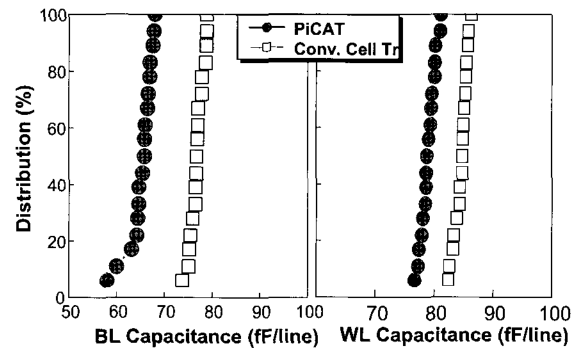

Fig. 15. Bit-line/word-line capacitances of PiCAT are reduced due to the PiOX structure.

VI. SUMMARY

We investigated the effects of PiOX layer through the simulation and evaluated the SCE immunity and the V_{TH} controllability through the characterization. The PiFETs showed good off-current characteristics in the subthreshold region, good SCE immunity in the linear region, and good output impedance in the saturation region over conventional one. These good performances mainly resulted from self-induced halo region, self-limiting S/D shallow junction, and reduced junction area due to PiOX layer formation. From the fabrication of an 80 nm 512M DRAM with PiCAT, its manufacturability was confirmed and its better SCE immunity was reconfirmed. Thus, the PiFET structure is believed to be one of the most promising candidates as a low power and high performance transistor in the ultimate scaling region of planar MOSFET.

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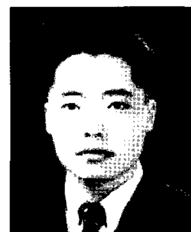

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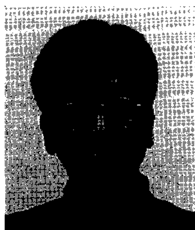

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