Schottky Barrier MOSFETs with High Current Drivability for Nano-regime Applications

Moongyu Jang*, Yarkyeon Kim*, Myungsim Jun*, Cheljong Choi*, Taeyoub Kim*, Byoungchul Park, and Seongjae Lee***

Abstract—**Various sizes of erbium/platinum silicided *n/p*-type Schottky barrier metal-oxide-semiconductor field effect transistors (SB-MOSFETs) are manufactured from 20μm to 10nm. The manufactured SB-MOSFETs show excellent DIBL and subthreshold swing characteristics due to the existence of Schottky barrier between source and channel. It is found that the minimization of trap density between silicide and silicon interface and the reduction of the underlap resistance are the key factors for the improvement of short channel characteristics. The manufactured 10 nm *n*-type SB-MOSFET showed 550μA/um saturation current at V_{GS}-V_T = V_{DS} = 2V condition (T_{ox} = 5nm) with excellent short channel characteristics, which is the highest current level compared with reported data.**

Index Terms—**SB-MOSFETs, scaling, nanotechnology, high performance**

I. INTRODUCTION

Recently, silicide metallic junction-based electronic devices are being studied for the applications in nanometer regime as an alternative of conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) [1-3]. In Schottky barrier MOSFETs (SB-MOSFETs), the source and drain are composed of silicide instead of impurity doped silicon. Thus, the parasitic source and drain resistance can be efficiently reduced and the process temperature can be reduced dramatically (lower than 600 ℃), giving the opportunity to use metal as gate electrode and high-K dielectric materials as gate insulator [1]. In SB-MOSFETs, most of the works are done in *p*-type transistors, using platinum-silicide because of its low Schottky barrier height (0.24 eV) for hole [2]. Recently, erbium-silicide is being considered as the candidate for the *n*-type SB-MOSFETs [2, 3]. The previous works reported the superior scaling characteristics of SB-MOSFETs in deep nano regime. However, the major drawback was the low current drivability in *n*-type SB-MOSFETs due to the high Schottky barrier height. The reported maximum saturation current was around 200 μA/um, which is too low compared with conventional MOSFETs [2, 3].

In this paper, various sizes of SB-MOSFETs are manufactured down to 10nm with 550μA/um saturation current at V_{GS}-V_T = V_{DS} = 2 V condition (T_{ox} = 5 nm). Also, the short channel characteristics of SB-MOSFETs are analyzed using DIBL and SS characteristics to check the scalability.

II. EXPERIMENTAL

As a starting material, (100) *n*-type and *p*-type silicon-on-insulator (SOI) wafers are used for the *n*-type and *p*-type SB-MOSFETs, respectively. SOI wafers are phosphorus and boron doped with a resistivity of 13.5-22.5 Ω·cm. The thickness of the SOI and buried oxide (BOX) layer is 100 nm and 200 nm, respectively. The gate oxide is 5 nm thick SiO_2, grown by thermal oxidation and the gate electrode is highly phosphorus doped *n*-type polycrystalline silicon. Electron-beam

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lithography is employed to define gate pattern. After gate etching, 30nm thick gate sidewall spacer is formed by using thermal oxidation method. After blanket dry etching of gate sidewall spacer the remained spacer thickness is around 15 nm. After sidewall etching, 100 nm thick erbium and platinum are sputtered for *n*-type and *p*-type SB-MOSFETs, respectively. Erbium-silicide and platinum-silicide are formed by using rapid thermal annealing (RTA) technique. Annealing temperature and time is 500 ℃ and 5 min, respectively. The non-reacted erbium and platinum are removed by using SPM and aqua regia for 10 min, respectively. The detailed SB-MOSFETs manufacturing procedures are summarized in Table 1. The formation of $ErSi_{1.7}$ and PtSi phase are confirmed by x-ray diffraction (XRD) and Auger electron spectroscopy (AES) analysis. The sheet resistance are less than 30 Ω/□ and 10 Ω/□ for erbium-silicide and platinum-silicide, respectively, even if the line width is less than 100 nm. Thus, erbium and platinum are applicable in sub-100 nm regime SB-MOSFETs manufacturing.

Table 1. Fabrication procedure of SB-MOSFETs

	Fabrication procedure
1	Cleaning of (100) SOI wafer (N_{SUB} = 10^{15} cm^{-3} for *n/p*-type substrate)
2	Active lithography (e-beam) and dry etching
3	PR strip, gate oxidation (T_{OX}= 5 nm) and n^+ polysilicon deposition.
4	Gate lithography (e-beam), dry etching and PR strip
5	Sidewall spacer oxidation (T_{SP}= 15 nm) and blanket etching
6	Erbium/Platinum deposition
7	Annealing (500℃, 10 min) and removal of erbium/ platinum

III. Results and Discussions

Erbium and platinum are chosen as source/drain metal of *n/p*-type SB-MOSFETs, because of its low Schottky barrier height for electrons and holes, respectively. Figure 1 shows the scanning electron microscopy (SEM) and transmission electron microscopy (TEM) of finally manufactured 10 nm-gate-length *n*-type SB-MOSFET. The uniform growth of $ErSi_{1.7}$ on the 20 nm width active region is shown in the SEM image. Also, from the TEM image, the gate length is 10 nm with the 15nm thick SiO_2 sidewall spacer. Figure 2 shows the diode characteristics of $ErSi_{1.7}$ on *p*-substrate and PtSi on *n*-substrate, respectively. N_2 annealing was a very efficient method to remove the interface trap existing between silicide and silicon, thus improving diode *I-V* characteristics [4]. After N_2 annealing, Schottky barrier height of $ErSi_{1.7}$ for hole is 0.77eV and PtSi for electron is 0.87eV which corresponds to 0.36eV for electron and 0.25eV for hole, respectively. Figure 3 shows I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics of the 20 μm long channel *n/p*-type SB-MOSFETs. The gate oxide and spacer thickness is 5 nm and 15 nm, respectively. Both the *n/p*-type SB-MOSFETs show high on/off current ratio, larger than $I_{on}/I_{off}>10^5$ with low leakage current (I_{LKG}<100 pA/㎛). The on/off ratio and the leakage current level is the highest and lowest values compared with previously published data in SB-MOSFETs [2]. Also, DIBL is almost suppressed in both *n/p*-type SB-MOSFETs and the SS value is 60 mV/decade both in *n*-type & *p*-type SB-MOSFETs, reaching the theoretical limit vsalue in MOSFETs.

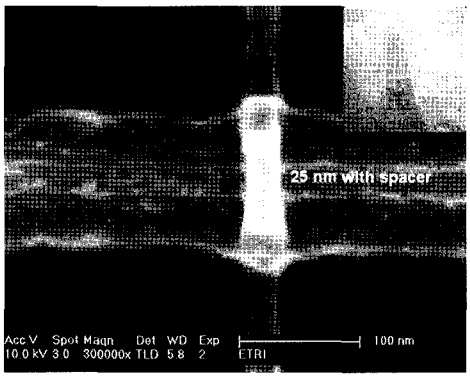

Fig. 1. SEM and TEM (inset) image of the 10 nm erbium-silicided *n*-type SB-MOSFET

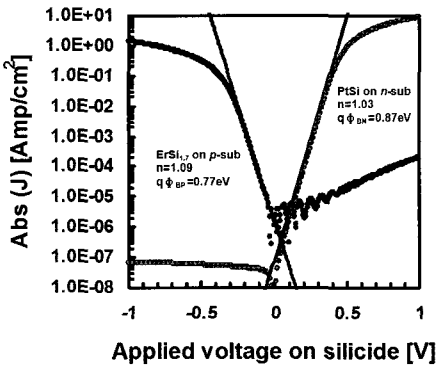

Fig. 2. Schottky diode I-V characteristics.

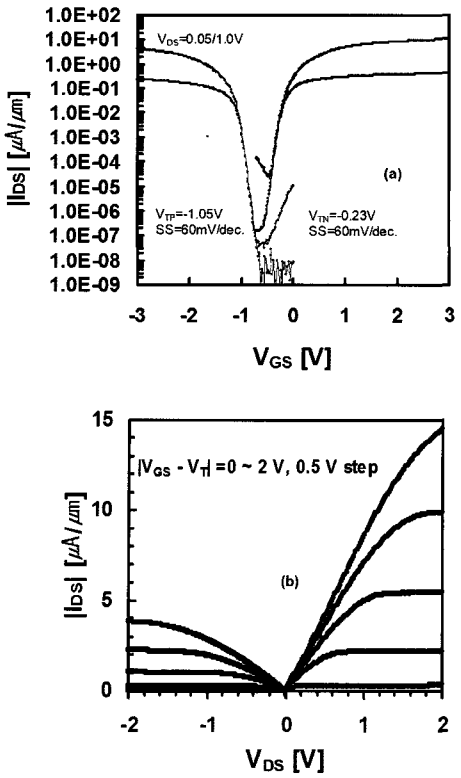

Fig. 3. I_{DS}-V_{GS} (a) and I_{DS}-V_{DS} (b) characteristics of 20㎛ long channel *n/p*-type SB-MOSFET.

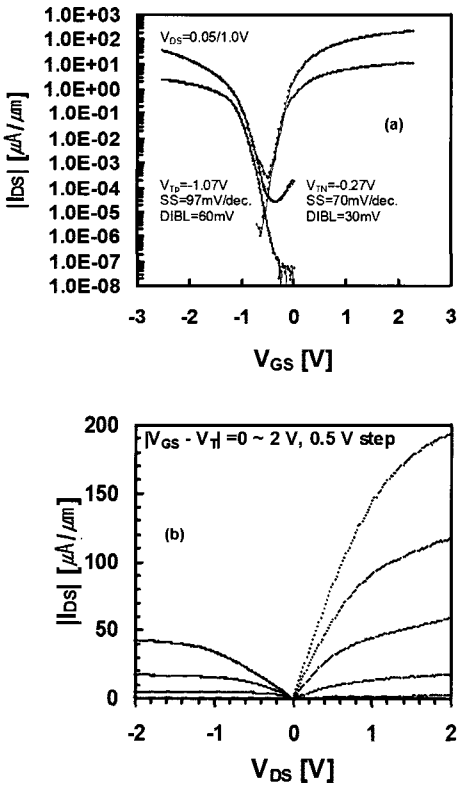

Fig. 4. I_{DS}-V_{GS} (a) and I_{DS}-V_{DS} (b) characteristics of 100 nm gate length *n/p*-type SB-MOSFET.

Figure 4 shows the I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics of 100 nm gate length *n/p*-type SB-MOSFETs. Also, this 100nm gate length *n*-type SB-MOSFET shows excellent short channel characteristics. The measured SS and DIBL values are 70mV/decade and 30mV, respectively.

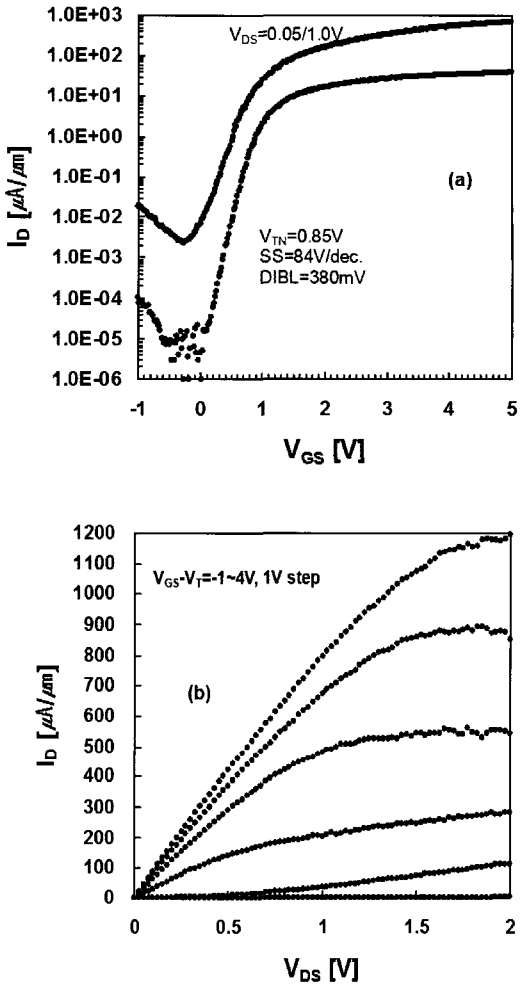

Fig. 5. I_{DS}-V_{GS} (a) and I_{DS}-V_{DS} (b) characteristics of 10 nm *n*-type SB-MOSFET.

Figure 5 shows the I_{DS}-V_{GS} characteristics of 10 nm gate length *n*-type SB-MOSFETs manufactured on *n*-type substrate. Although the substrate doping concentration is $10^{15}cm^{-3}$, short channel effect is sufficiently suppressed due to the existence of Schottky barrier between source and channel. The saturation current measured at V_{GS}-V_T=V_{DS}=2V is 550 μA/μm (T_{ox}= 5 nm). This is the highest saturation current value compared with the reported data. The major reason for the increase of saturation current is due to the reduction of underlap resistance by changing substrate type from *p* to *n*-type.

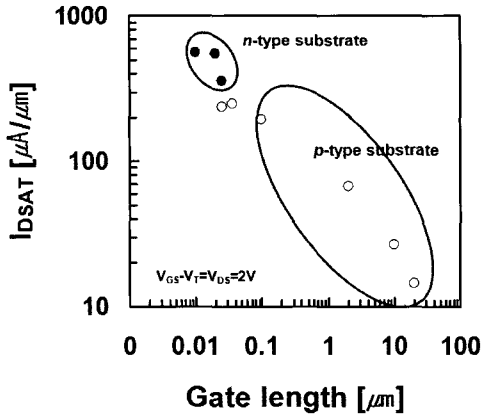

Fig. 6. Variation of saturation current with gate length.

Figure 6 shows the variation of saturation current with the gate length in *n*-type SB-MOSFETs. As the gate length decreases, saturation current increases. But the saturation current is clamped around 250 μA/μm if the used substrate is *p*-type (open circle). By changing the substrate type from *p* to *n*, the saturation current gradually increases up to 550μA/μm (closed circle). The major reason for the increase of saturation current is the reduction of parasitic underlap resistance.

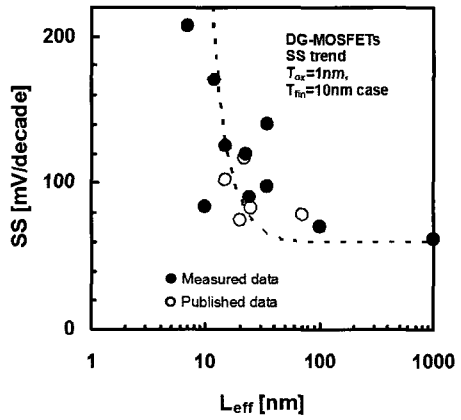

Fig. 7. Subthreshold swing (SS) characteristics. Scaling theory is applied for the evaluation of SS.

Figure 7 shows the SS characteristics of SB-MOSFETs with the variation of gate length. In Figure 7, dotted line represents theoretical DIBL characteristics of DG-MOSFETs. The scaling theory of DG-MOSFETs can be found in [5]. In the calculations of SS in DG-MOSFETs, gate oxide and fin thickness are assumed as 1 nm and 10 nm, respectively. Note that these assumed values correspond to the ultimate minimum values in device technology. The SS characteristics of SB-MOSFETs are better than the ultimate limit characteristics of DG-MOSFETs. The reason for this is due to the existence of the Schottky barrier between source and channel. In MOSFETs and DG-MOSFETs, the subthreshold characteristics, including DIBL and SS, are mainly determined by the built-in potential. In short channel device, as the drain voltage increases, built-in potential between source and channel decreases, giving DIBL effect. But in SB-MOSFETs, the subthreshold characteristics are mainly determined by the Schottky barrier.

IV. Conclusions

In conclusion, various sizes of erbium/platinum silicided *n/p*-type SB-MOSFETs are manufactured from 20 μm to 10 nm. The manufactured SB-MOSFETs show excellent DIBL and subthreshold swing characteristics due to the existence of Schottky barrier between source and channel. It is found that the minimization of trap density between silicide and silicon interface and the reduction of the underlap resistance are the key factors for the improvement of short channel characteristics. The manufactured 10 nm *n*-type SB-MOSFET showed 550 μA/μm saturation current at V_{GS}–V_T = V_{DS} = 2V condition (T_{ox} = 5nm) with excellent short channel characteristics, which is the highest current level compared with reported data.

In SB-MOSFETs, SS characteristics of SB-MOSFETs are better than the ultimately scaled DG-MOSFETs, which show the possible application of SB-MOSFETs in nanoscale regime as an alternative to the MOSFETs.

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