Journal of the Korea Institute of Applied Superconductivity and Cryogenics
Vol.8, No.2, (2006), pp.17~19

A GHz-Level RSFQ Clock Distribution Technique with Bias Current Control in JTLs

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Abstract-- **A novel clock distribution technique for pipelined-RSFQ logics using variable Bias Currents of JTLs as delay-medium is newly proposed. RSFQ logics consist of several logic gates or blocks connected in a pipeline structure. And each block has variable delay difference. In the structure, this clock distribution method generates a set of clock signals for each logic blocks with suitable corresponding delays. These delays, in the order of few to tens of pS, can be adjusted through controlling bias current of JTL of delay medium. While delays with resistor value and JJ size are fixed at fabrication stage, delay through bias current can be controlled externally, and thus, is heavily investigated for its range as well as correct operation within current margin. Possible ways of a standard delay library with modular structure are sought for further modularizing Pipelined-RSFQ applications. Simulations and verifications are done through WRSpice with Hypres 3-um process parameters.**

1. INTRODUCTION

Rapid Single-Flux-Quantum(RSFQ) or SFQ superconductive logic circuits have been drawing attentions for a possible realization of a few hundred GHz range superconductive digital circuits and system [1][2]. It has many difficult problems to design superconductive systems or integrated circuits with SFQ or RSFQ system which is operating in the range of a hundred GHz. One of these problems is global clock distribution because clock speed is too fast for applying digital device in RSFQ or SFQ. For solving these problems, new clock distribution techniques are required. A new clock distribution technique can control whole system or IC blocks effectively and ensure its operation speed. Serious works were done for this ultra-high speed RSFQ clock distribution so far, based on self-aligned and GALS (Globally Asynchronous Locally synchronous system) idea [3-5]. For synchronization in order of tera-hertz, a new clock distribution technique which exactly generates and controls delay within range of few pS is needed. In the proposed clock distribution technique, new clock distribution net is constructed with only Josephson Transmission Lines (JTLs). This technique has some guarantee such as small chip size and simple structure which doesn't require any other circuits. Only JTLs that are used as delay control units are parallel connected with a pipelined RSFQ logic data path. These delays are generated from a few to tens of pS in time and previously investigated through [6] [7].

The concepts and techniques relating to variable delay control from fixed clock pulse frequency are described in section II. Section III discusses the issues related to pipelined-structure. And final section discusses results of simulation circuit. The circuit simulation is done and verified through the WRspice.

2. DELAY CONTROL UNIT

Fig. 1 shows JTL structure as a delay control unit for variable delay by controlling bias current. It is named delay-media. A delay-media generates delay between input pulse and out pulse in the order of a few to tens of pS. To realize effect by adjustment of bias current, suppose other parameters such as resistance, inductance and junction size are fixed. In ideal case, it is able to suppose that clock pulse line has no jitter by supply and signal paths. A set of output pulse is generated at the absolute point in time where we want to be. But in most case of RSFQ logic has pulse with jitter. However if the range of delay variation by controlling bias current is very narrow, exemplary close to few pS, it could be recognized at each other times as several pulses with different delays.

Typically jitter range in RSFQ logic is close to a few pS. Therefore the delay-media must be able to control delay at least more a ten pS. And also inherently the smaller current generates more delay. As a result, it is required as possible as least current for the most delay. But JTLs must still be in operation range. Bias current margin are determined by this value. Table I shows current and average delays in a single clock line which is constructed by six serially connected JTLs with equal bias currents. Delays through JTLs don't have absolute value by changing current. However, if clock

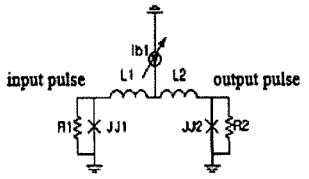

Fig. 1. JTL for variable delay by controlling bias current.

TABLE I
AVERAGE DELAY OF JTLS BY ADJUSTING BIAS CURRENT

Bias current (mA)	Average Delay of a JTL in 5 X JTLs (pS)
0.35	9.5
0.30	11.3
0.25	14.5
0.20	29.1

line includes jitter or not, delay can be recognized in time domain, because variation ranges of delay are very narrow. In these case, current margin are approximately 0.35 ~ 0.20 mA and range of delay 10 ~ 30 pS with 10 GHz clock frequency. Delay variation is maximum 1.83 pS from average delay. More exact measurement is discussed in the next section.

3. PIPELINED-RSFQ LOGIC STRUCTURE

Fig. 2 shows block diagram of pipelined-RSFQ sequential logic structure with Clock Distribution Net (CDN). Pipelined-RSFQ logic is constructed by several clock lines which are serial connection of JTLs with controllable bias current. By fixed bias current, clock line supplies clock pulse to its bottom sequential logics at user defined time point. Each clock lines can have many different sequential logics in realization. However, it is only used D-Flip-Flops in the simulation for simplicity. Considering whole system, the unique clock pulse is distributed from CDN to several clock lines. Each clock line has different delay by fixed bias current. Therefore it is possible that sequential logics of each clock lines can be controlled synchronously at adjustable clock time.

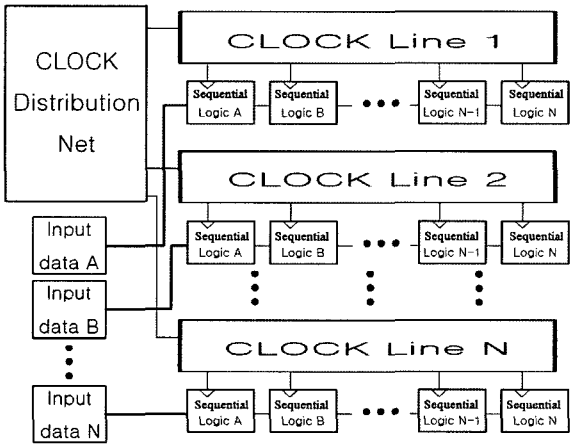

Fig. 2. Block diagram of Pipelined-RSFQ Logic.

Fig. 3 shows block diagram of clock line structure in the pipelined-SFQ sequential logic. The clock pulse goes through delay medium with a certain delay. And the data input pulse passes through sequential blocks. Data inputs of D Flip-Flops can be same or not. It also can be connected serial or parallel inputs and be connected other Flip-Flop outputs. It is determined by design of circuit. The important issue is that how exactly clock pulse can input, because these outputs of sequential logic are synchronized in clock pulse. So to terminate issues which interrupt right follow of clock pulse, CDN is designed carefully in the layout. Fig. 4 shows basic idea structure of CDN. This structure is constructed by several pulse splitters. Because most jitter is generated from structural mismatch, all paths from clock source to each delay medium which is connected with clock line input in the pipelined-RSFQ logic require same length. Although this CDN structure is very idle, considering process variation unfortunately we can't be sure its operation.

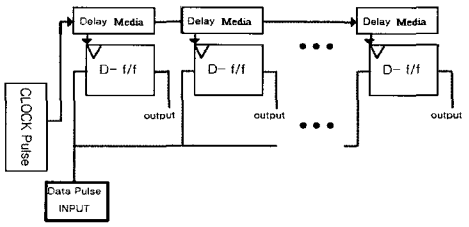

Fig. 3. Block diagram of Clock line.

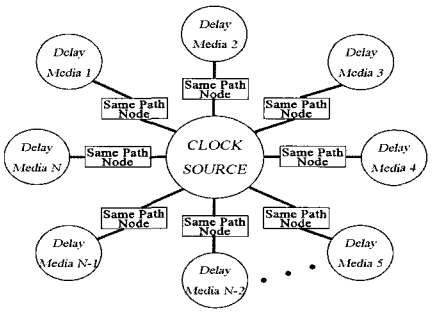

Fig. 4. Structure of Clock Distribution Net.

4. CLOCK DISTRIBUTION TECHNIQUE FOR PIPELINED-SFQ SEQUENTIAL LOGIC

Issues of CDN and pipelined-RSFQ logic are discussed in the previous section. Here, we assume that there's no process variation in CDN to apply this structure for pipelined-RSFQ logic simulation. D Flip-Flop has more slow operation speed than JTL. For ensuring operation of the sequential logic device, delay of JTL needs to be enlarged. And clock frequency is in the range of 5 ~ 20 GHz by considering these delay in the simulation.

TABLE II
SIMULATION RESULTS WITH BIAS CURRENT VARIATION

Bias current (mA)	Average delay of clock line (pS)	Average input of RSFQ sequential logic from delay pulse (pS)	Clock frequency
0.35	26.75	27	5 GHz
0.30	35.96	36.25	
0.25	55.6	55.8	
0.20	180	180.5	

Fig.5 shows simulation result of clock line structure in shown Fig. 3. This simulation is done with 5 GHz clock speed at 0.25 mA bias current. It shows that a clock line structure of pipelined-RSFQ logic works well by fixed bias current in the range of bias current margin. Table II shows the simulation results in clock line. By decreasing bias current, average delay of clock line is increased.

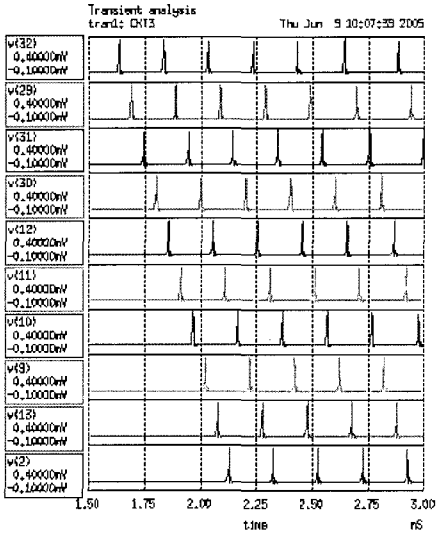

Fig. 5. Simulation result of clock line.

TABLE III
SIMULATION RESULTS OF WHOLE PIPELINED-RSFQ STRUCTURE

Parallel connected clock line	Bias current (mA)	Average delay of clock line (pS)	Average delay of sequential logic1 (pS)	Average delay of sequential logic2 (pS)	Clock frequency
Clock line 1	0.35	25.88	18.95	45.97	5 GHz
Clock line 2	0.30	33.73	18.95	52.98	
Clock line 3	0.25	48.63	18.75	68.13	
Clock line 4	0.20	69.82	18.72	87.77	
Clock line 1	0.35	25.35	19.15	46.83	10 GHz
Clock line 2	0.30	33.68	19.10	53.19	
Clock line 3	0.25	48.77	18.88	68.42	
Clock line 4	0.20	68.08	18.85	87.72	
Clock line 1	0.35	25.75	19.15	45.95	20 GHz
Clock line 2	0.30	33.96	19.15	53.01	
Clock line 3	0.25	49.25	19.02	68.25	
Clock line 4	0.20	68.78	19.01	87.65	

The entire structure is constructed with four clock lines and CDN in shown Fig. 2. The pipelined-RSFQ structure has several clock lines which are parallel connected with CDN. And each clock line is constructed serial connection of ten delay medium and D Flip-Flops. And Table III shows simulation results of whole pipelined-RSFQ structure. Because delay of clock line is determined by bias currents, each of clock lines has different delay time.

5. CONCLUSION

A new clock distribution technique is proposed for pipelined-RSFQ logics. Delay-media is constructed by simple JTLs. And its delay can be controlled by adjusting bias current. Bias current range is in the range of 0.35 ~ 0.20 mA. Delay is in the range of 10 ~ 180 pS in the simulation. Also the simulation results verify that this technique is effective and simple. Possible ways of a standard delay library with modular structure are sought for further modularizing Pipelined-RSFQ applications. Simulations and verifications are done through WRSpice with Hypres 3-um process parameters.

ACKNOWLEDGMENT

This work was supported by the GOAL-NURI (Gerontology for the Old age with an Active Life style-New University for Regional Innovation) program, Ministry of Education, Korea.

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