Trade-off Characteristic between Gate Length Margin and Hot Carrier Lifetime by Considering ESD on NMOSFETs of Submicron Technology

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Hot carrier degradation and roll off characteristics of threshold voltage (V_{tl}) on NMOSFETs as I/O transistor are studied as a function of Lightly Doped Drain (LDD) structures. Pocket dose and the combination of Phosphorus (P) and Arsenic (As) dose are applied to control V_{tl} roll off down to the 10 % gate length margin. It was seen that the relationship between V_{tl} roll off characteristic and substrate current depends on P dopant dose. For the first time, we found that the n-p-n transistor triggering voltage (V_{tl}) depends on drain current, and both I_{t2} and snapback holding voltage (V_{sp}) depend on the substrate current by characterization with a transmission line pulse generator. Also it was found that the improved lifetime for hot carrier stress could be obtained by controlling the P dose as loosing the V_{tl} roll off margin. This study suggests that the trade-off characteristic between gate length margin and channel hot carrier (CHC) lifetime in NMOSFETs should be determined by considering Electrostatic Discharge (ESD) characteristic.

Keywords : CHC lifetime, Submicron MOSFET, Threshold voltage, ESD characteristics, LDD structure

1. INTRODUCTION

The hot electron induced device degradation is a historical threat to MOSFETs reliability and poses some serious constraints in MOSFETs scaling[1]. The population of the hot carriers generated in the drain high field region, measured by the substrate current, has long been used as a key monitor for hot electron induced device degradation[2,3].

Due to the continuous downscaling of device geometries, without a corresponding decrease in the operating voltages, the electrical fields in the devices increase. Due to these field increases, two major reliability problems have become critical during the last decade. The high fields in the oxide lead to increased problems of time dependent dielectric breakdown, whereas the high fields in the silicon give rise to problems with hot carrier degradation. The latter is due to the fact that, under the influence of the high lateral fields in short channel MOSFETs, electrons and holes in the channel and pinch off regions of the transistor can gain sufficient energy to surmount or tunnel through the energy barrier between the silicon and the oxide. This leads to an injection of a gate current into the oxide and subsequently to the generation of traps, both at the interface and in the oxide, and to electron and hole trapping in the oxide, which will cause changes in transconductance, threshold voltage, and drive currents of the MOSFETs. Also, the threshold voltage depends on the temperature of the MOSFETs[4]. The hot carrier degradation problems and the technology measures taken to cope with them have had a strong influence on another

important reliability problem, namely ESD[5].

Hence, the hot carrier reliability and ESD in I/O (Input/Output) devices have become major issues for current dual or multiple oxide CMOS technologies. The roll off characteristic of threshold voltage (V_{tl}) of I/O transistor with 3.3 V operating voltage is also a major concern to get the gate length margin on deep submicron technology. Therefore, there were a lot of researches to achieve the hot carrier lifetime of device by optimization of the LDD structure maintaining device margin[6-11].

Some papers[5,12] have reported the relationship between ESD induced effects and hot carrier lifetime. However, they didn't consider the short channel margin on I/O device in dual gate oxide process.

In this paper, we experiment on characteristics of NMOSFETs with P and As dose. Also, we showed that the ESD parameter I_{t2} depends on the substrate current instead of drain current, hence that trade off between short channel margin and hot carrier reliability considering ESD can be optimized maintaining device performance or drain on-current.

2. EXPERIMENT AND ANALYSIS

The NMOSFETs used for experiments were fabricated using 0.15 μm CMOS technology with dual gate oxide process, i. e., 26 Å for 0.15 μm MOSFETs and thick oxide of 65 Å for 0.35 μm MOSFETs. Following is the key processes of used 0.15 μm CMOS technology. Shallow trench isolation (STI) with a depth of 3500 Å, retrograde twin well, dual nitrided gate oxide (NO) with a thin oxide of 26 Å for 0.15 μm MOSFETs and thick oxide of 65 Å for 0.35 μm MOSFETs, LDD and halo implantation, oxide and nitride double sidewall with a total thickness of about 1000 Å, and novel two step Co/Ti salicide with a thickness of 90/150 Å. Then, high performance back-end-of line process is applied.

To analyze the hot carrier effect, I/O devices were applied for split conditions at LDD region, which dopants consist of P and As. All other conditions are the same. The hybrid splits have P with dose ranging from 4.0×10^{13} to 5.0×10^{13} with 60 keV and As splits with dose ranging from 2.0×10^{13} to 7.0×10^{13} with 30 keV. Sample types consisted of the combination for P and As within split ranges, respectively. Also we controlled only the drain current by controlling P dose to analysis ESD characteristics when the substrate current was constant.

The trend of threshold voltage with gate lengths was compared to split conditions, and the substrate current versus the drain current curves also was plotted to analyze the electric field dependence for sample types. And the drain avalanche hot carrier (DAHC) stresses were applied to the discrete devices, where the degradation of drain saturation currents was characterized in

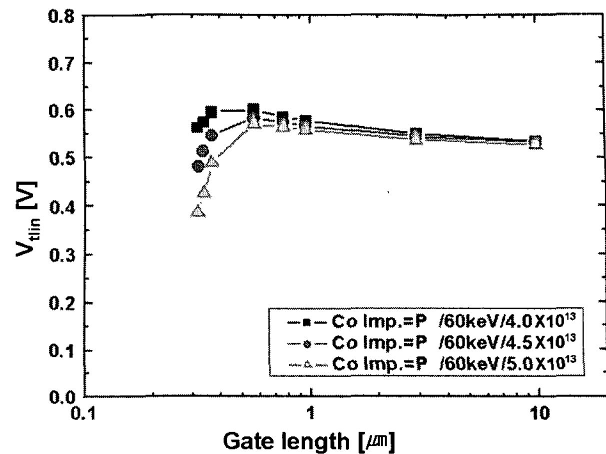

Fig. 1. The gate length dependence of threshold voltage roll-off on the P dose with constant As dose.

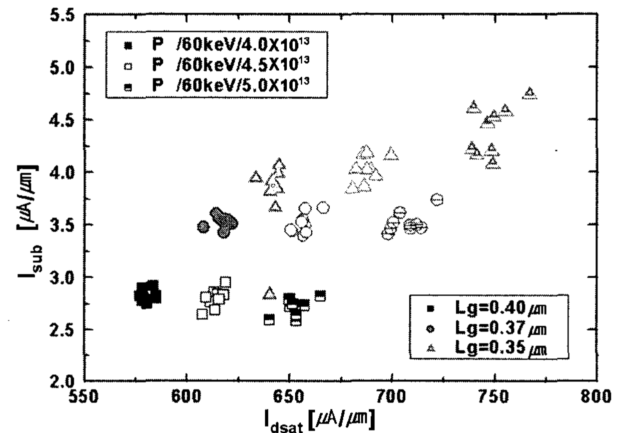

Fig. 2. The substrate current (I_{sub}) vs. the drain current (I_{dsat}) as a function of P dose.

forward mode. The ESD performance with LDD structures was measured using a transmission line pulse technique. Junction depth was extracted from SPREME IV which was tuned for the thermal budget and SIMS profile by the optimized 0.15 μm process.

3. RESULTS AND DISCUSSION

P dopant has been used to make a double diffused drain structure, which is general method to improve the lifetime by reducing the lateral electric field on I/O transistor with thick gate oxide. Figure 1 shows the gate length dependence of threshold voltage (V_{tl}) with a P dose split, where V_{tl} roll off increases as the P dose increases as it should be. Hence, we could get the good V_{tl} roll off by controlling P dose.

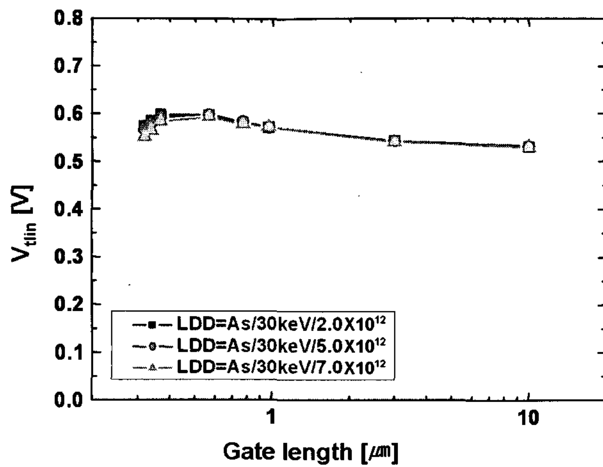

Fig. 3. The gate length dependence of threshold voltage roll-off on the As dose.

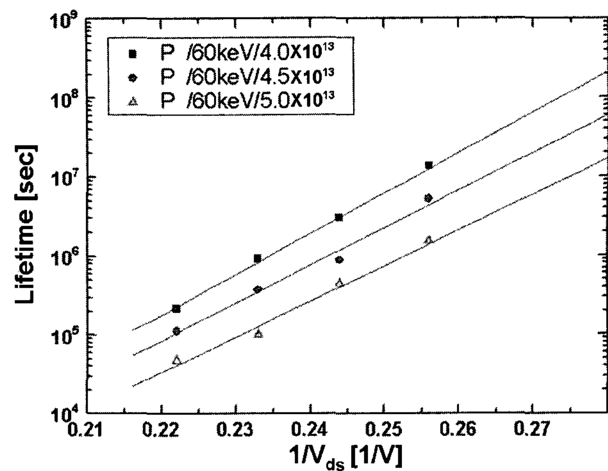

Fig. 5. The hot carrier lifetime dependence on the P dose Lifetime dependence on the P dose is due to the drain current difference.

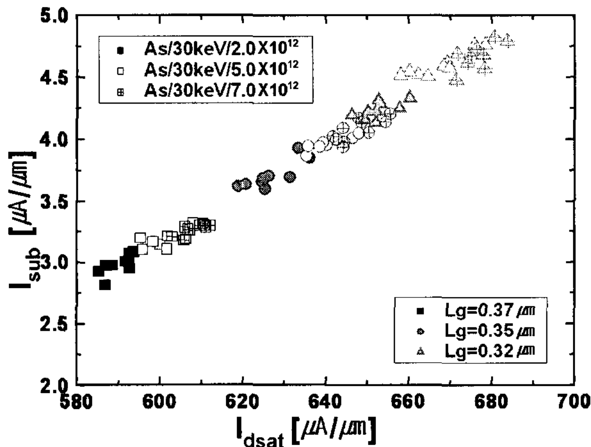

Fig. 4. The substrate current (I_{sub}) vs. the drain current (I_{dsat}) as a function of As dose.

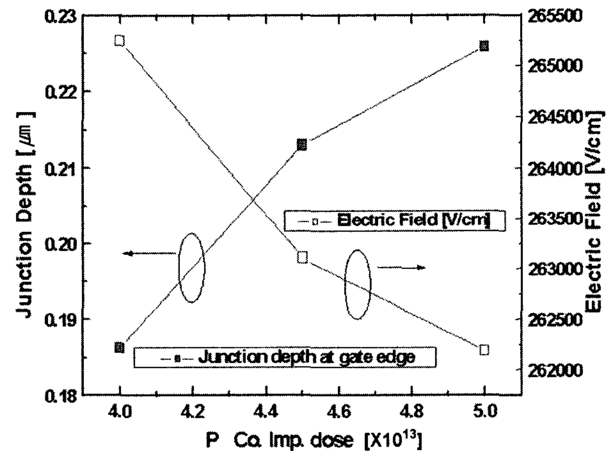

Fig. 6. Junction depth and electric field at the gate edge as a function of P dose.

To analyze the substrate current trend according to the P dose, I_{sub} vs. I_{dsat} curve was compared as shown in Fig. 2. The substrate current decreased as the gate length increased at the same P dose. When the gate length is 0.35 ㎛, the substrate current increased as the p dose increased and it is decreased more than 11 % by increasing P dose of 1×10^{13} cm^{-2}. Therefore, the P dose and the gate length on LDD is a critical factor to get the target V_{tl} roll off and substrate current, i.e., the substrate current can be controlled with a constant drain current as shown in Fig. 2.

In the case of As, the threshold voltage shows little dependence on As dose as shown in Fig. 3 and I_{sub} vs. I_{dsat} curve moves the same line with As dose splits as shown in Fig. 4 contrary to the case of P split. Therefore, drain current tuning is possible by controlling As dose without changing V_{tl} roll off.

The hot carrier lifetime is measured as a function of drain voltage under the DAHC (Drain avalanche hot carrier) stress for 0.35 ㎛ NMOSFETs as shown in Fig. 5. The device lifetime is increased as the P dose is decreased. The trend is mainly due to the increase of drain current and substrate current.

We compared the junction depth at the gate edge and the channel electric field with phosphorus dose splits. Junction depth was extracted from SPREME IV which was tuned for the thermal budget and SIMS profile by the optimized 0.15 ㎛ process. The electric field was calculated by using the junction depth and process parameters. As shown in Fig. 6, the electric field decreased for the deep junction depth, which depends on the phosphorus dose. Then, the transmission line pulse technique is used to analyze the ESD performance.

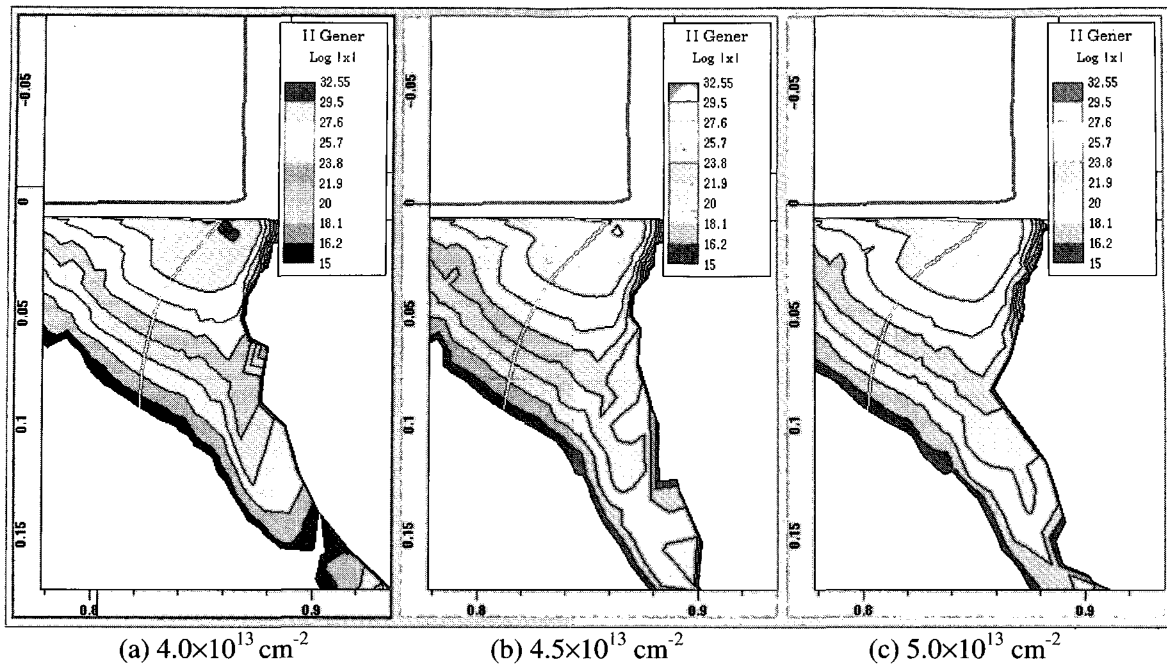

Fig. 7. Maximum impact ionization site with a split P dose.

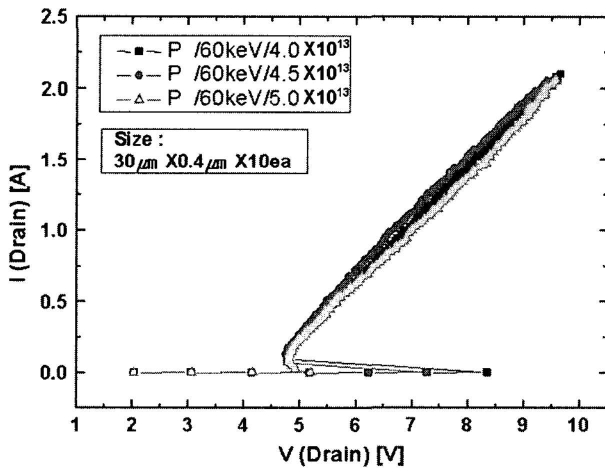

Fig. 8. I-V characteristics of multi fingered MOSFETs. V_{t1} and I_{t2} show little dependence on the P dose.

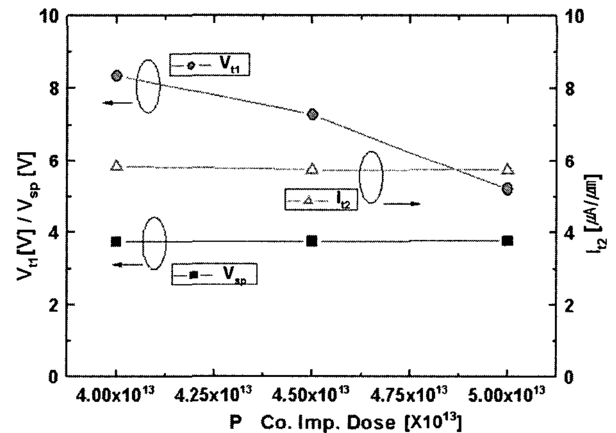

Fig. 9. Dependence of V_{t1}, I_{t2} and V_{sp} on P dose. Only V_{t1} shows strong dependence on the P dose.

To gain further insights, we simulated the maximum impact ionization site in the NMOSFETs at the maximum substrate current for V_{ds}=3.63 V. The impact ionization site for the lower P dose is located at the near the interface of SiO_2-Si surface at the gate edge and the maximum electric field (red site) is increased as the P dose decreased as shown in Fig. 7.

Figure 8 shows the typical pulsed I-V characteristics for a multiple fingered NMOSFETs as a function of P dose and Fig. 9 summarized the dependence of V_{t1}, I_{t2} and V_{sp} on P dose. As the P dose increased, I_{t2} remained constant while V_{t1} decreased and especially the highest P dose showed significant differences in the n-p-n transistor triggering voltage (V_{t1}). This lower V_{t1} value means that the avalanche multiplication process across the drain-substrate junction increases with increasing P dose, hence strongly dependent on the drain current. Contrary to V_{t1}, the snapback holding voltage, V_{sp} is nearly the same regardless of P dose split. It is also shown that the I_{t2} has similar property with V_{sp} when the substrate current was the same. The current at which second breakdown takes place is the important parameter

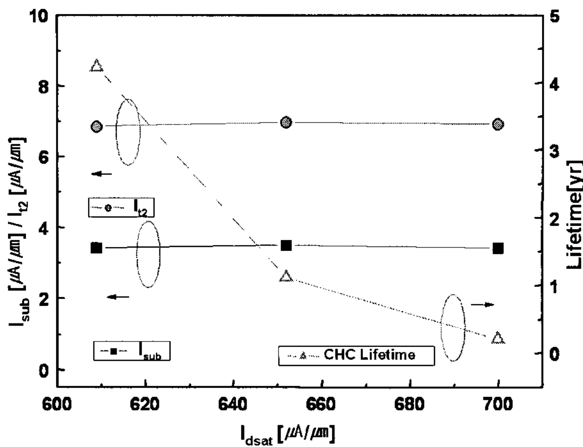

Fig. 10. Dependence of I_{t2}, I_{sub} and CHC lifetime on the drain current. Only lifetime shows strong dependence on the I_{dsat}.

for monitoring ESD robustness of a protection structure, which is widely used as the boundary condition for damage. Those similar I_{t2} and V_{sp} trend indicate that bipolar conduction is almost the same with P dose split and has little effect on the drain current. It is said that second breakdown voltage depends on substrate current.

Figure 10 shows the trend of I_{t2}, substrate current, and device lifetime as a function of drain current. Substrate current and I_{t2} show similar value regardless of drain current, but lifetime shows strong dependence. Therefore, it can be concluded that the I_{t2} depend on the substrate current and the V_{t1} depend on the drain current. Hence, the higher I_{t2} value can be obtained by only controlling the substrate current without variation of drain current.

4. CONCLUSION

In this paper, hot carrier lifetime, substrate current, roll off of threshold voltage and ESD characteristics have been investigated using hybrid As/P LDD structure on 0.15 μm CMOS technology. We found that I_{sub} vs. I_{dsat} curves shifts to the other line with P dose splits, but moves the same line with As dose splits on NMOSFETs.

From these results, substrate current and V_{t1} roll off characteristic can be controlled by combination of As/P dose. Also low substrate current shows the poor V_{t1} roll-off curve at the target drain current. We confirmed that the n-p-n transistor triggering voltage (V_{t1}) depends on drain current, and I_{t2} and V_{sp} depend on the substrate current, which is the first time to explain separately the dependence on ESD parameters for drain current and substrate current.

This study indicated that the improved device margin could obtain when V_{t1} roll off and ESD performances show good characteristics at the same drain current. Therefore, the trade-off between gate length margin and substrate current can be obtained by considering the ESD characteristics and hot carrier lifetime.

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