Correlated Effects of Decoupling Capacitors and Vias Loaded in the PCB Power-Bus

PCB Power-Bus에 장하된, 결합제거 커패시터와 금속선의 상관관계적 영향 연구

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Abstract

This paper investigates how the PCB power-bus sturcture's characteristics are influenced by the loading of decoupling capacitors in conjunction to other lumped elements including vias. The fields and impedance profiles are rigously evaluated and analyzed on various cases loaded with the above components and their effects will be given to bring better PCB EMC countermeasurs.

요 약

본 논문은 결합제거용 커패시터가 금속선을 포함한 타 집중 소자들과 함께 장하될 경우 PCB power-bus에 미치는 영향을 살펴본다. 향상된 PCB EMC 대책을 준비하는 일환으로 장하된 PCB power-bus 다양한 경우에 대해 전자장과 임피던스가 엄밀하게 계산되고 결과 분석이 이뤄진다.

Key words : PCB Level EMC, PCB Power-Bus, Decoupling Capacitors, Vias, Field Calculation

Ⅰ. Introduction

Communication systems today are typically equipped with stacked PCBs with ascending operating frequency and complexity in their architecture. The more densely each of the layers is populated, the more care needs taking of to avoid unwanted EMIs. In particular, when it comes to the digital functions together with the analog ones for one circuit, a couple of layeres are assigned as power supply planes like DC power-bus and ground, and they form cavity-type parallel plates that will possibly leave the system with spurious resonances as in area-fills[1]~[6].

To take some steps against the resonance, its precise prediction is prerequisite with rigorous analyses of the power-bus structures without any approximation[2],[3]. Based upon the results, it needs examining that placing local elements on the power plane and ground affects the initial resonances[2]~[6]. As the local components, decoupling capacitor(DeCap)s are commonly used to circumvent the resonance. However, in a significant number of cases, this is not that effective due to the disturbance of other surface mounting elements or vias.

This paper suggests the full-wave based calculation of the DC power-bus loaded with DeCaps along with vias in the same structure. Besides the electromagnetic

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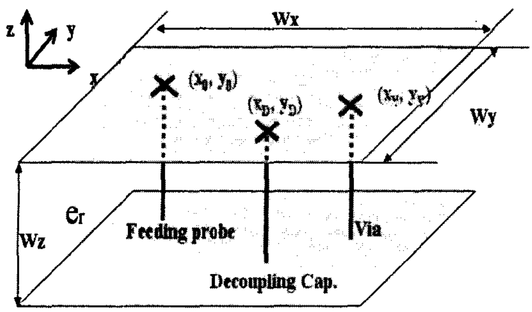


Fig. 1. DC power bus modelled as parallel-planes.

fields and impedance profiles, the correlated influence of the DeCaps and other lumped elements loaded in the structure are given.

Ⅱ. Theory

The PCB typically holds drivers, traces and receivers. Also, multiple PCBs are stacked, following the design rule to assure required EMC properties. They are connected through vias or isolated between digital and analog functions. Most of them can be considered parallel plates without loss of accuracy in electromagnetic modeling. Particularly, the DC power supply plane and its ground are a good example of parallel planes. In Fig. 1, such a structure is illustrated with W_x by W_y by W_z in size.

Using the feeding probe denoted as (X_0, Y_0), the current is given and works as the DC supply. The point of field excitation is assumed to coincide with that of the observation at (X_0, Y_0). The intermediate region between the metal planes corresponds to the PCB's substrate and 4.2 and 0.02 are each chosen as its relative dielectric constant and loss tangent, which is confined within the magnetic-walls. Outside the planes, air is assumed as the medium. The electromagnetic field(E_z) is expressed as well-known as in [2] and can be converted to the voltage or interpreted as the impedance with no difficulty. Particularly, the impedance is given as follows.

$$Z(X_0,\ Y_0 \mid X_f,\ Y_f) = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\gamma_{mn}\cdot C_{mn}(X_0,\ Y_0)\cdot C_{mn}(X_f,\ Y_f)\cdot W_z / [[\varepsilon\mu/Q + j\{\varepsilon\omega - (k_{xm}^2 + k_{yn}^2)/(\omega\mu)\}]\cdot(W_x W_y)] \quad (1)$$

where

$$C_{mn}(X,\ Y) = \cos(k_{xm}X)\cdot\cos(k_{yn}Y)$$
$$k_{xm} = m\pi/W_x,\ k_{yn} = n\pi/W_y,\ \omega = 2\pi f$$
$$Q = [\tan\delta + \{2/(\omega\mu_0\kappa W_z^2)\}^{0.5}]^{-1}$$
$$\omega_{mn} = \{(k_{xm}^2 + k_{yn}^2)/(\varepsilon\mu)\}^{0.5}$$
$$G_{mn} = C_0 \times \omega_{mn}/Q$$

γ_{mn} is 1 and 4 for (m=0, n=0) and ($m \neq 0$, $n \neq 0$) each. With ($m \neq 0$, n=0) or (m=0, $n \neq 0$), γ_{mn} is 2. $\tan\delta$, ε, μ, f and j denote loss-tangent, permittivity, permeability, frequency and $\sqrt{-1}$, respectively. Eqn. (1) itself does not have terms to consider N_{Lu} loads with the equivalent lump elements(Z_{Lu}) of which can be simply expressed as a series equivalent circuit

$$Z_{Lu} = R_{Lu} + j(\omega L_{Lu} - 1/(\omega C_{Lu})) \quad (2)$$

In order for the loading effect to be included, the following matrices can be used

$$\begin{bmatrix} V_0 \\ [V_{Lu(i)}] \end{bmatrix} = \begin{bmatrix} Z_{00} & [Z_{0,Lu(j)}] \\ [Z_{Lu(i),0}] & [Z^{Int}_{Lu(i),Lu(j)}] \end{bmatrix}\cdot\begin{bmatrix} I_0 \\ [I_{Lu(j)}] \end{bmatrix} \quad (3)$$

And

$$[V_{Lu(i)}] = -[Z^{Ext}_{Lu(i),Lu(j)}]\cdot[I_{Lu(j)}] \quad (4)$$

with

$$Z^{Ext}_{Lu(i),Lu(i)} = Z_{Lu},\ Z^{Ext}_{Lu(i),Lu(j)} = 0$$
$$Z^{Int}_{Lu(i),Lu(i)} = Z(X_{Lu(i)},\ Y_{Lu(i)} \mid X_{Lu(i)},\ Y_{Lu(j)}).$$
$$Z_{0,Lu(j)} = Z(X_0,\ Y_0,\ X_{Lu(j)},\ Y_{Lu(j)}),\ Z_{Lu(i),0} = Z(X_{Lu(i)},\ Y_{Lu(i)} \mid X_0,\ Y_0)$$

These are manipulated as

$$Z_{00} \leftarrow Z_{00} - [Z_{0,Lu(i)}]\cdot([Z^{Int}_{Lu(i),Lu(i)}] + [Z^{Ext}_{Lu(i),Lu(i)}])^{-1}\cdot[Z_{Lu(j),0}] \quad (5)$$

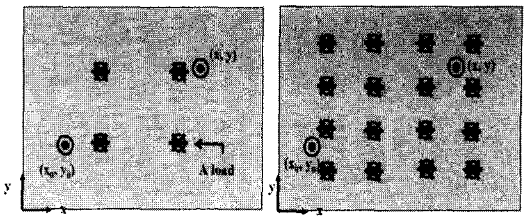
which is the generalized input impedance. The generalized trans impedance can be obtained in a similar manner. If a DeCap is placed in the structure for damping the resonance, its values will be substituted for (2).

On account of its denominator's zeroes, the impedance profile in the frequency range shows a spiky behavior as resonance. The resonance points are determined depending on size-related modes, substance and frequency. What is intriguing with the resonance is attributed to the emiited radiation, ground bounce, Delta-I noise, etc that end up with EMIs. Researches have seen the mounted elements on either or both of the parallel planes can change the resonance characteristics. Many such activities have followed the mounting of decoupling capacitors to lower the impedance's increase due to the stacked PCB's inductive loop behavior. In addition, other local elements such vias are forced to exist together with the decoupling capacitors in the same power-bus. Since it is easy to guess that they affect each other and the overall resonance characteristcis, both of them need considering for one geometry. In Fig. 1, the placement assigns a via and a decoupling capacitor at (X_D, Y_D) and (X_V, Y_V), respectively. These lumped elements' influences are reflected in the field calculation as is in [3].

Ⅲ. Numerical Results

Before starting to examine the characteristics of a variety of loads, we need to state the following. The number, positions, distribution, equivalent circuit values (R_{Lu} L_{Lu} and C_{Lu}) and combination of DeCaps are varied, and the thickness, dielectric constant and loss tangent are changed to quickly see the electromagnetic behaviors of the power-bus. And this is followed by the experiment that includes vias. All the cases go with the observation point (X=144.4 mm, Y=100 mm) and the feed point at (X_0=44.4 mm, Y_0=50 mm). The power-bus size amouns to (W_x=200 mm, W_y=150 mm, W_z=1.5 mm).

Firstly, we investigate the impedance of the power-



(a) (b)

Fig. 2. 4 and 16 DeCaps evenly placed in the DC power bus.

bus when we change the number, distribution and positions of DeCaps. Four cases are dealt with, where 4, 16, 25 and 36 DeCaps are evenly distributed in the power-bus. They look like sqaure matrices of DeCaps' positions. The 4 and 16 DeCaps are placed as follows.

For evaluating the impedance between (X_0, Y_0) and (X, Y), all the DeCaps are given 7.3 nF as capacitance, 0.5 nH as ESL, and 85 mΩ as ESR which is commercially available. Now we compare how the 4, 16, 25 and 36 DeCaps affect the impedance(Fig. 3).

Seeing Fig. 2, it is obvious the more DeCaps are placed in the power-bus, the wider becomes the resonance-suppressed regime. Particularly, from the use of 16 DeCaps, the impedance can be lowered by over 40 dB at 500 MHz with respect to the 4 DeCap-case. Next, we are dealing with the rectangular matirces of DeCap positions. Example 1 is to compare 2-by-4 and

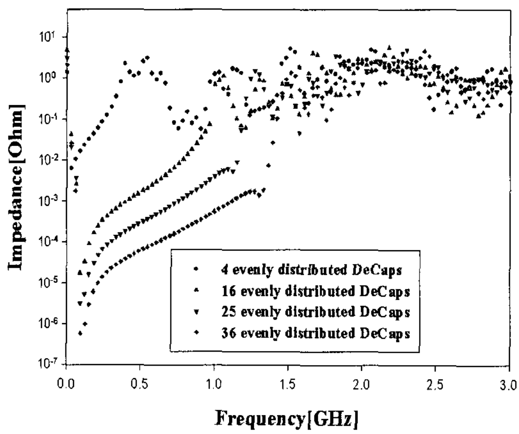
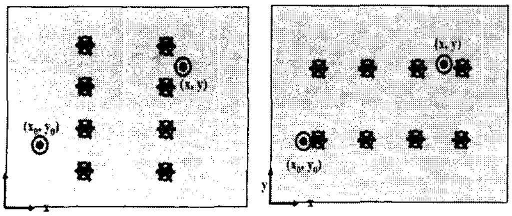


Fig. 3. Impedance for the 4 16, 25 and 36 DeCap placement.



(a) (b)

Fig. 4. 2-by-4 and 4-by-2 rectangularly placed DeCaps.

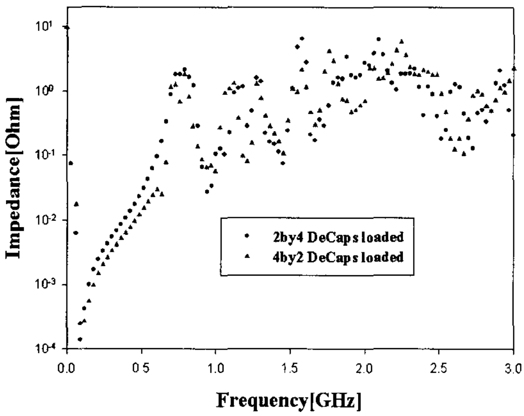


Fig. 5. Impedance of the 2-by-4 and 4-by-2 rectangularly placed DeCaps.

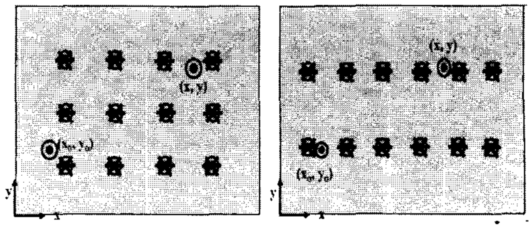
4-by-2 rectangular distribution. Each of them has 8 DeCaps in a total. The following shows the illustration of these two ways of placement.

When the impedance is calculated, all the DeCaps are assumed the same as those of Fig. 3.

Example 1 results in not much difference between the two cases, since the density of population is close to each other. However, the 4-by-2 case is superior to the other in noise-suppression around 500 MHz, because DeCaps are in the vicinity of both the two ports. Similary, in Example 2, 12 DeCaps are laid in two distribution cases as 4-by-3 and 6-by-2. They are illustrated as follows.

Solving Example 2 on the rectangular matrix of placement, the DeCaps are identical with Fig.s 3 and 5.

Fig. 7 tells us that both the cases have a similar tendency in the higher frequency regime over 600 MHz. However, the 6-by-2 case shows superiority in lowering



(a) (b)

Fig. 6. 4-by-3 and 6-by-2 rectangularly placed DeCaps.

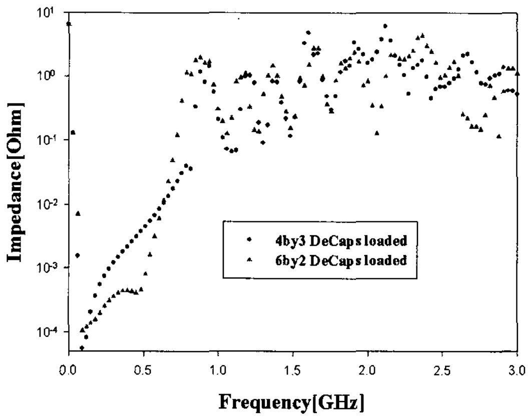


Fig. 7. Impedance of the 4-by-3 and 6-by-2 rectangularly placed DeCaps.

the impedance at less than 600 MHz, to the 4-by-3 case, since the ports of the former case are closer to their adjacent DeCaps, compared to the latter.

Secondly, the combinations of different DeCaps are studied with a fixed square matrix of placement. The 2-by-2 case is mentioned again and 4 positions are marked with numbers as follows.

Two types of DeCaps are used. DeCap 1 has 7.3 nF as capacitance, 0.5 nH as ESL, and 85 mΩ as ESR.

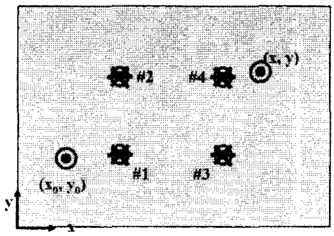


Fig. 8. 4 DeCaps in a 2-by-2 square matrix of placement.

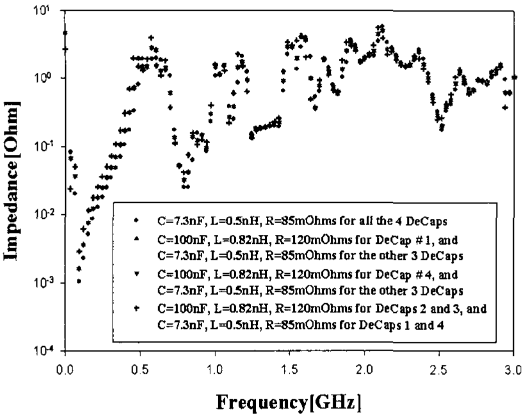


Fig. 9. Impedance of 4 combinations of DeCaps 1 and 2.

DeCap 2 is given 10 nF as capacitance, 0.82 nH as ESL, and 120 mΩ as ESR. 4 cases of combinations are considered as 'DeCap 1 for all the positions', 'DeCap 2 for #1 and DeCap 1 for #2, #3 and #4', 'DeCap 2for #4 and DeCap 1 for #1, #2 and #3', and 'DeCap 2 for #2 and #3 and DeCap 1 for #1 and #4'.

According to Fig. 9, all the combinations there result in similarity, since there is no change in the spatial relationship between the 4 positions and ports, without regard to the two different kinds of DeCaps. It is noteworthy that using DeCaps of type 1 can be more effective than the mixture of the two kinds in this experiment.

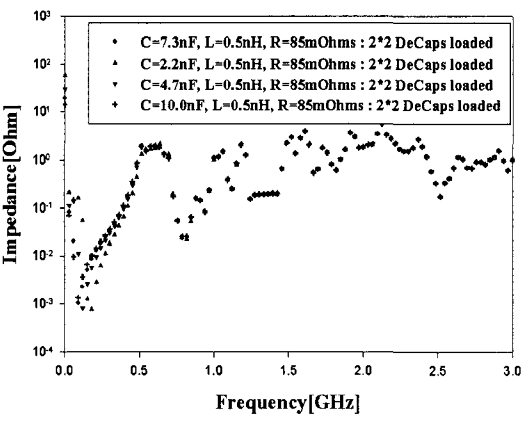


Fig. 10. Impedance of the power-bus loaded with 4 DeCaps with changed capacitance, but with unchanged ESL and ESR.

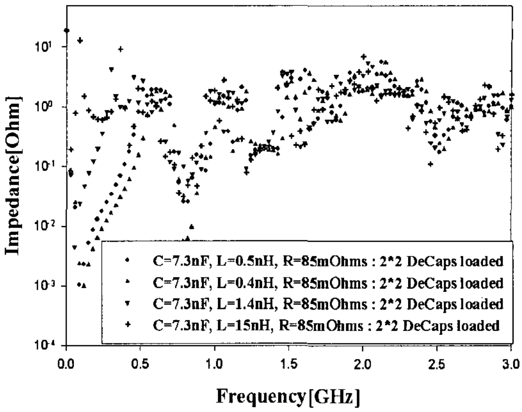


Fig. 11. Impedance of the power-bus loaded with 4 DeCaps with changed ESL, but with unchanged capacitance and ESR.

Thirdly, we are varying the capacitance of DeCaps. The DeCaps are distributed as Fig. 8 for the sake of convenience. The ESL and ESR remain unchanged as 0.5 nH and 85 mΩ, respectively.

The major variation is seen in the region less than 500 MHz, because the capacitance ranges far greater than pF. As the capacitance rises, the dip in the lower frequency area moves toward the DC point.

Fourthly, we are changing the ESL of DeCaps from 0.4 nH through 15 nH. The the capacitance and ESR remain unchanged as 7.3 nF and 85 mΩ, respectively.

Different from Fig. 10, the rise in the ESL influences the impedance more seriously. The increasing ESL moves the dip point down in the lower frequency region, for the dip is equivalent to the admittance's resonance. And the admittance can be affected by inductance with higher sensitivity for this cavity structure.

Fifthly, with the capacitance and ESL of DeCaps constant as 7.3 nF and 0.5 nH respectively, the ESR changes from 55 mΩ through 104 mΩ.

As is clearly seen, the change in the ESR can not cause the shift of the resonance points. Especially, as the ESR lies in mΩ, all the results of Fig. 12 look quite similar.

Sixthly, we are presenting the impedance of the unloaded structure in accordance with the change in the

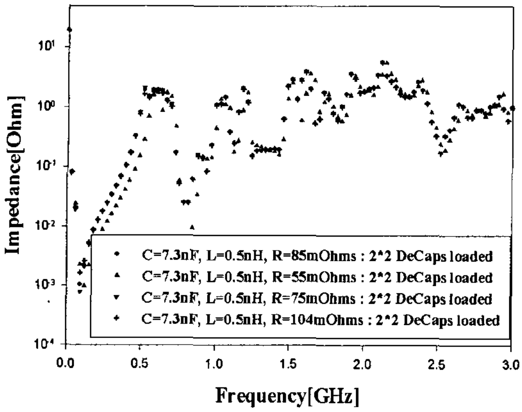


Fig. 12. Impedance of the power-bus loaded with 4 DeCaps with changed ESR, but with unchanged capacitance and ESL.

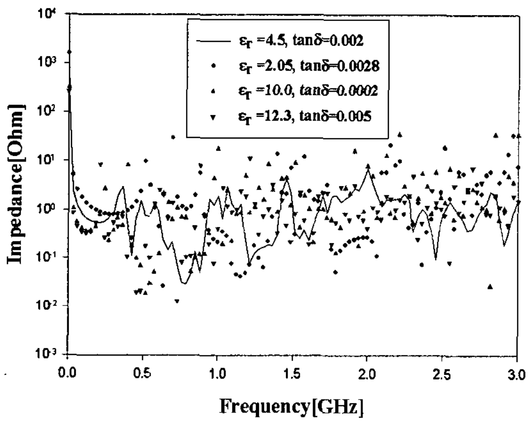


Fig. 13. Impedance of the unloaded power-bus with 4 cases of substrates.

dielectric constant and loss tangent of the substrate. We have chosen four substrates that are practically used. Case 1 is the substrate that has been used from beginning in this paper. Cases 2, 3, and 4 are Teflon, Alumina and Silicon, respectively.

All the substrates are 1.5 mm thick. As was expected, the increasing dielectric constant of the substrate tends to make the cavity electrically larger and lead to more cavity resonance points.

Seventhly, the thickness of the unloaded structure's substrate is changed. Cases 1, 2, 3, and 4 have 1.5 mm, 2.0 mm, 2.5 mm and 3.0 mm.

Lastly, the structure is dealt with for 4 different

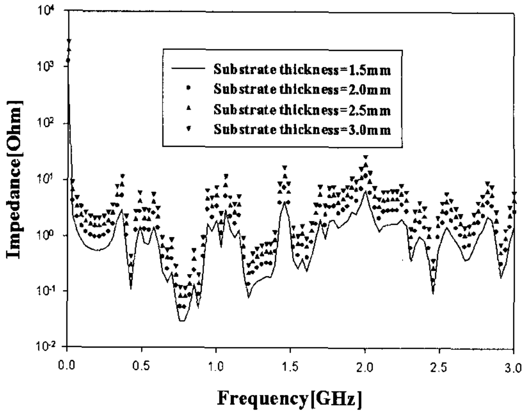


Fig. 14. Impedance of the unloaded power-bus with 4 cases of thickness.

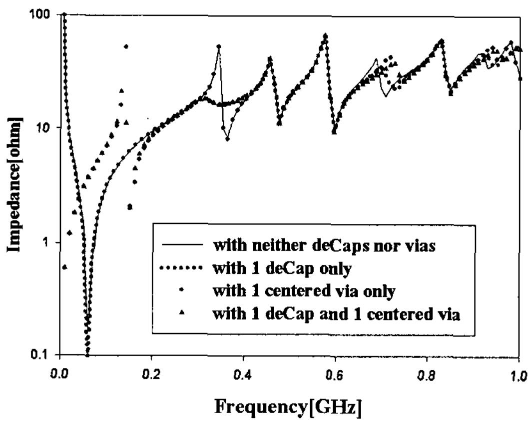


Fig. 15. Input impedance of the power bus with and without loading of the DeCap and the via.

loading conditions. The cases are of no loading, only 1 DeCap, 1 via, and 1 DeCap and 1 via., with (X_0=0, Y_0=0), and 1 via at (X_V=100 mm, Y_V=75 mm) and 1 DeCap at (X_D=200 mm, Y_D=75 mm) are used. The DeCap has C_D=47 pF with R_D=5.2 Ohms and L_D=3.8 nH Similarly, the value of the via is given as L_V=1.097 nH as can be done in [5].

As case 1 goes with neither vias nor DeCaps, it shows its original resonance modes. With only the DeCap loaded, case 2 sees the successful damping of (1, 0)-mode. It is a matter of course that the other resonance modes at higher frequencies undergo slight changes. In case 3, a via centered at the planes shifts (2, 0) and (0, 2) modes and results in no intended damping,

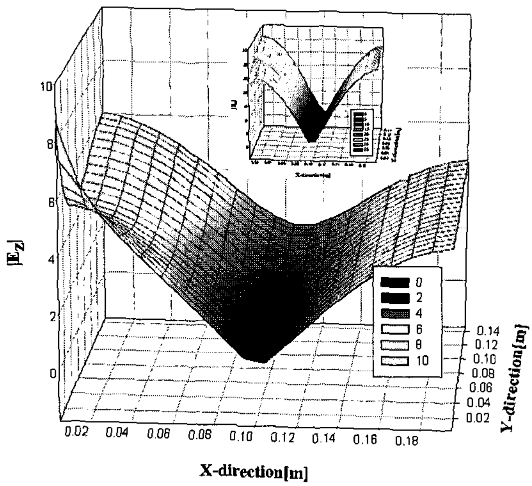


Fig. 16. E_z over the DC power bus with the DeCap (Inset: without the DeCap).

but causes an additional resonance around 120 MHz which is believed to be a critical noise. This via still brings that extra resonance with (1, 0) resonance mode damped by the DeCap in case 4. These noises could stem from added inductance. As of now, we'll take a gander at the field distribution(E_z) over the DC power-bus, for it will make things clear. Primarily, E_z is plotted with and without the DeCap at 376 MHz of (1, 0)-mode.

Without any loading except for the feed, E_z is formed satisfying (1, 0)-resonance mode condition where along the edges one half wavelength and zero variation of E_z are seen along the x and y-directions, respectively. And the intensity of E_z is of significance. Applying the DeCap to it, the damping occurs and is quite effective, since most of the plane area comes to have reduced intensity. Secondarily, the via is added to the DeCap. The location is the center of the planes and the simulation is performed at 376 MHz as before.

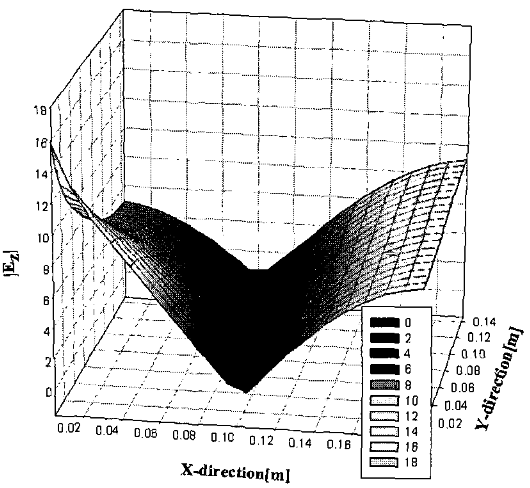


Fig. 17. E_z over the DC power bus with the DeCap and the via.

Obviously, the DeCap dominantly lowers the intensity of E_z in both the cases. And note the via at the center plays an important role in reducing more of the resonance, while the E_z has not changed a bit right at the feeding point. Going through the macro-model pole extraction, it is found out that below (1, 0)-mode frequency, the DeCap loaded case has no complex poles with $-14{,}952$ and -5.19×10^9 (like LPF), while the addition of via results in the poles at $-4.32\times10^6 \pm j\,0.184\times10^9$ with $j=\sqrt{-1}$(like BPF). At this point, one must bear in mind that if the via is placed near a null of E_z that is primarily damped by the DeCap correlated effects of damping can be achieved.

Ⅳ. Conclusion

Considering the EMI-causing resonance related to the DC power-bus modelled as cavity-type parallel planes, the structure's field and impedance are rigorously evaluated. Based upon this prediction method, positions and values of DeCaps are tried in the power-bus to damp the undesirably high impedance with resonance. This can lead to success in suppressing the specific resonance. Particularly, this paper enlightens the way DeCaps can be affected by other lumped elements like vias and other physical input-parameters in a variety of manners for coping with better PCB EMC countermeasures. And their LPF and BPF behaviors have been mentioned in terms of pole extraction.

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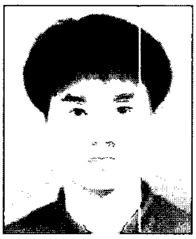

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