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Thermo-piezoelectric Si_3N_4 cantilever array on a CMOS circuit for probe-based data storage using wafer-level transfer method

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Abstract

In this research, a wafer-level transfer method of cantilever array on a conventional CMOS circuit has been developed for high density probe-based data storage. The transferred cantilevers were silicon nitride (Si_3N_4) cantilevers integrated with poly silicon heaters and piezoelectric sensors, called thermo-piezoelectric Si_3N_4 cantilevers. In this process, we did not use a SOI wafer but a conventional p-type wafer for the fabrication of the thermo-piezoelectric Si_3N_4 cantilever arrays. Furthermore, we have developed a very simple transfer process, requiring only one step of cantilever transfer process for the integration of the CMOS wafer and cantilevers. Using this process, we have fabricated a single thermo-piezoelectric Si_3N_4 cantilever, and recorded 65nm data bits on a PMMA film and confirmed a charge signal at 5nm of cantilever deflection. And we have successfully applied this method to transfer 34 by 34 thermo-piezoelectric Si_3N_4 cantilever arrays on a CMOS wafer. We obtained reading signals from one of the cantilevers.

Key Words : Thermo-piezoelectric Si3N4 cantilever, PZT, probe-based data storage, wafer level transfer

1. Introduction

Probe-based data storage has been studied extensively to overcome the storage density limits of HDD and semiconductor memories. In our previous studies, a thermo-piezoelectric read/write mechanism with a resistively heated AFM tip and a piezoelectric PZT sensor was developed, as shown in Figure 1 [1, 2]. The resistively heated tip writes data bits by scanning over a polymer media and a piezoelectric sensor reads data bits using the self-generated charges induced by the deflection of cantilever as it scans across the indentations on the polymer media. To improve the uniformity and mechanical stability of the cantilever array, silicon nitride film was used to fabricate the cantilevers. Previously, *Vettiger et.al* developed a CMOS back end of the line (BEOL) method compatible with wafer-scale device. However, this technology requires a two-step bonding process; in the first step, cantilevers are transferred onto a glass wafer, and in the second step, they are transferred onto the CMOS wafer. Moreover, this transfer method requires a SOI wafer for cantilever uniformity [3].

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2. Results and Discussion

In our fabrication process, a conventional p-type wafer instead of SOI wafer is needed to fabricate the cantilever array since silicon nitride film is used to fabricate cantilever. Moreover, only one step is needed to transfer cantilever array on a CMOS wafer because CMOS wafer can be integrated before removing the seed wafer. Figure 2 summarizes this wafer-level transfer method of the thermo-piezoelectric Si_3N_4 cantilever array As summarized in Figure 2, it consists of Si_3N_4 cantilevers deposited by LPCVD, the cantilever tips formed by KOH

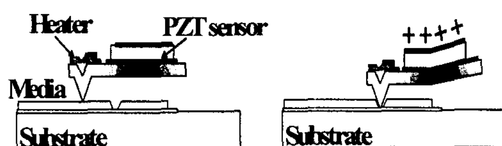

Fig. 1. Reading mechanism of a thermo-piezoelectric Si_3N_4 cantilever.

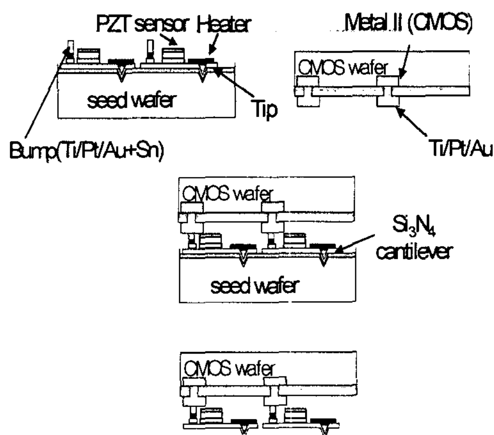

Fig. 2 Fabrication process of wafer-level thermo-piezoelectric Si_3N_4 cantilever transferred on a conventional CMOS wafer.

etching process, poly silicon heaters on the tip side and the PZT capacitors. A stack of Ti/Pt/Au metal layers has been deposited on the interconnection part of CMOS wafers and a stack of Ti/Pt/Au+Sn bumps were formed as pads on the cantilever array side to form an interconnection between the cantilever array and the CMOS wafer. During the wafer-level bonding, the condition for the pressure and temperature was 10 bar and 300 °C, respectively. Figure 3 shows the scanned data bits of 65 nm in diameter and a reading signal at 5 nm depth using the single cantilever. Figure 4 shows the microscope image of thermo-piezoelectric Si_3N_4 cantilevers transferred on the dummy CMOS wafer. Figure 5 shows the charge signal using the fabricated cantilever. Moreover, the 34 x 34 thermo-piezoelectric Si_3N_4 cantilever array was successfully integrated on a CMOS wafer as shown in Figure 6. Figure 7 shows several SEM images of this cantilever array where the estimated deflection of the cantilever is approximately 2.25 um, the tips were very sharp and the initial bending of the cantilever array was very uniform. Using the proposed wafer-level transfer technology, 34 x 34 thermo-piezoelectric Si_3N_4 cantilever arrays on a CMOS circuit were successfully fabricated. Silicon nitride film was used to fabricate cantilevers and tip for thickness uniformity and mechanical stability. This method can lower the fabrication cost where a conventional p-type wafer is needed to fabricate the thermo-piezoelectric Si_3N_4 cantilever arrays. Furthermore, this method is simple requiring only one step to integrate CMOS wafer and the cantilever array since the seed wafer does not

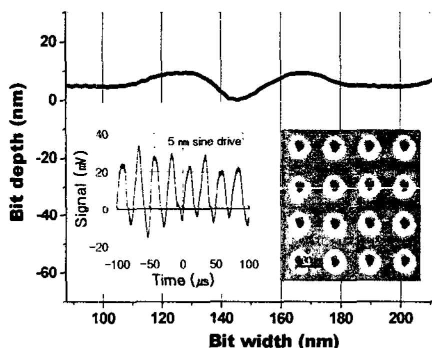

Fig.3 Read/write signals using single transferred thermo-piezoelectric Si_3N_4 cantilever. The inset figures show readback signal(left) and a scanned image of data bits(right).

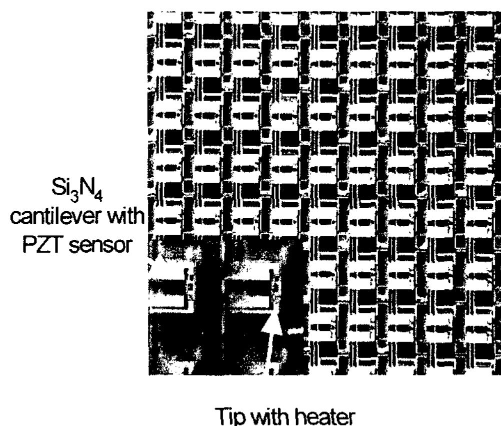

Fig. 4 A microscope image of the transferred cantilever array on a dummy CMOS wafer.

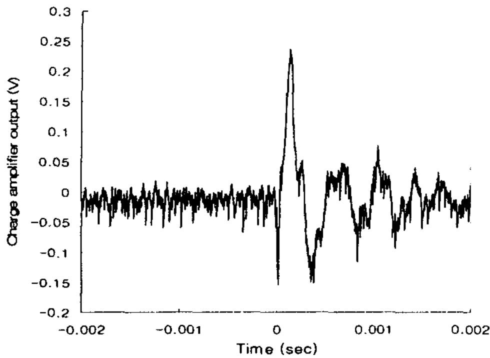

Fig. 5 Readback signal using one of the transferred cantilever array.

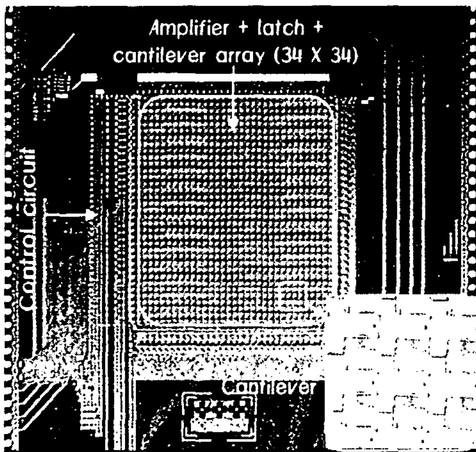

Fig. 6 Microscope image of the transferred 34 X 34 cantilever array on a CMOS wafer

need to be removed before the integration. Moreover, the read/write signals were successfully obtained using the fabricated cantilever array. Further studies to read and write data bit using our cantilever array with CMOS control circuit, and to build the overall systems are required.

3. Conclusion

In this research, we have developed a technology of wafer-level transfer of cantilevers on a conventional CMOS wafer for batch fabrication of system on a chip.

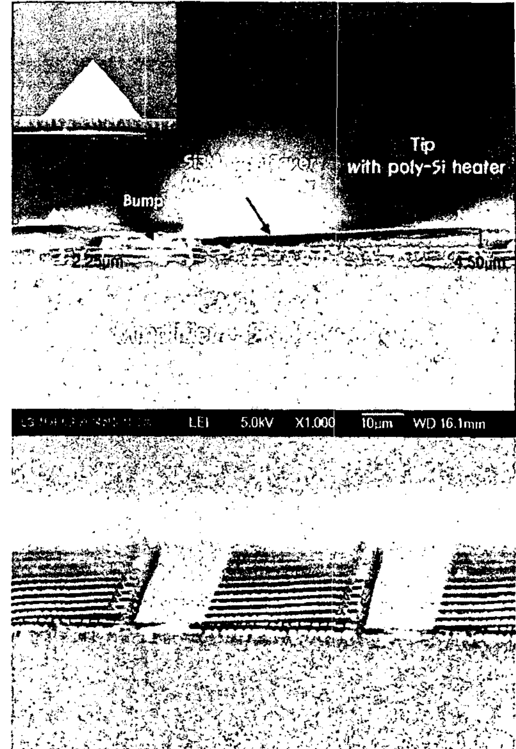

Fig. 7 SEM image of the transferred cantilever array on a CMOS wafer

The transferred cantilevers were silicon nitride (Si_3N_4) cantilevers integrated with poly-silicon heaters and piezoelectric sensors, called thermo-piezoelectric Si_3N_4 cantilevers, for thermo-mechanical writing and piezoelectric readback on a polymer film for low power probe based data storage system. In this process, we did not use a SOI wafer but a conventional p-type wafer for the fabrication of the thermo-piezoelectric Si_3N_4 cantilever arrays. Furthermore, we have developed a very simple transfer process, requiring only one step of cantilever transfer process for the integration of the CMOS wafer and cantilevers. Using this process, we have fabricated a single thermo-piezoelectric Si_3N_4 cantilever, and recorded 65nm data bits on a PMMA film and confirmed a charge signal at 5nm of cantilever deflection. And we have successfully applied this method to transfer 34 by 34 thermo-piezoelectric Si_3N_4 cantilever arrays on a CMOS wafer. We obtained reading signals from one of the cantilevers.

Acknowledgment

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